DESCRIPTION

MGFS39E2527A is a 4-stage amplifier designed for WiMAX CPE.

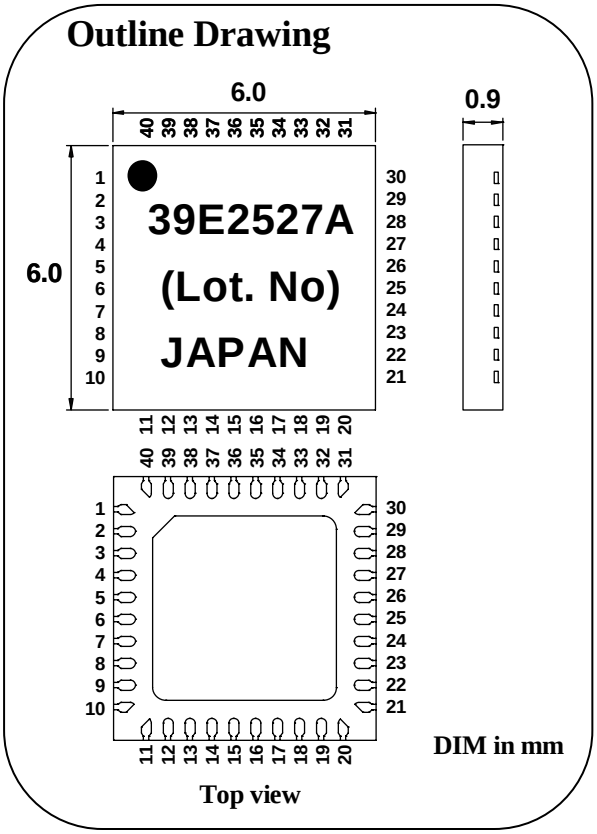
FEATURES

- InGaP HBT Device
- 6V Operation
- 30dBm Linear Output Power (64QAM, EVM=2.5%)
- 40dB Linear Gain
- Integrated Output Power Detector
- Integrated 1-bit Step Attenuator
- Surface Mount Package
- RoHS Compliant Package

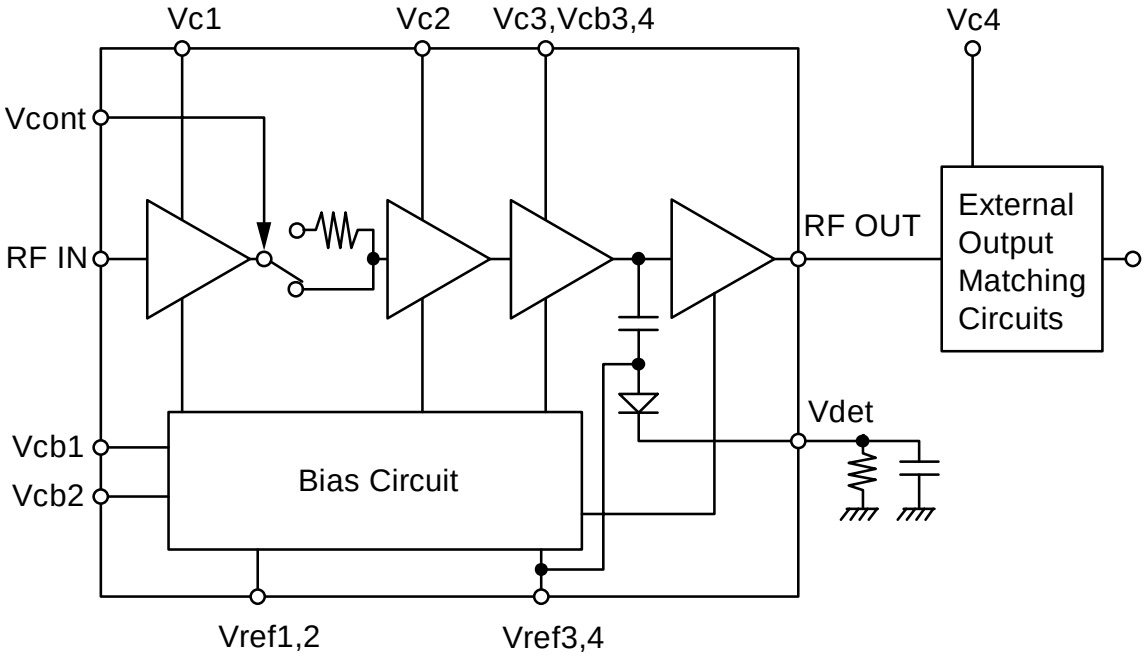
APPLICATION

IEEE802.16-2004

Outline Drawing



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Value	Unit
Vc1,Vc2, Vc3,Vc4, Vcb1,Vcb2 Vcb3,Vcb4	Collector Supply Voltage	-	8	V
Vref	Reference Voltage	-	3	V
Vcont	ATT Control Voltage	-	3.3	V
Ic1	Operation current	-	80	mA
Ic2			300	mA
Ic3			300	mA
Ic4			2000	mA
Pin	Input Power	-	-3	dBm
Tj	Junction Temperature	-	160	deg.C
Tc(op)	Operation Temperature	Pout<=30dBm Duty<=50%	-40 to +85	deg.C
Tstg	Storage Temperature	-	-40 to +125	deg.C

NOTE :
Each maximum rating is guaranteed independently.
Please take care that MGFS39E2527A is operated under these conditions at the worst case on your terminal.

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
f	Frequency		2.500		2.700	GHz
Gp	Gain	Vc=6V, Vref=2.85V		42		dB
Ict	Total current	Pout=30dBm		1250		mA
EVM	EVM	64QAM OFDM Modulation		2.5		%
RLin	Input Return Loss	Duty Cycle <= 50%		10		dB
Vdet	Power Detector Voltage			1.5		V
ATT	Control Gain Step			19		dB

NOTE : Zin=50 Ohm, Zout : Measured with application circuit

ESD RATING : Class 2 (HBM)

MOISTURE SENSITIVITY LEVEL : LEVEL3

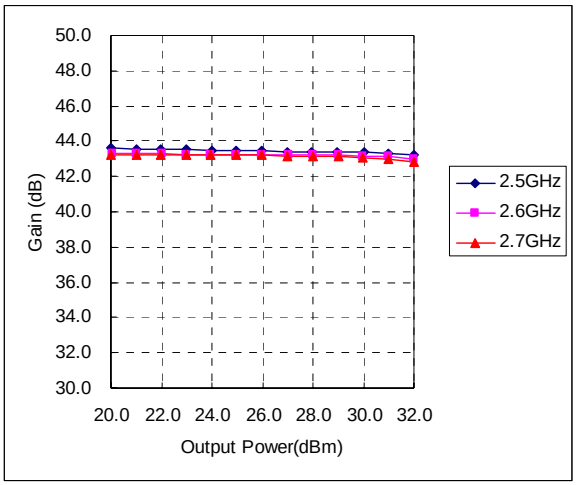
THERMAL RESISTANCE : 4.0 deg.C/W

(The thermal resistance of the 4th stage is calculated as 5.5 deg.C/W)

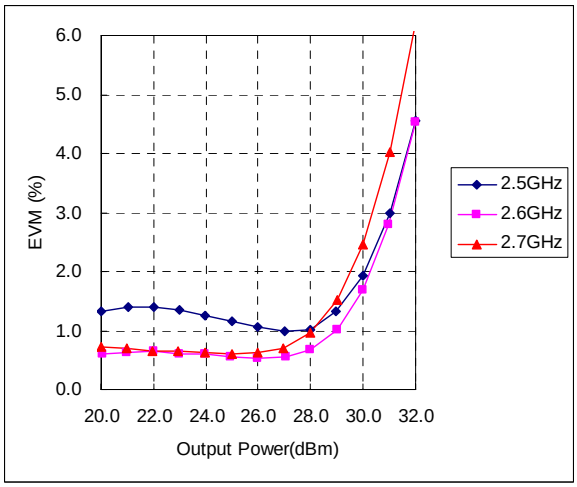
PERFORMANCE DATA (WiMAX OFDM 64QAM signal input)

- Vc=6V Ta=25deg.C

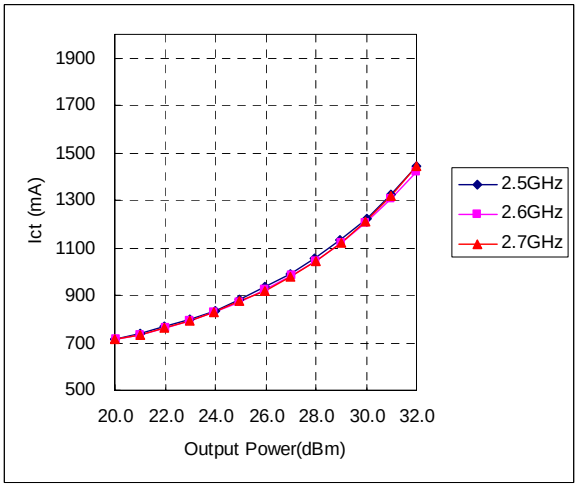
Gain vs. Output Power



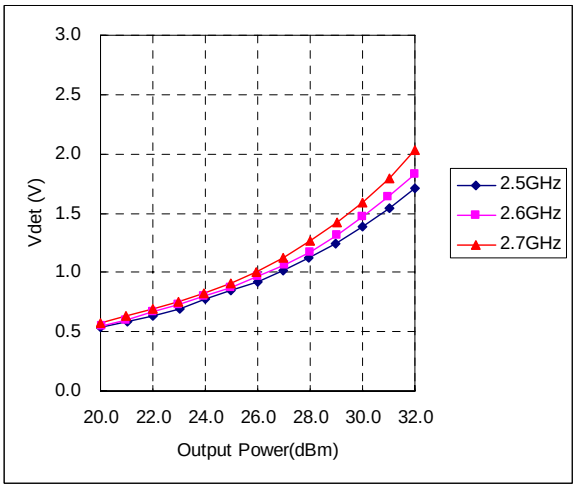
EVM vs. Output Power



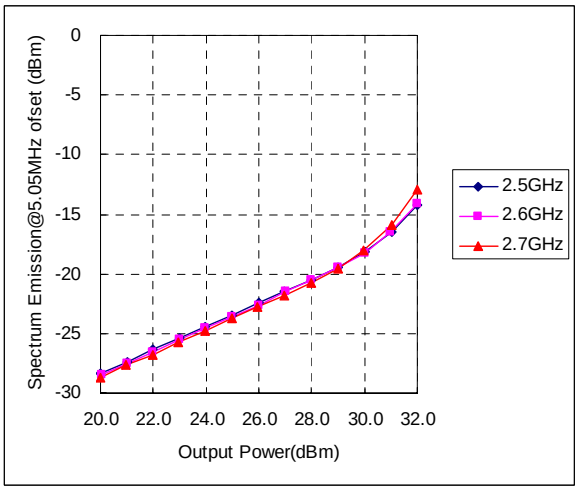
Collector Current vs. Output Power



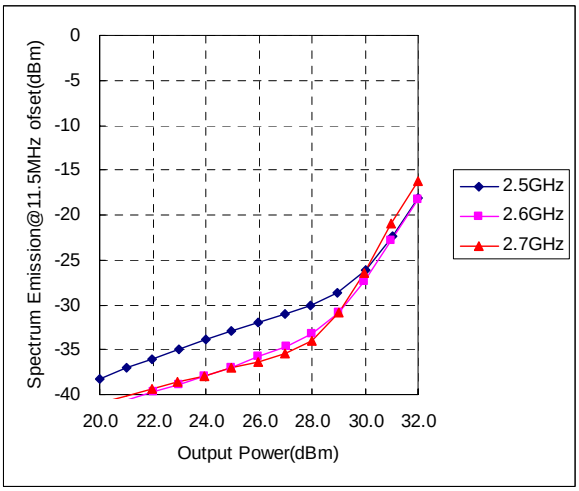
Detector Voltage vs. Output Power



Spectrum Emission Mask

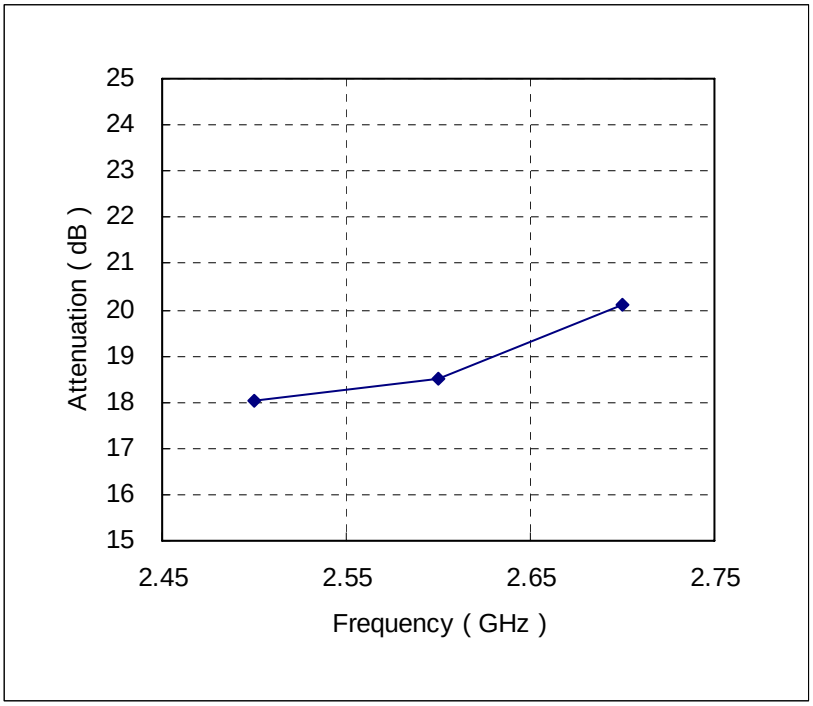


(a)5.05MHz offset

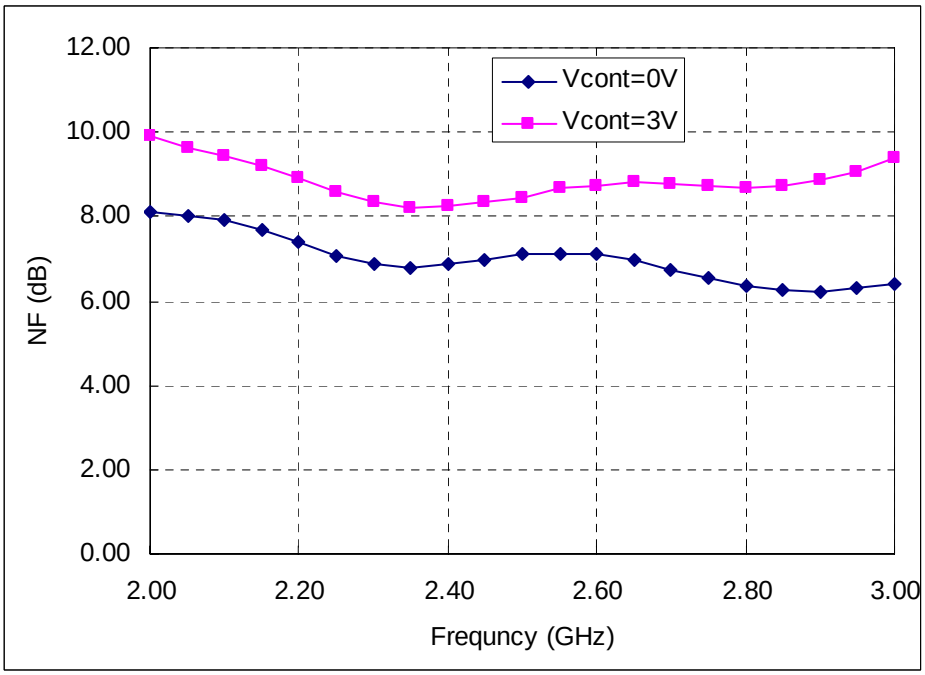


(b)11.5MHz offset

Attenuator Performance

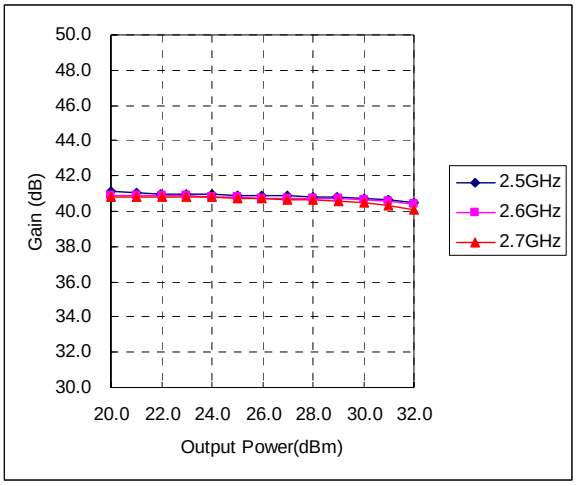


Noise figure

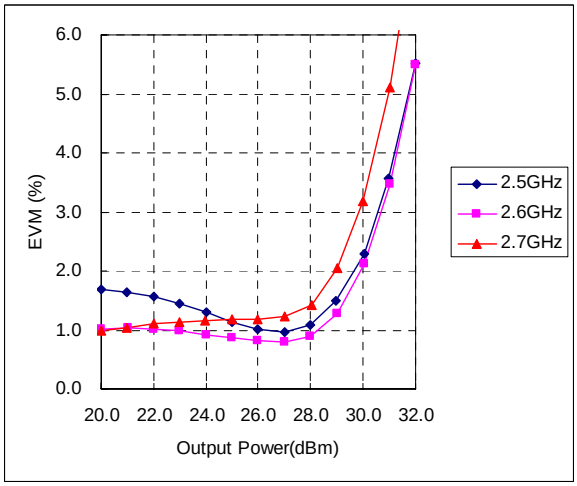


- Vc=6V Ta=85deg.C

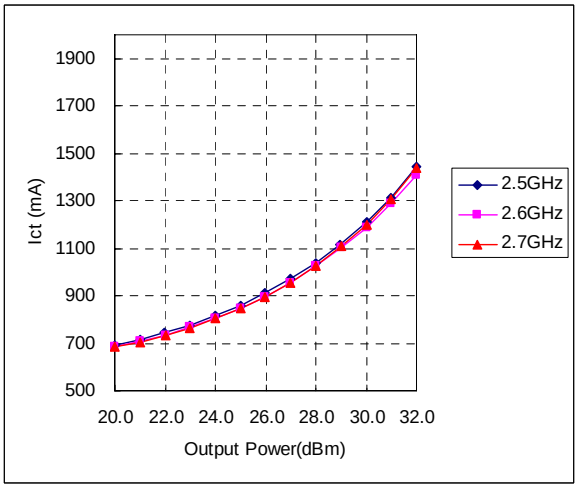
Gain vs. Output Power



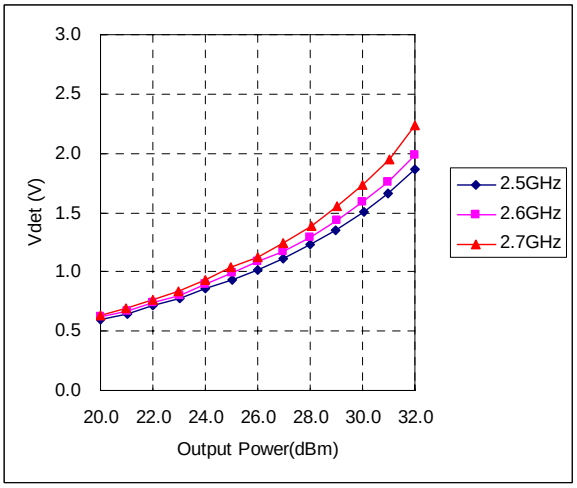
EVM vs. Output Power



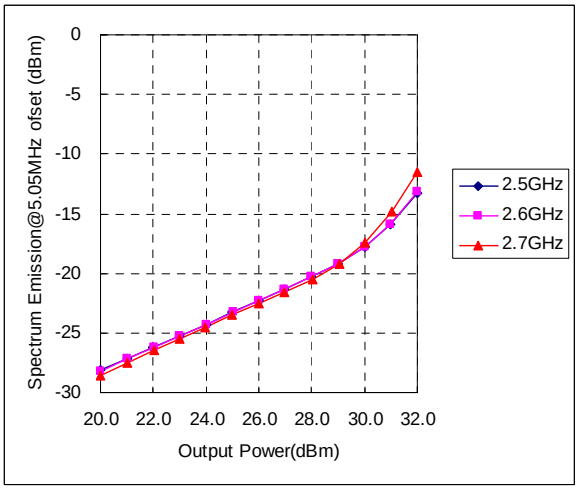
Collector Current vs. Output Power



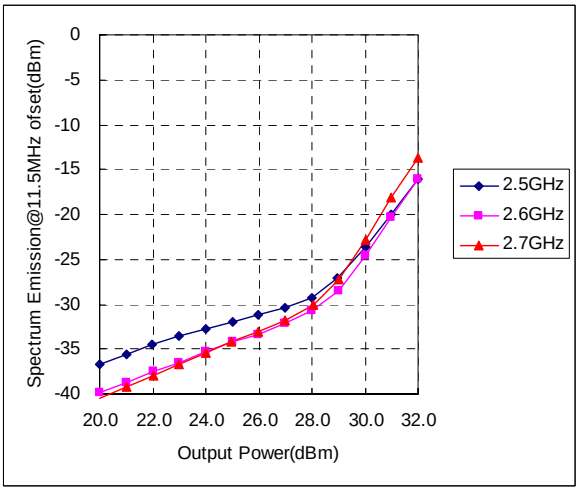
Detector Voltage vs. Output Power



Spectrum Emission Mask

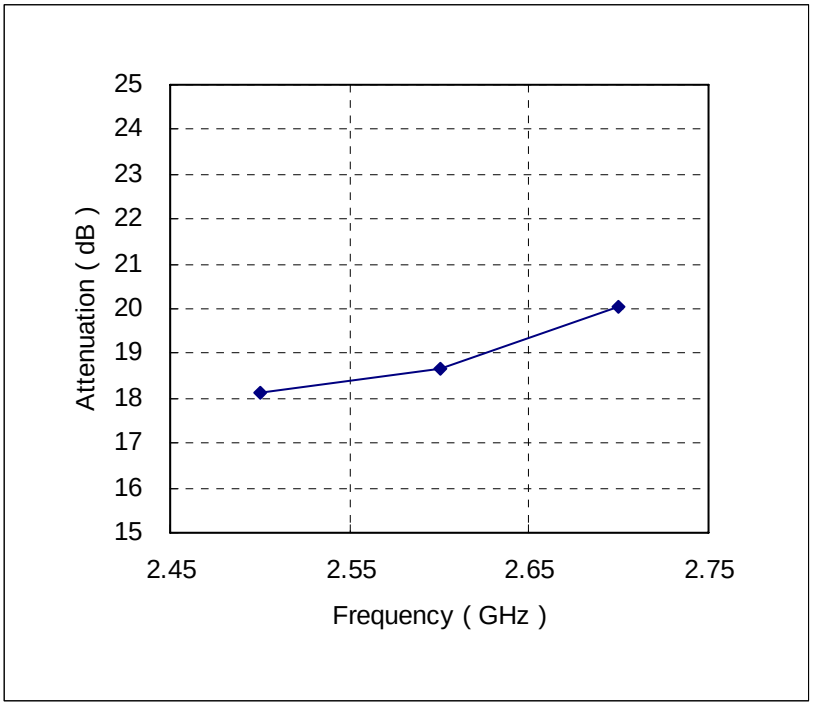


(a)5.05MHz offset

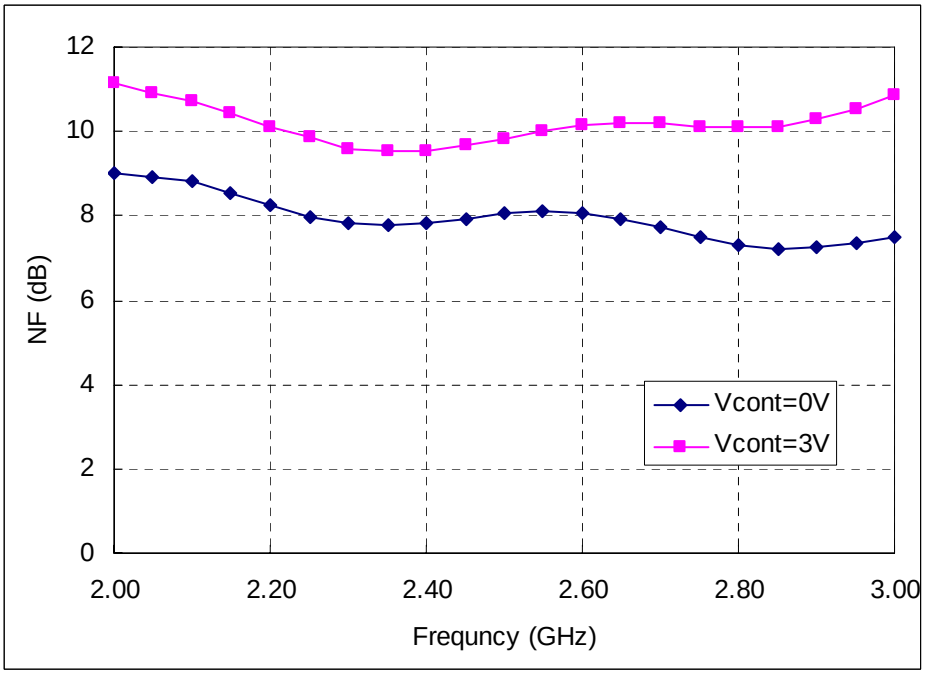


(b)11.5MHz offset

Attenuator Performance

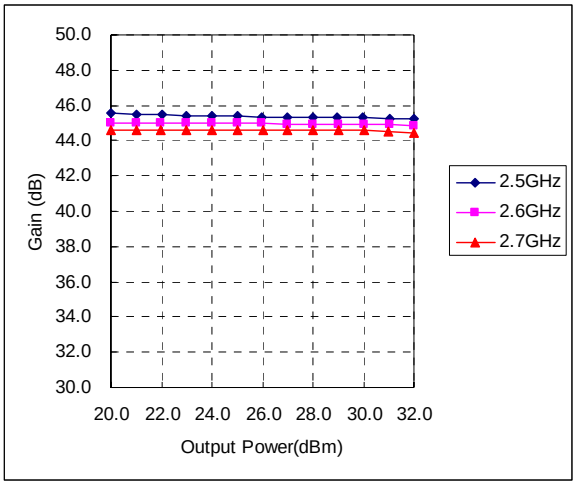


Noise figure

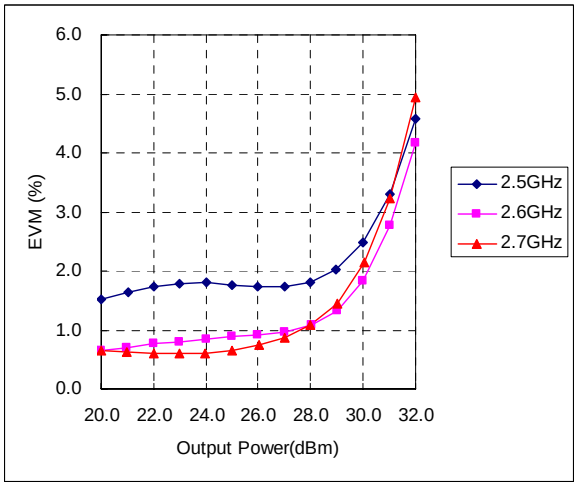


- Vc=6V Ta=-40deg.C

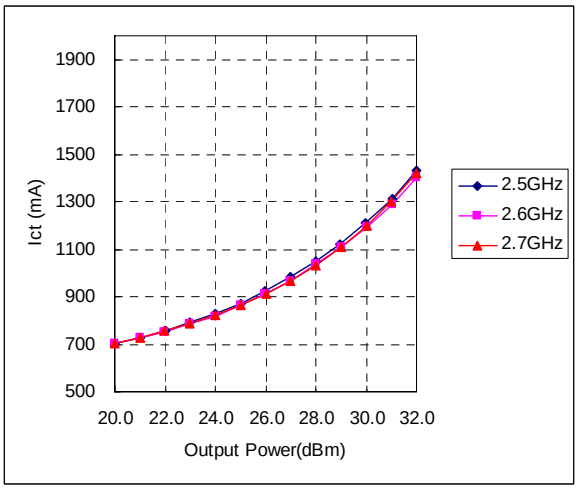
Gain vs. Output Power



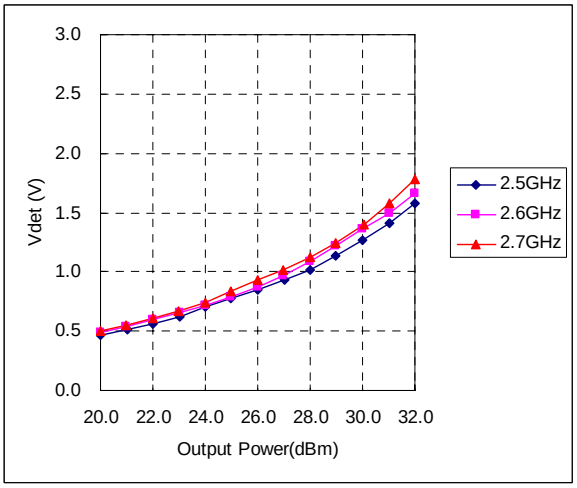
EVM vs. Output Power



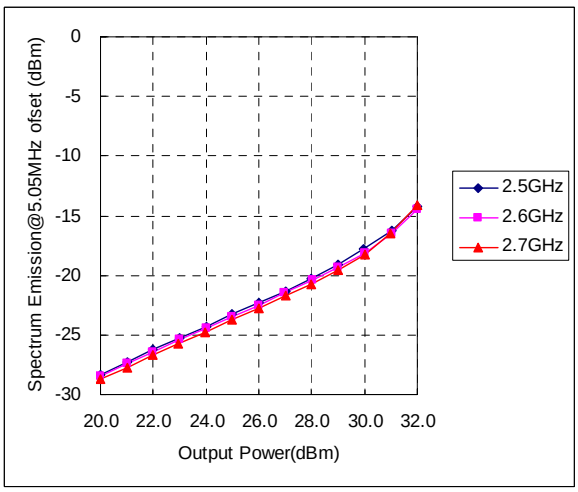
Collector Current vs. Output Power



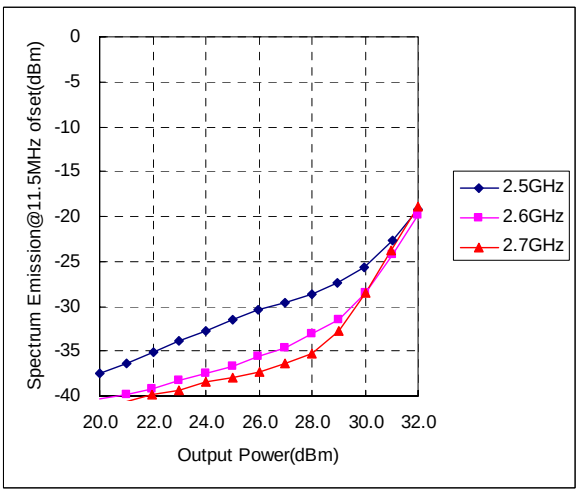
Detector Voltage vs. Output Power



Spectrum Emission Mask

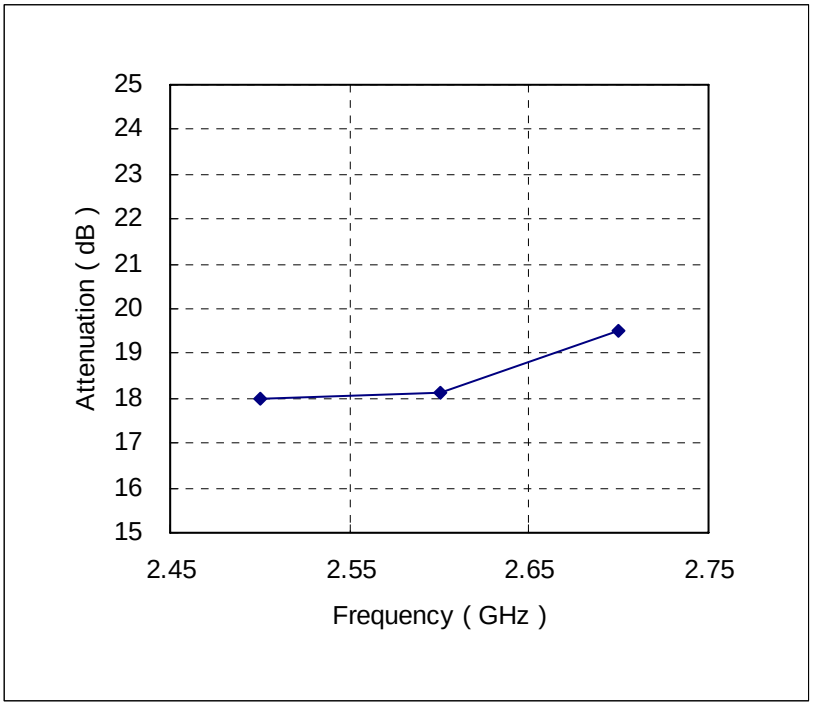


(a)5.05MHz offset

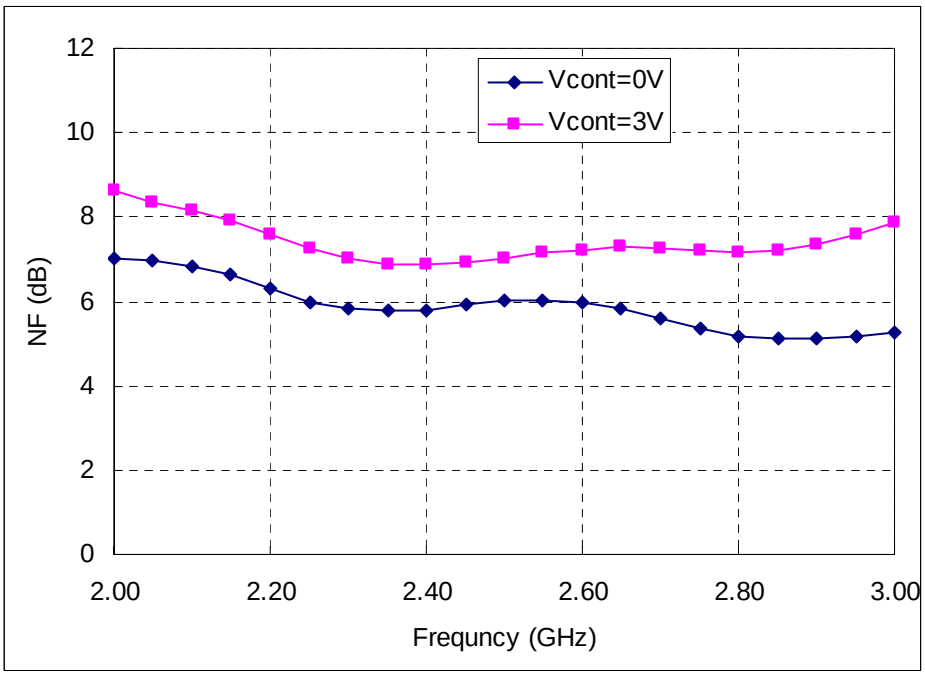


(b)11.5MHz offset

Attenuator Performance

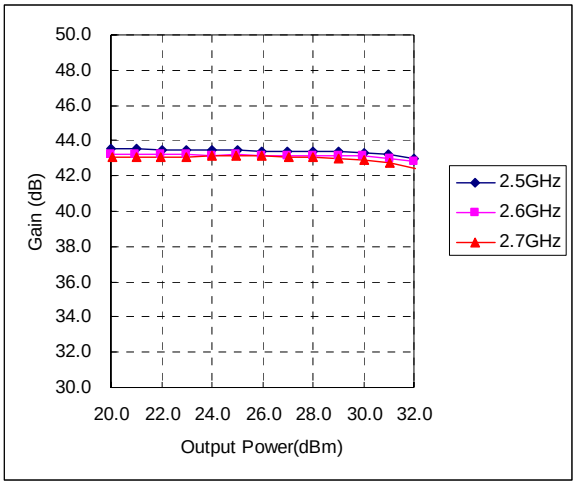


Noise figure

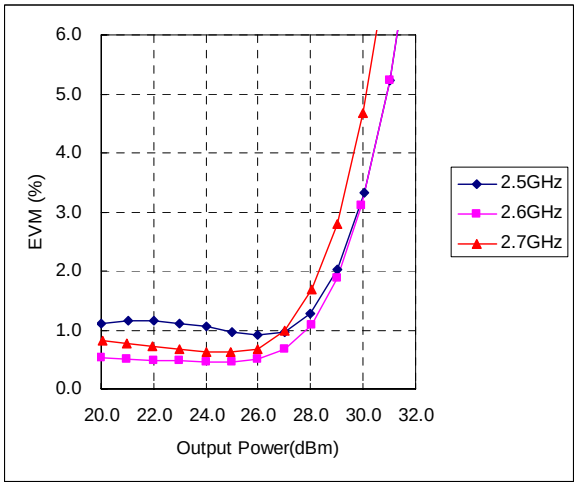


- Vc=5V Ta=25deg.C

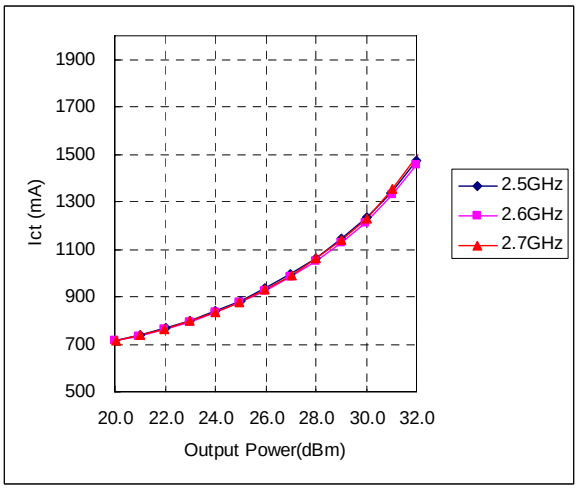
Gain vs. Output Power



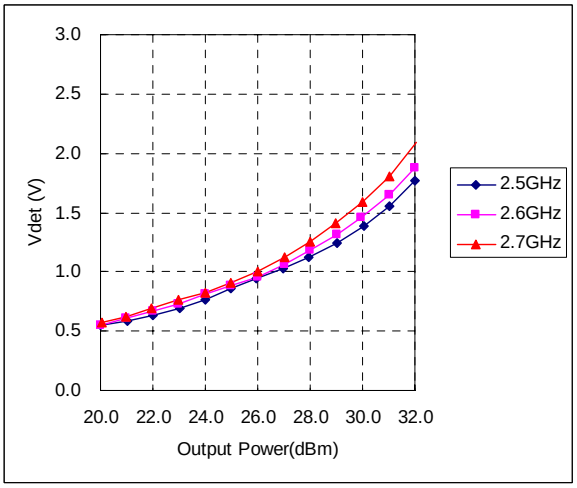
EVM vs. Output Power



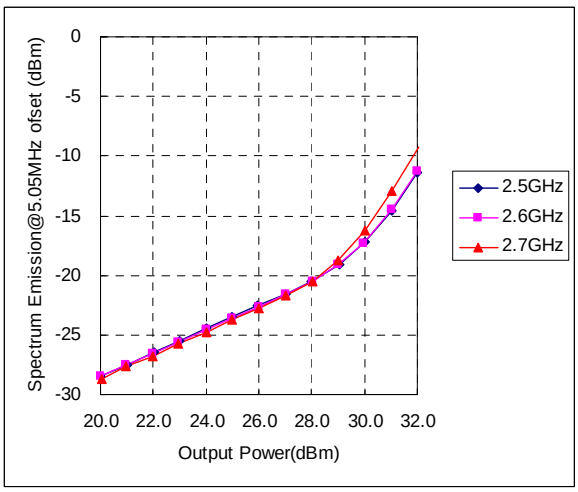
Collector Current vs. Output Power



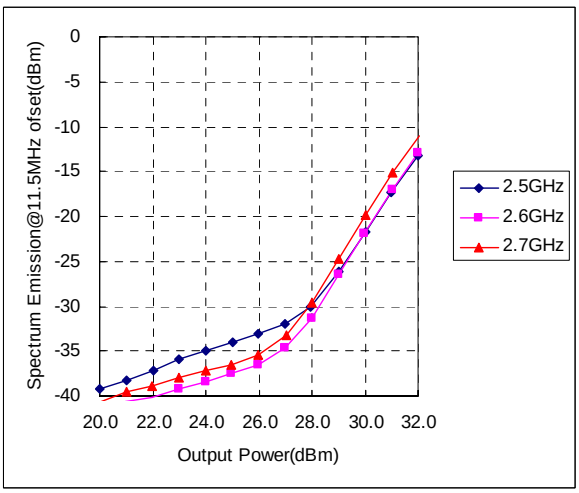
Detector Voltage vs. Output Power



Spectrum Emission Mask

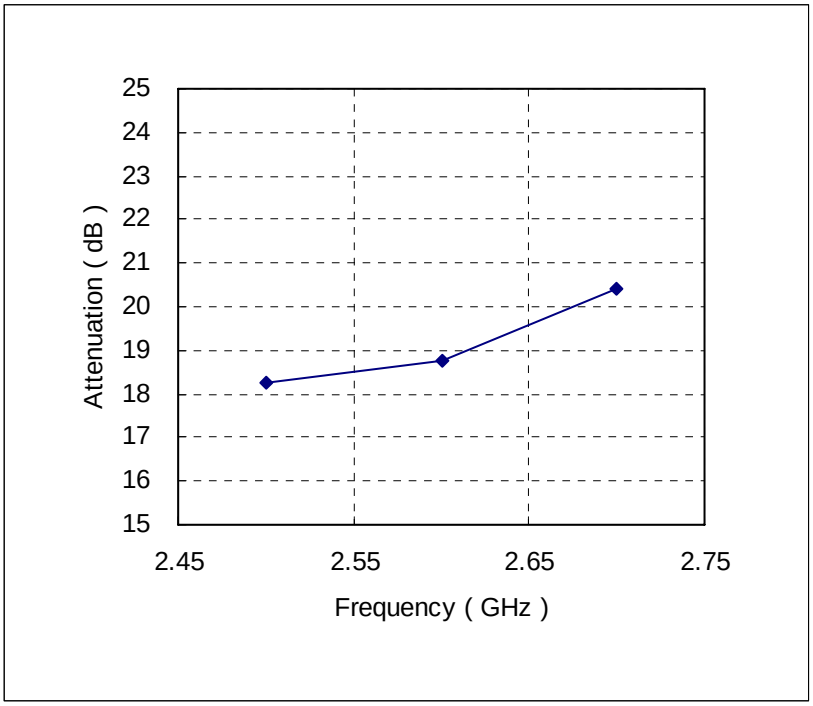


(a)5.05MHz offset

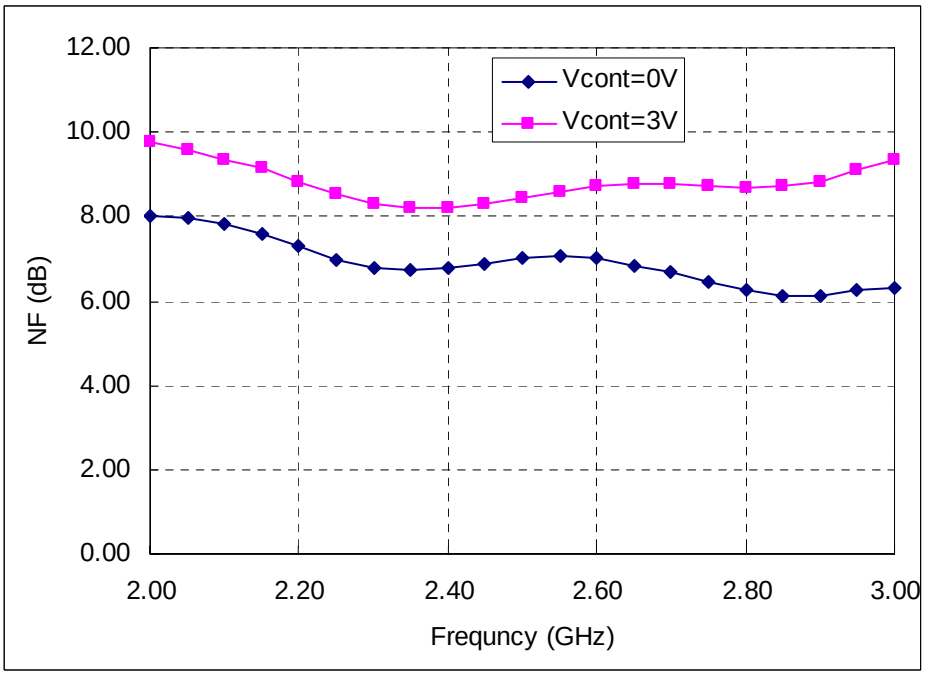


(b)11.5MHz offset

Attenuator Performance

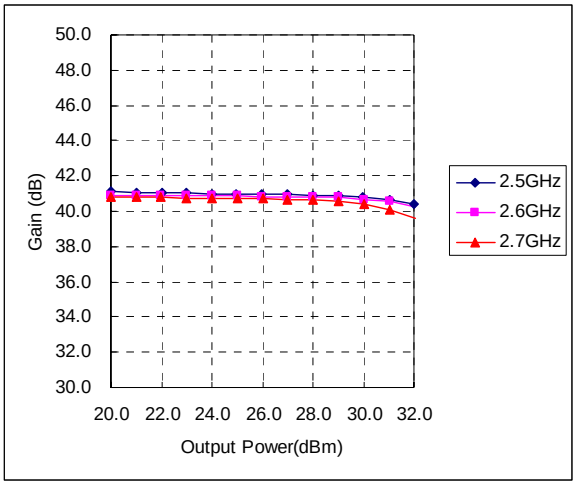


Noise figure

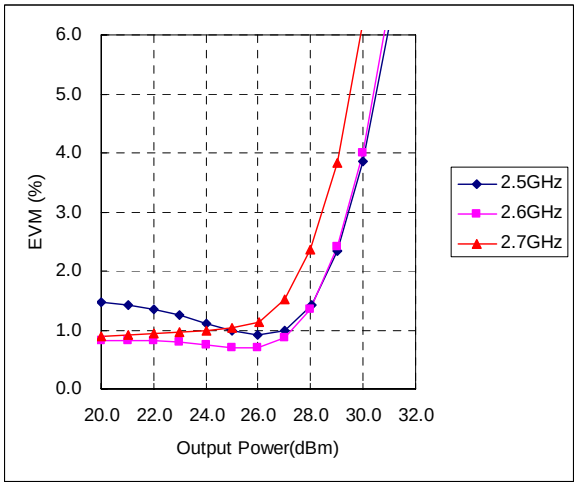


- Vc=5V Ta=85deg.C

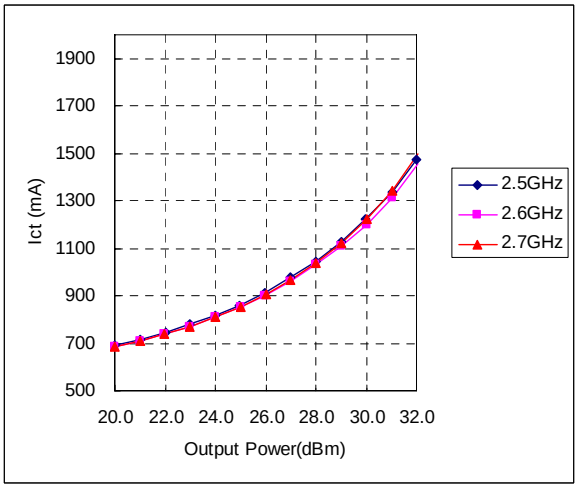
Gain vs. Output Power



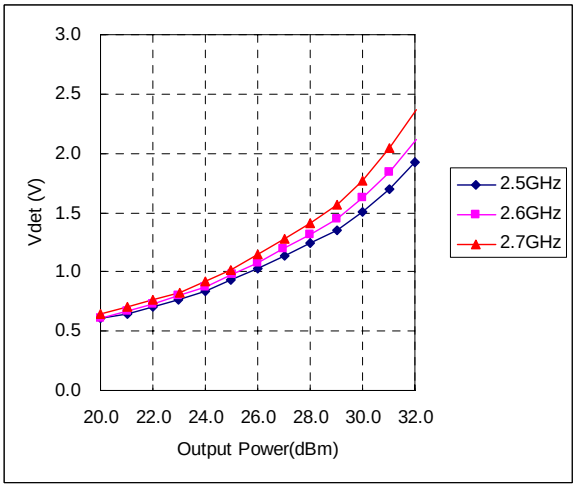
EVM vs. Output Power



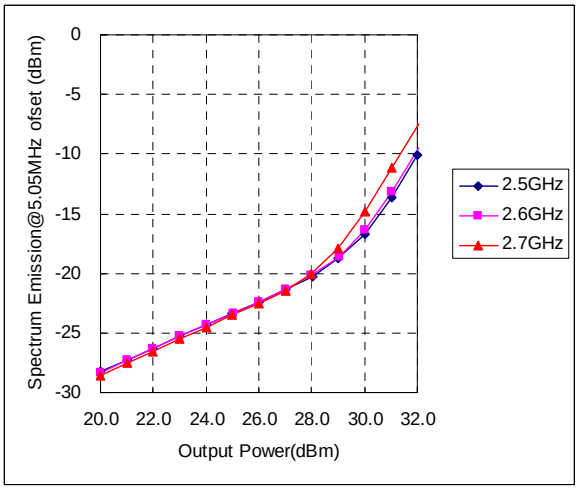
Collector Current vs. Output Power



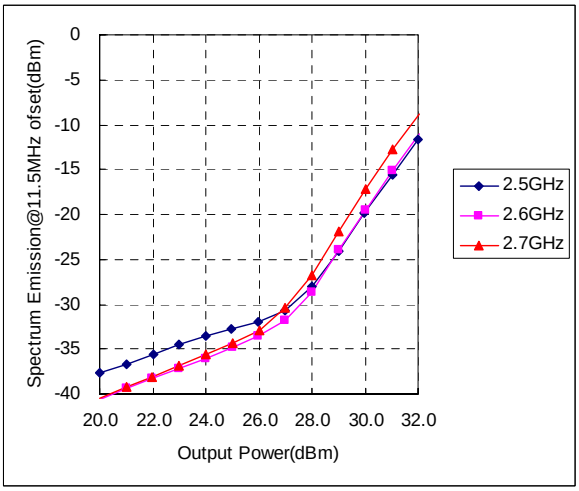
Detector Voltage vs. Output Power



Spectrum Emission Mask

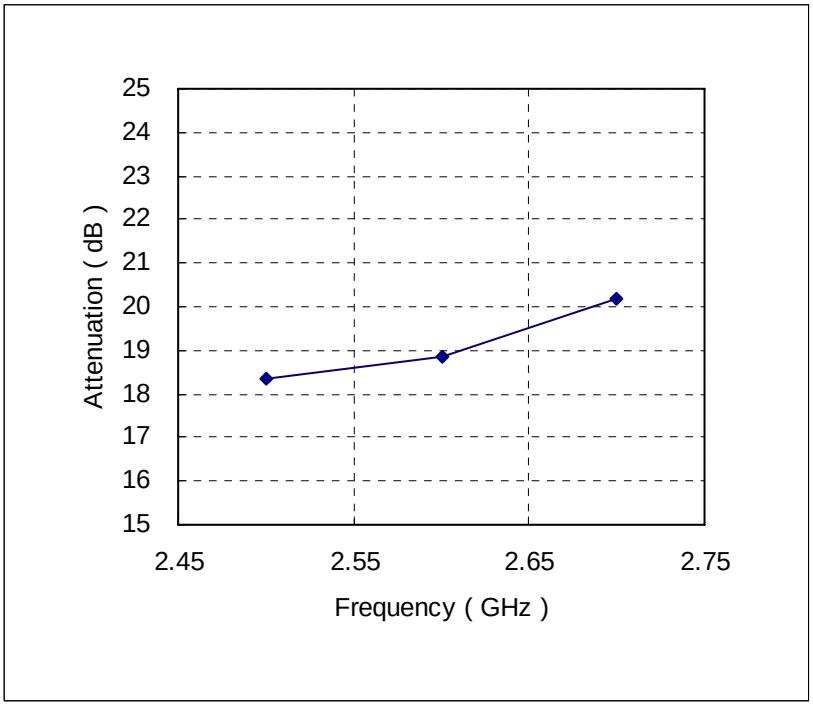


(a)5.05MHz offset

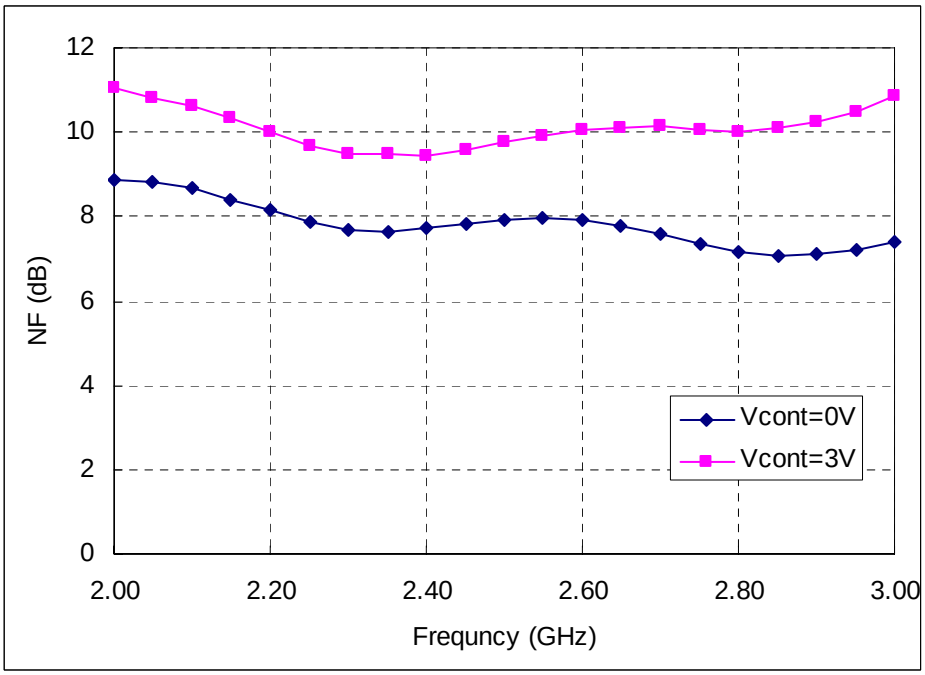


(b)11.5MHz offset

Attenuator Performance

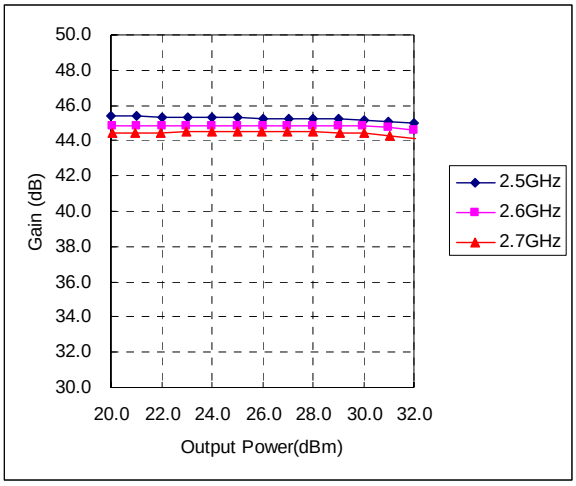


Noise figure

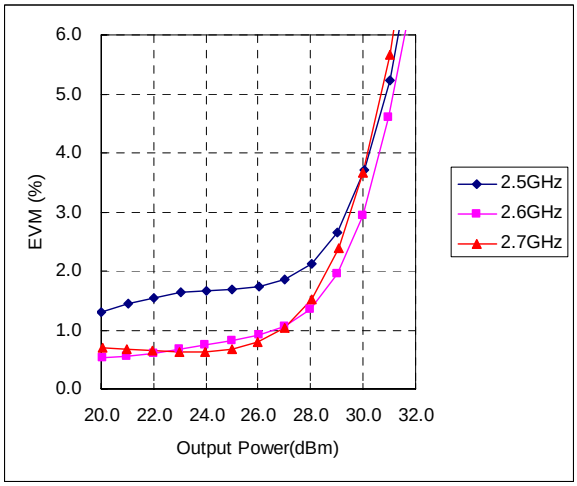


- Vc=5V Ta=-40deg.C

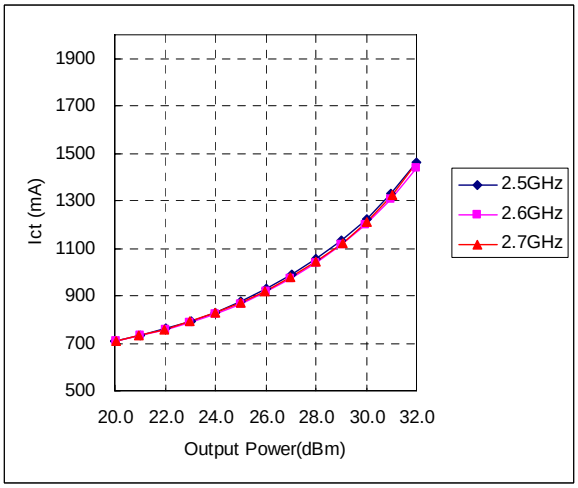
Gain vs. Output Power



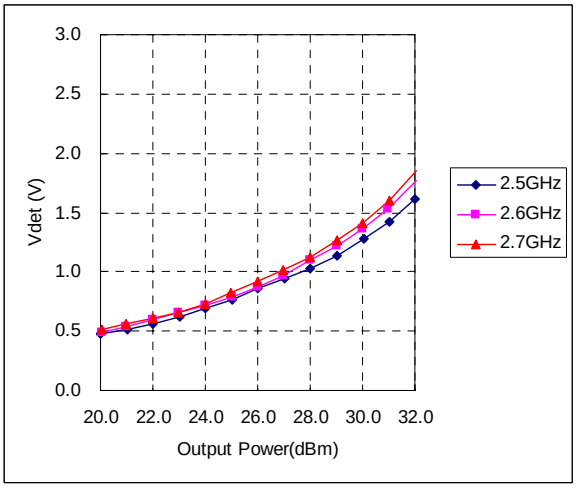
EVM vs. Output Power



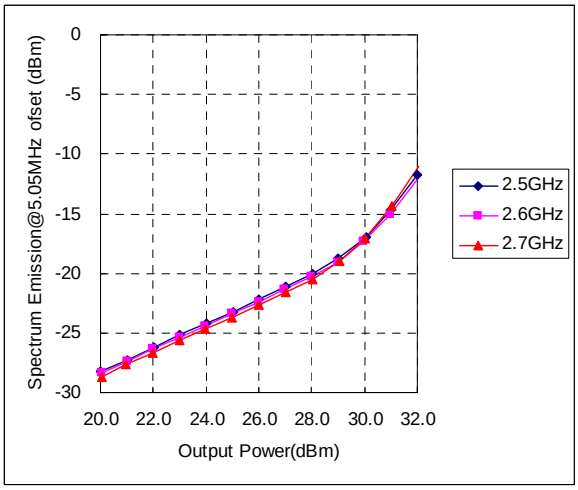
Collector Current vs. Output Power



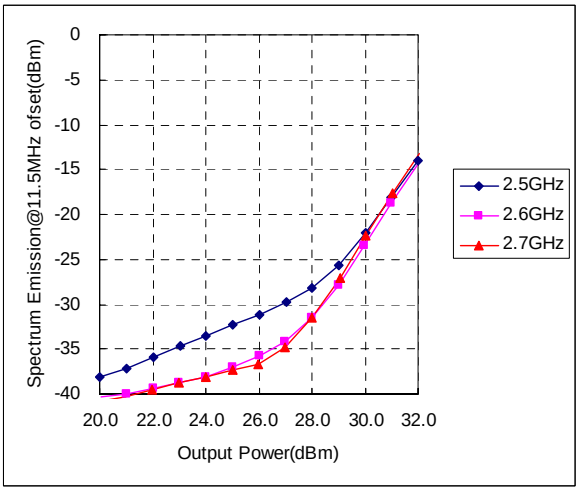
Detector Voltage vs. Output Power



Spectrum Emission Mask

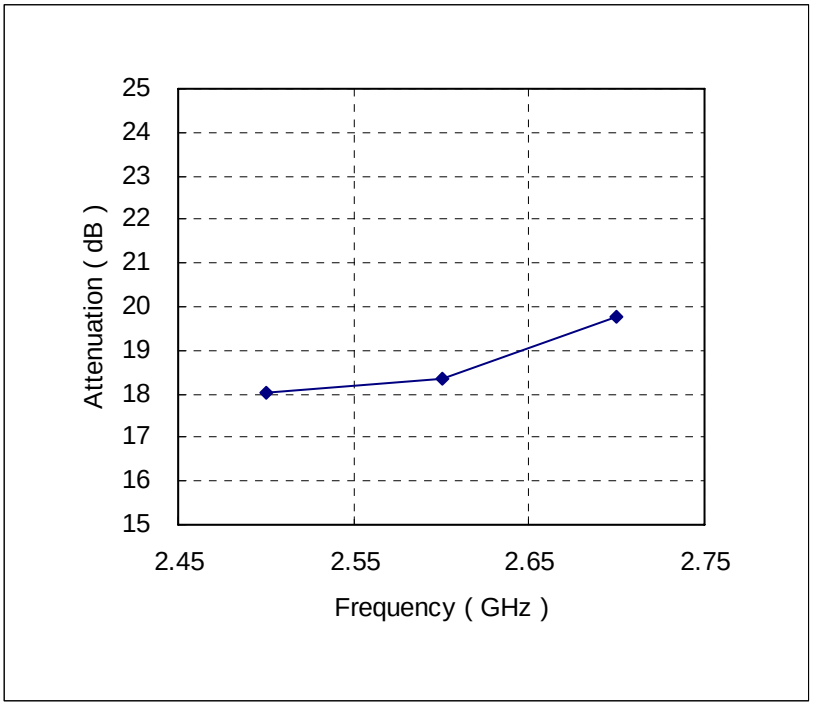


(a)5.05MHz offset

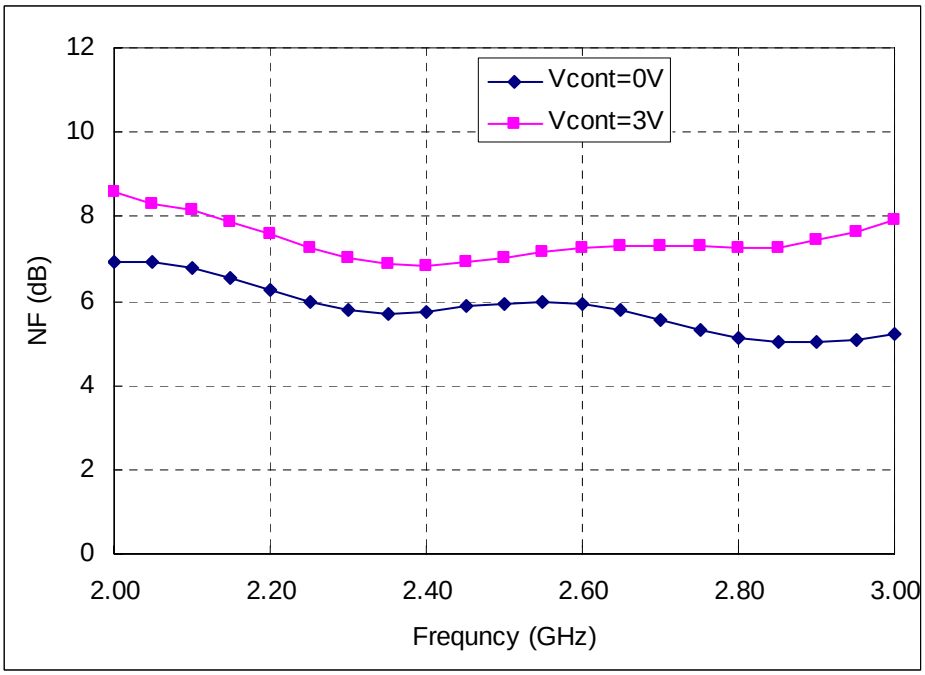


(b)11.5MHz offset

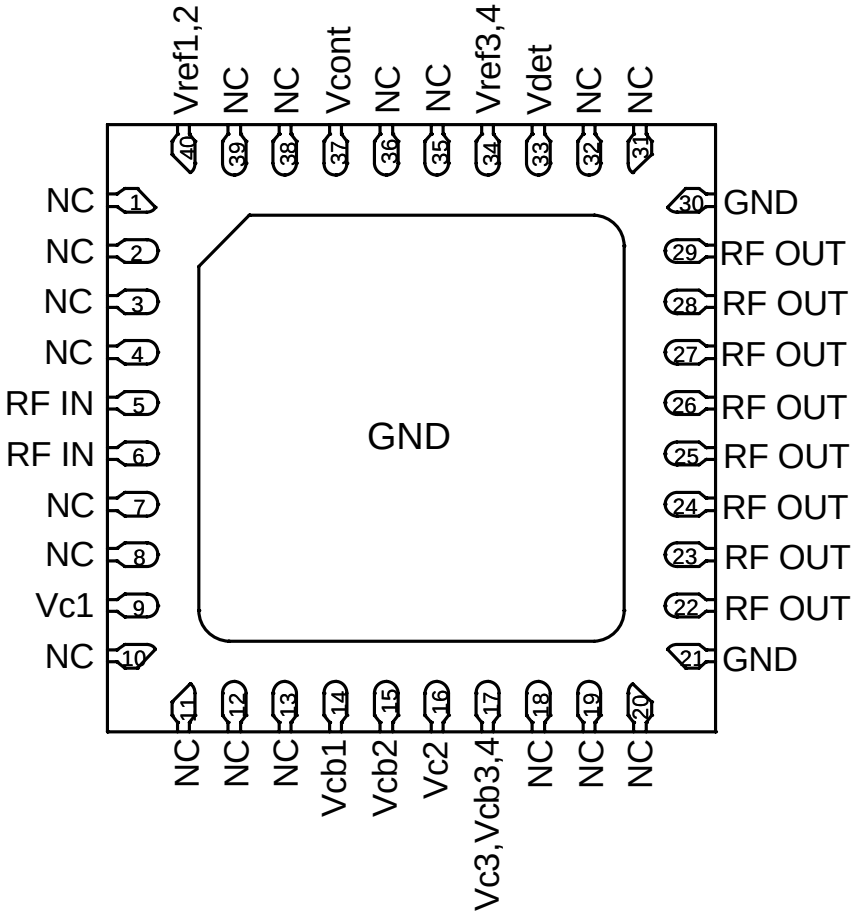
Attenuator Performance



Noise figure



PACKAGE PIN ASSIGN

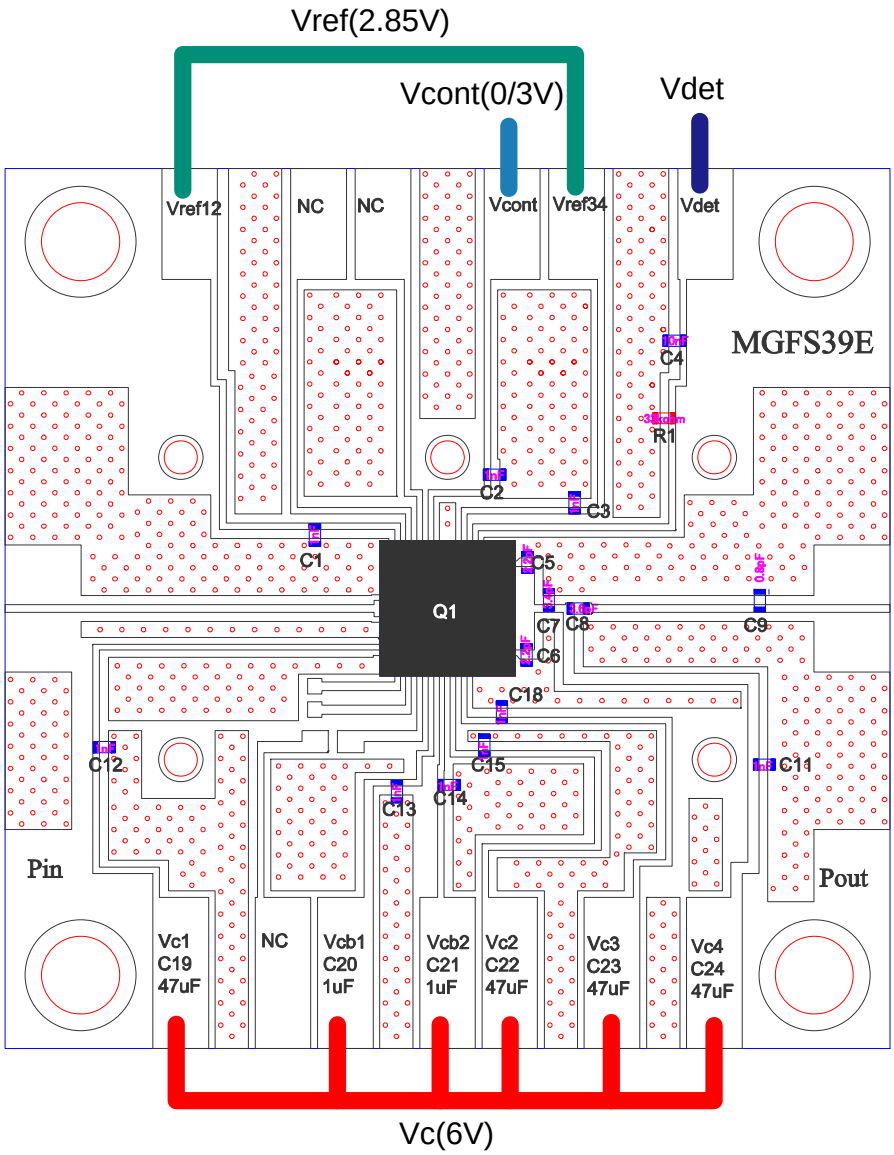


Top View

Mitsubishi Electric Corp. reserves the right to make changes to the product and its related material at any time without notice.

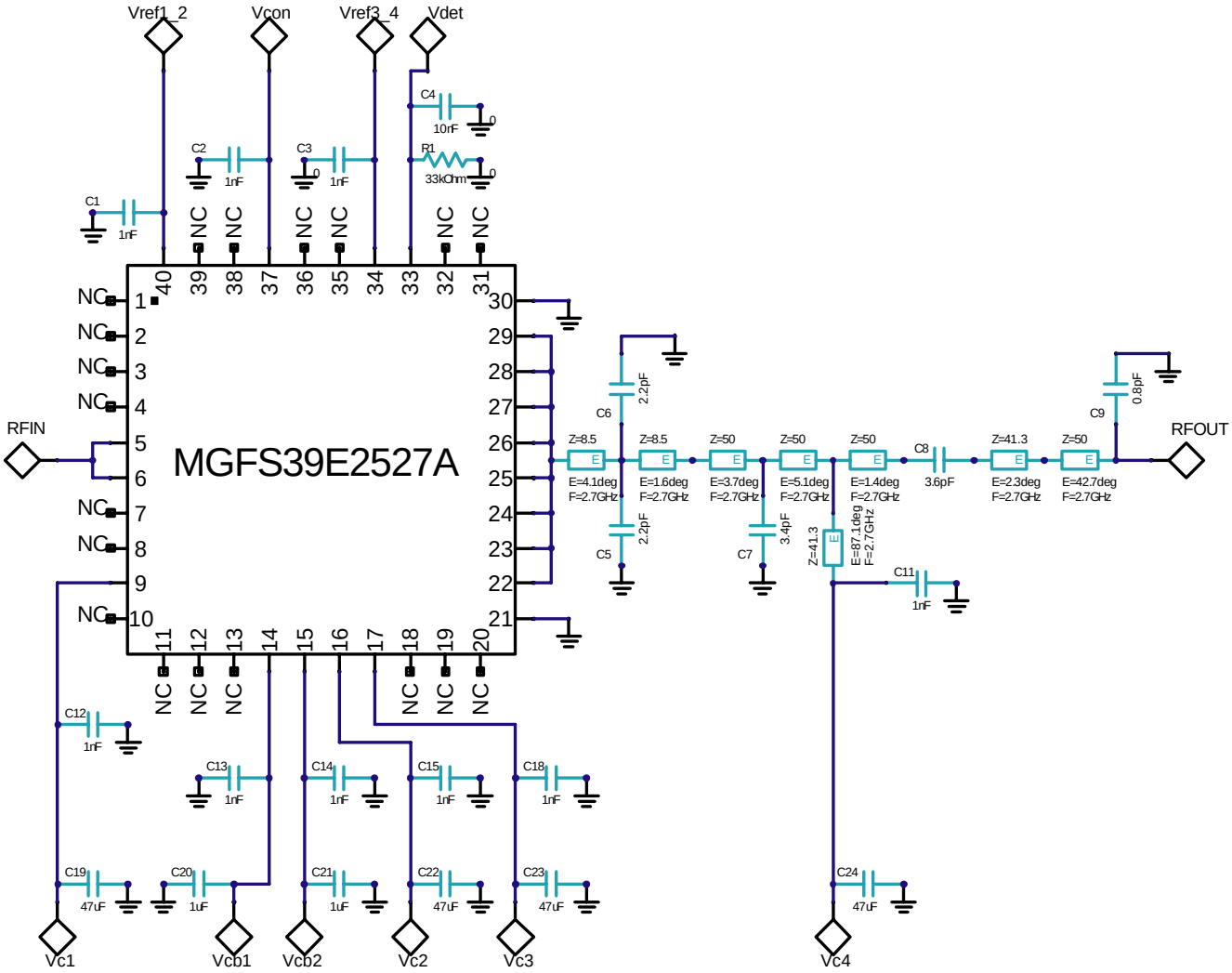
Pin	Function	Description
1,2,3,4,7,8,10, 11,12,13, 18,19,20, 31,32,35,36,38,39	NC	These pins are not wired inside. Both connecting to GND and open is acceptable. It is recommended to connect as shown in the example metal land plan.
21,30	GND	These pins are internally grounded inside the package and it is recommended to ground them.
5,6	RF IN	RF input terminals, internally DC-grounded. Do not apply DC voltage to them
9	Vc1	This is the collector of the 1st stage.(5-6V)
14	Vcb1	This is the supply voltage for 1st stage base bias circuit. (5-6V)
15	Vcb2	This is the supply voltage for 2nd stage base bias circuit. (5-6V)
16	Vc2	This is the collector of the 2nd stage. (5-6V)
17	Vc3	This is the collector of the 3rd stage and the supply voltage for 3rd and 4th stage base bias circuit. (5-6V)
22,23,24,25, 26,27,28,29	RF OUT	These are the RF output pins. These are the collector of the 4th stage.
33	Vdet	This is the output port of the detector sampled at the input of the 4th stage.
34	Vref3,4	This is the reference voltage and power up/down control pin for the 3rd and the 4th stage. The voltage can be applied together with pin 40. DC duty cycle is controlled with pin 34 and 40.(2.85V/0V)
37	Vcon	This is the control voltage for attenuator. (3V/0V)
40	Vref1,2	This is the reference voltage and power up/down control pin for the 1st and 2nd stage. The voltage can be applied together with pin 34. DC duty cycle is controlled with pin 34 and 40. (2.85V/0V)

EXAMPLE LAYOUT OF EVALUATION BOARD (40mmX 40mm, t=0.2mm(RF), Er=4.2,FR-4)



ITEM	DESCRIPTION	NOTE
Q1	MGFS39E2527A	6mmX6mm, QFN
C1, C2, C3, C11, C12, C13, C14, C15, C18	1 nF, 1005	Murata, GRM155B11H102K
C4	10 nF, 1005	Murata, GRM155B11E103K
C5, C6	2.2 pF, 1005	Murata, GJM1553C1H2R2B
C7	3.4 pF, 1005	Murata, GJM1553C1H3R4B
C8	3.6 pF, 1005	Murata, GJM1553C1H3R6B
C9	0.8 pF, 1005	Murata, GJM1554C1HR80B
C19, C22, C23, C24	47 uF, 3216	Murata, GRM32EB31C476K
C20, C21	1 uF, 1608	Murata, GRM188B31E105K
R1	33K, 0603	Taiyosha, RPCO3T333J

APPLICATION CIRCUIT IN EVALUATION BOARD



NOTE:

<Layout>

A properly designed PC board is essential to any RF/microwave circuit. Be sure to use controlled impedance lines on all high-frequency inputs and outputs. A ground plane should be present on both the top and bottom of the PC board and plated-through via holes connecting the top and bottom ground planes should be distributed (See page 6). GND pins and ground paddle of the package should be connected to the bottom ground plane with plated-through via holes close to the package. To improve the heat resistance, place as many plated-through via holes as possible under the ground paddle (See page. 9).

<Output matching circuit>

The output matching circuit is not included in the device so that users can determine the optimum output performance on their boards at the frequencies of interest. Since the circuit dictates the RF characteristics of PA, especially distortion, it should be designed with great care to obtain its maximum ability.

The schematic of the evaluation board is shown above. Capacitors, C5~C10 and C24, and controlled impedance lines are optimized to realize broad-band output matching at frequencies from 2.5 to 2.7GHz.

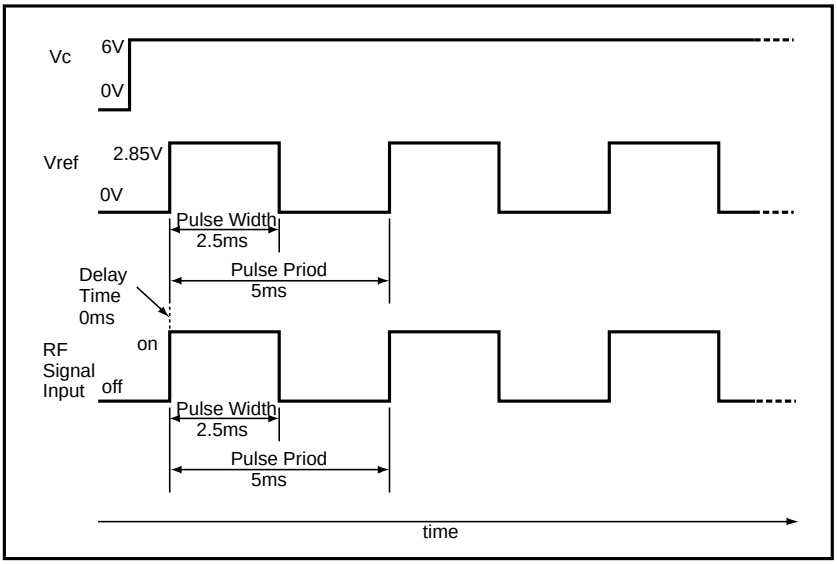
Input and output matching networks are very sensitive to layout-related parasitic effects. Suggested component values may vary according to layout and PC board material.

<Bias circuit>

Since the high-impedance feed line for Vc4 is not included in the device, the line has to be laid out on the PCB. In layout design, please refer to the reference circuit of the feed line which affects the distortion.

Each Vc node on the board should have its own decoupling capacitor to minimize supply coupling from one section of the MMIC to another. A bypass capacitor with low ESR at the RF frequency of operation is located close to the package to reject the RF noise. In addition, a large decoupling capacitor is located on each power supply line to reject low frequency noise.

RECOMMENDED PULSE CONDITION

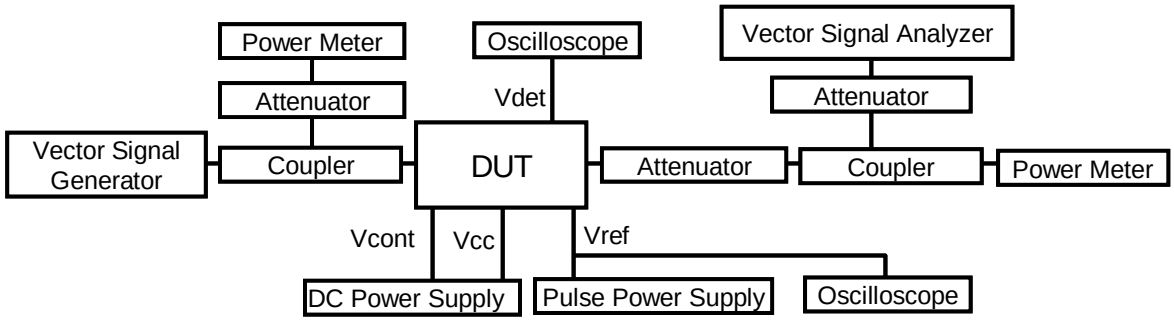


- Pulse Period : 5ms
- Pulse Width : 2.5 ms
- Delay time : 0 ms
- Rise time of Vref pulse : 100ns
- Set up time of quiescent current after Vref turn on : 1 us

- This figure shows the timing chart between Vref and input signal.
- Only while the reference voltage is 2.85V, the device transmits the input signal (*1).
- We usually set the delay time at 0ms in our EVB evaluation because of short set-up time. However set-up time often depends on bypass capacitors of PCB. Therefore, please give appropriate delay time (e.g. about the rise time of Vref) between the rise edge of Vref and that of the input signal .
- We recommended the device operate with less than 50% duty cycle of a 5msec period in order to ensure specified reliability.

*1: In case the device is operated under the Vref conditions of more than 50% duty cycle, self-heating will cause reliability problem, thereby degrading both power gain and EVM performance unexpectedly.

TEST SET-UP



- Calibrate power meters at input/output ports on the EVB.
- Apply DC voltage to Vcc (Vcb1-3, Vcb4, Vc1~Vc4) and Vcont, where pulsed power supply should be applied to Vref for pulsed operation. .
- Monitor DC output voltage from Vdet using an oscilloscope or a multimeter.

<Power up sequence>

GND->Vcc->Vref->Vcont

(1)Apply 6V to Vcc, where stepping up from 0 to 6V is preferable.

(2)Supply pulsed voltage between 0 and 2.85V for Vref.
Please check the voltage level of Vref close to EVB and the timing chart between Vref and input signal using an oscilloscope. Also please do not apply supply voltage exceeding 3V(absolute maximum rating) to the Vref terminal.

(3)Supply Vcont with 3V for the attenuation mode. In the thru-mode, apply 0V to Vcont or keep it open.

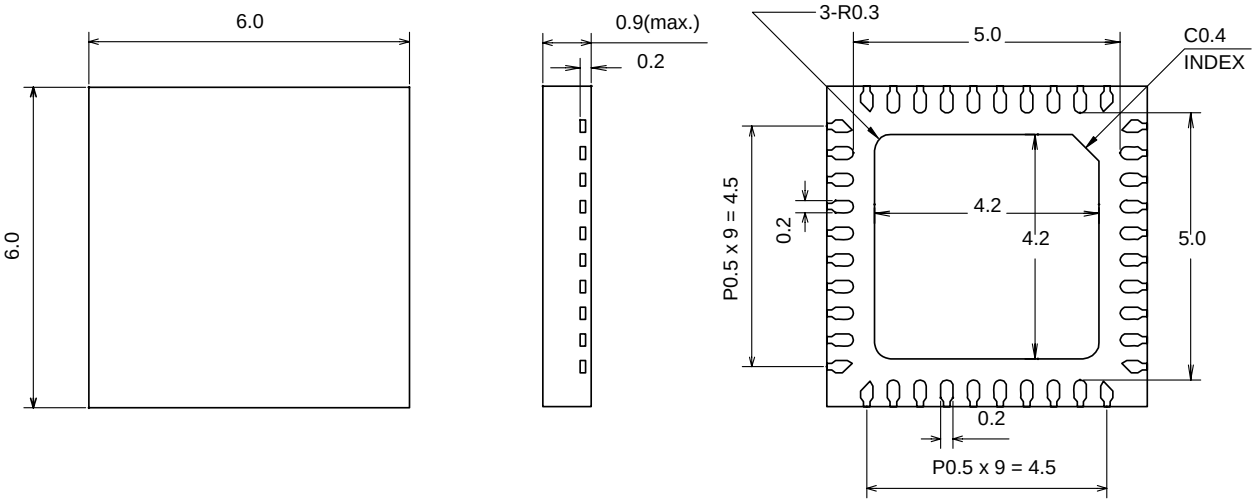
<Power off sequence>

Vcont->Vref->Vcc->GND

The reverse procedure is recommended for bias off.

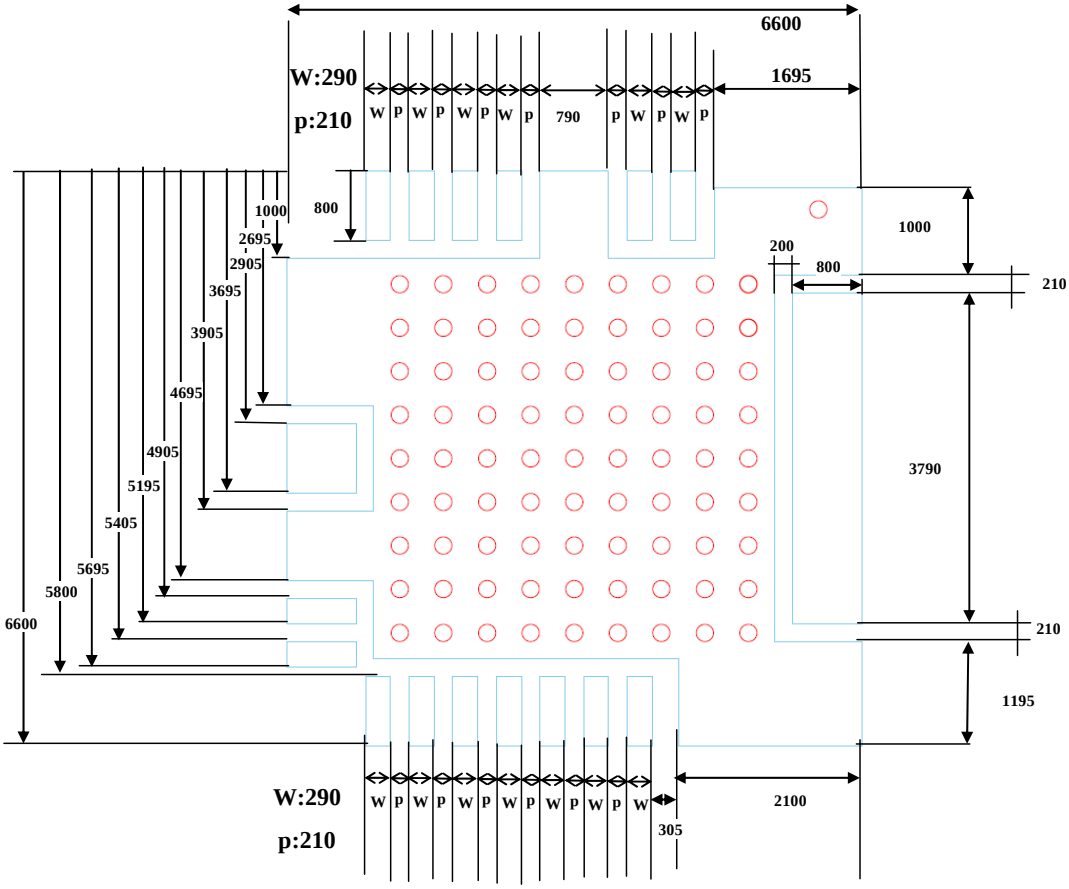
PACKAGE DRAWING DIMENSIONS

All Dimensions are in mm. General tolerance is ±0.1mm.



Top View Side View Bottom View

EXAMPLE METAL LAND PATTERN



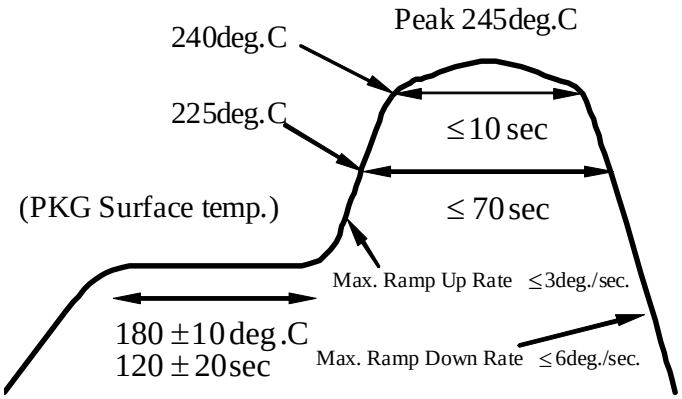
Note:
UNIT : um
Through holes with 200um diameter should be put with a distance of 500um among them.
It is recommended that they have metallization of 25um thick on the inside wall.

HANDLING PRECAUTION

1) Work desk, test equipment, soldering iron and worker should be grounded before mounting and testing. Please note that electric discharge of GaAs HBT is much more sensitive than that of Si transistor. Handling without ground possibly damages GaAs HBT.

2) The surface of a board on which this product is mounted should be as flat and clean as possible to prevent a substrate from cracking by bending this product.

3) Recommended IR reflow soldering condition is shown as follows. (Max. two times)



4) Handling precaution at high temperature
In case of heating this product, please keep the same heat profile as recommended reflow one.
Please note that crack, flaw or modification may be generated if epoxy resin part is handled with tweezers and etc. at high temperature.

5) Cleaning condition
Please select after confirming administrative guidance, legal restrictions, and the mass of the residual ion contaminant etc., and use it.

6) After soldering, please remove the flux. Please take care that solvent does not penetrate into this product.

7) GaAs HBT contains As(Arsenic). This product should be dumped as particular industrial waste.