

MARVELL 88E6161 ETHERNET SWITCHES

Ref : 004773A

Duration : 3 days

OBJECTIVES

- Providing the basic knowledge on 802.3 and 802.1
- Understanding the parameters that determine the QoS
- Implementing the Dynamic Queue Limit architecture
- Description of the Address Lookup engine
- Implementing the Distributed Switch Architecture
- Becoming familiar with the API defined by Marvell

PREREQUISITES

- Knowledge of Ethernet (802.3) and Bridging (802.1) is recommended (Course 003367A)
- Knowledge of Precise Time Protocol (IEEE1588) is recommended (Course 004701A)

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Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

100 Mbps ETHERNET BASICS

- MAC layer, frame format, frame filtering
- Full duplex Ethernet vs CSMA/CD
- PHY layer, scrambling, 4b/5b coding, NRZI
- Auto-negotiation, utilization of FLPs
- MII

1 Gbps ETHERNET BASICS

- 1000BASE-T
- 1000BASE-X
- GMII transfer protocol, RGMII, SGMII

802.1Q BASICS

- Spanning tree algorithm, RSTP, MSTP
- VLAN tag, selecting one tree and selecting the priority of a frame
- Port states
- Automatic address learning
- Automatic address aging
- Handling multicasts, GVRP, IGMP snooping

INTRODUCTION TO 88E6161 SWITCHES

- Block diagram, ports 0-3 features
- Port 4 and port 5 operating modes
- Pin strapping
- Application examples

BASIC SWITCH FUNCTIONS

- MACs
- PPU
- RMON registers
- Basic switch operation
- 802.1X source address authentication
- Multiple FIDs in VLAN systems

NORMAL PORTS

- Ingress policy
- VLANs
- Special frame handling
- QOS qualification
- Port-based Ingress Rate Limiting
- Queue Controller
- Egress policy

PROVIDER PORTS

- Distinguishing S-TAG from C-TAG
- Customer-to-Provider traffic
- Provider-to-Customer traffic

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DSA PORTS

- Implementing control traffic between switches and management CPU
- Forward DSA tag
- TO_CPU DSA tag
- FROM_CPU DSA tag
- Interconnecting switches by using cross-chip links
- Switch handling of DSA frames
- Secure Control Technology

ADVANCED SWITCH FUNCTIONS

- Spanning Tree support
- Ingress MGMT/BPDU frame detection
- Proper connection to a management CPU and to a router
- Port mirroring
- Port trunking support
- PTP implementation

ACCESSING SWITCH REGISTERS

- The 16 register groups
- Multi-chip addressing mode
- Single-chip direct access to registers
- Remote Management frames

PHY LAYER

- Transmit PCS and PMA
- Receive PCS and PMA
- Power management
- Far End Fault indication
- Auto MDI/MDIX crossover
- LED interface
- Accessing PHY registers, MDC/MDIO interface
- Auto-configuration

SOFTWARE ARCHITECTURE

- DSDT suite
- Multi-layer architecture
- OS independency
- Source code organization
- Platform specific routines
- SMI interface functions
- Switch driver layer
- API layer
- Interrupts

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATION

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