LMV831 Single/ LMV832 Dual/ LMV834 Quad 3.3 MHz Low Power CMOS, EMI Hardened Operational Amplifiers

Check for Samples: LMV831, LMV832, LMV834

FEATURES

- **Unless Otherwise Noted, Typical Values at T_A= 25°C, V^+ = 3.3V**
- **Supply Voltage 2.7V to 5.5V**
- **Supply Current (per Channel) 240 µA**
- **Input Offset Voltage 1 mV Max**
- **Input Bias Current 0.1 pA**
- **GBW 3.3 MHz**
- **EMIRR at 1.8 GHz 120 dB**
- **Input Noise Voltage at 1 kHz 12 nV/$\sqrt{Hz}$**
- **Slew Rate 2 V/µs**
- **Output Voltage Swing Rail-to-Rail**
- **Output Current Drive 30 mA**
- **Operating Ambient Temperature Range −40°C to 125°C**

APPLICATIONS

- **Photodiode Preamp**
- **Piezoelectric Sensors**
- **Portable/Battery-Powered Electronic Equipment**
- **Filters/Buffers**
- **PDAs/Phone Accessories**

DESCRIPTION

TI's LMV831, LMV832, and LMV834 are CMOS input, low power op amp IC's, providing a low input bias current, a wide temperature range of −40°C to 125°C and exceptional performance making them robust general purpose parts. Additionally, the LMV831/LMV832/LMV834 are EMI hardened to minimize any interference so they are ideal for EMI sensitive applications.

The unity gain stable LMV831/LMV832/LMV834 feature 3.3 MHz of bandwidth while consuming only 0.24 mA of current per channel. These parts also maintain stability for capacitive loads as large as 200 pF. The LMV831/LMV832/LMV834 provide superior performance and economy in terms of power and space usage.

This family of parts has a maximum input offset voltage of 1 mV, a rail-to-rail output stage and an input common-mode voltage range that includes ground. Over an operating range from 2.7V to 5.5V the LMV831/LMV832/LMV834 provide a PSRR of 93 dB, and a CMRR of 91 dB. The LMV831 is offered in the space saving 5-Pin SC70 package, the LMV832 in the 8-Pin VSSOP and the LMV834 is offered in the 14-Pin TSSOP package.

Typical Application

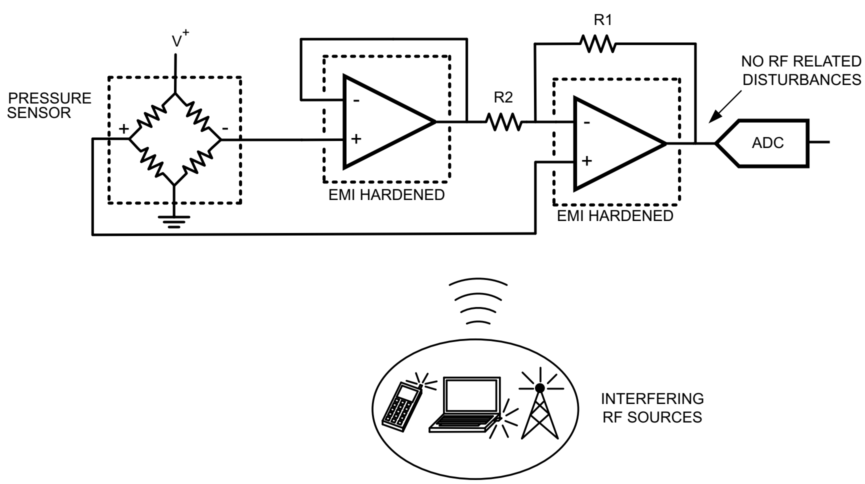

Figure 1. EMI Hardened Sensor Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2 kV
	Charge-Device Model	1 kV
	Machine Model	200V
V_{IN} Differential		± Supply Voltage
Supply Voltage ($V_S = V^+ – V^−$)		6V
Voltage at Input/Output Pins		V^++0.4V, $V^−$ −0.4V
Storage Temperature Range		−65°C to 150°C
Junction Temperature (4)		150°C
Soldering Information	Infrared or Convection (20 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range (2)		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^−$)		2.7V to 5.5V
Package Thermal Resistance ($θ_{JA}$ (2))	5-Pin SC70	302°C/W
	8-Pin VSSOP	217°C/W
	14-Pin TSSOP	135°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.3V Electrical Characteristics (1)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3V, $V^−$ = 0V, $V_{CM} = V^+/2$, and R_L =10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage (4)				±0.25	±1.00 **±1.23**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift (4)(5)		LMV831, LMV832		±0.5	±1.5	μV/°C
			LMV834		±0.5	±1.7	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is specified by design and/or characterization and is not tested in production.

3.3V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
I_B	Input Bias Current(5)				0.1	10 **500**	pA
I_{OS}	Input Offset Current				1		pA
CMRR	Common-Mode Rejection Ratio(4)	0.2V ≤ V_{CM} ≤ V^+ - 1.2V		76 **75**	91		dB
PSRR	Power Supply Rejection Ratio(4)	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V		76 **75**	93		dB
EMIRR	EMI Rejection Ratio, IN+ and IN-(6)	V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 400 MHz			80		dB
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 900 MHz			90		
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 1800 MHz			110		
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 2400 MHz			120		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB		−0.1		2.1	V
A_{VOL}	Large Signal Voltage Gain(7)	R_L = 2 kΩ, V_{OUT} = 0.15V to 1.65V, V_{OUT} = 3.15V to 1.65V	LMV831, LMV832	102 **102**	121		dB
			LMV834	102 **102**	121		
		R_L = 10 kΩ, V_{OUT} = 0.1V to 1.65V, V_{OUT} = 3.2V to 1.65V	LMV831, LMV832	104 **104**	126		
			LMV834	104 **103**	123		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2	LMV831, LMV832		29	36 **43**	mV from either rail
			LMV834		31	38 **44**	
		R_L = 10 kΩ to V^+/2	LMV831, LMV832		6	8 **9**	
			LMV834		7	9 **10**	
	Output Voltage Swing Low	R = 2 kΩ to V^+/2			25	34 **43**	
		R_L = 10 kΩ to V^+/2			5	8 **10**	
I_{OUT}	Output Short Circuit Current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	LMV831, LMV832	27 **22**	28		mA
			LMV834	24 **19**	28		
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV		27 **21**	32		
I_S	Supply Current		LMV831		0.24	0.27 **0.30**	mA
			LMV832		0.46	0.51 **0.58**	
			LMV834		0.90	1.00 **1.16**	
SR	Slew Rate(8)	A_V = +1, V_{OUT} = 1 V_{PP}, 10% to 90%			2		V/µs

(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.
(8) Number specified is the slower of positive and negative slew rates.

3.3V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
GBW	Gain Bandwidth Product			3.3		MHz
Φ_m	Phase Margin			65		deg
e_n	Input Referred Voltage Noise Density	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.005		pA/√Hz
R_{OUT}	Closed Loop Output Impedance	f = 2 MHz		500		Ω
C_{IN}	Common-mode Input Capacitance			15		pF
	Differential-mode Input Capacitance			20		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz		0.02		%

5V Electrical Characteristics(1)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L = 10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage(4)				±0.25	±1.00 **±1.23**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift(4)(5)		LMV831, LMV832		±0.5	±1.5	µV/°C
			LMV834		±0.5	±1.7	
I_B	Input Bias Current(5)				0.1	10 **500**	pA
I_{OS}	Input Offset Current				1		pA
CMRR	Common-Mode Rejection Ratio(4)	0V ≤ V_{CM} ≤ V^+ −1.2V		77 **77**	93		dB
PSRR	Power Supply Rejection Ratio(4)	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V		76 **75**	93		dB
EMIRR	EMI Rejection Ratio, IN+ and IN-(6)	V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 400 MHz			80		dB
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 900 MHz			90		
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 1800 MHz			110		
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 2400 MHz			120		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB		–0.1		3.8	V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).

5V Electrical Characteristics(1) (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, and R_L = 10 kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
A_{VOL}	Large Signal Voltage Gain(7)	R_L = 2 kΩ, V_{OUT} = 0.15V to 2.5V, V_{OUT} = 4.85V to 2.5V	LMV831, LMV832	107 **106**	127		dB
			LMV834	104 **104**	127		
		R_L = 10 kΩ, V_{OUT} = 0.1V to 2.5V, V_{OUT} = 4.9V to 2.5V	LMV831, LMV832	107 **107**	130		
			LMV834	105 **104**	127		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$	LMV831, LMV832		32	42 **49**	mV from either rail
			LMV834		35	45 **52**	
		R_L = 10 kΩ to $V^+/2$	LMV831, LMV832		6	9 **10**	
			LMV834		7	10 **11**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$			27	43 **52**	
		R_L = 10 kΩ to $V^+/2$			6	10 **12**	
I_{OUT}	Output Short Circuit Current	Sourcing V_{OUT} = V_{CM} V_{IN} = 100 mV	LMV831, LMV832	59 **49**	66		mA
			LMV834	57 45	63		
		Sinking V_{OUT} = V_{CM} V_{IN} = −100 mV	LMV831, LMV832	50 **41**	64		
			LMV834	53 41	63		
I_S	Supply Current		LMV831		0.25	0.27 **0.31**	mA
			LMV832		0.47	0.52 **0.60**	
			LMV834		0.92	1.02 **1.18**	
SR	Slew Rate(8)	A_V = +1, V_{OUT} = $2V_{PP}$, 10% to 90%			2		V/µs
GBW	Gain Bandwidth Product				3.3		MHz
Φ_m	Phase Margin				65		deg
e_n	Input Referred Voltage Noise	f = 1 kHz			12		nV/√Hz
		f = 10 kHz			10		
i_n	Input Referred Current Noise	f = 1 kHz			0.005		pA/√Hz
R_{OUT}	Closed Loop Output Impedance	f = 2 MHz			500		Ω
C_{IN}	Common-mode Input Capacitance				14		pF
	Differential-mode Input Capacitance				20		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz			0.02		%

(7) The specified limits represent the lower of the measured values for each output range condition.
(8) Number specified is the slower of positive and negative slew rates.

Connection Diagram

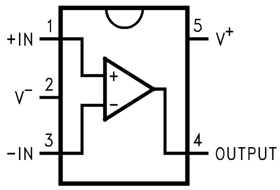

Figure 2. 5-Pin SC70 Top View

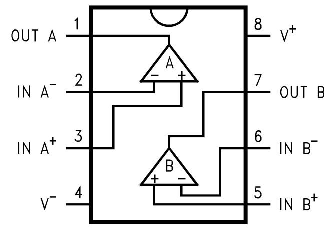

Figure 3. 8-Pin VSSOP Top View

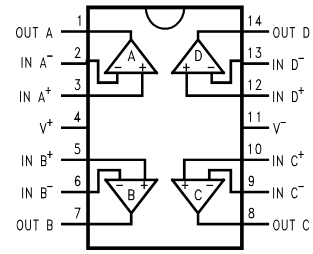

Figure 4. 14-Pin TSSOP Top View

Typical Performance Characteristics

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

V_{OS} vs. V_{CM} at V^+ = 3.3V

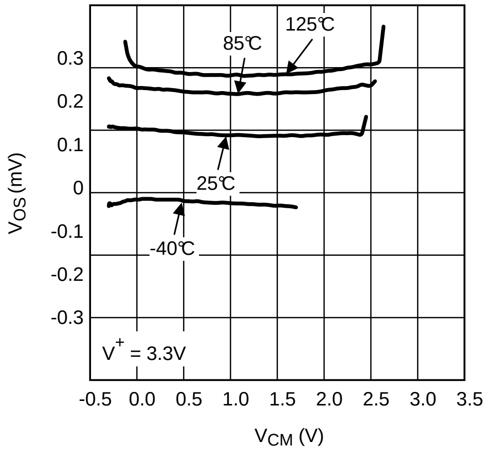

Figure 5.

V_{OS} vs. V_{CM} at V^+ = 5.0V

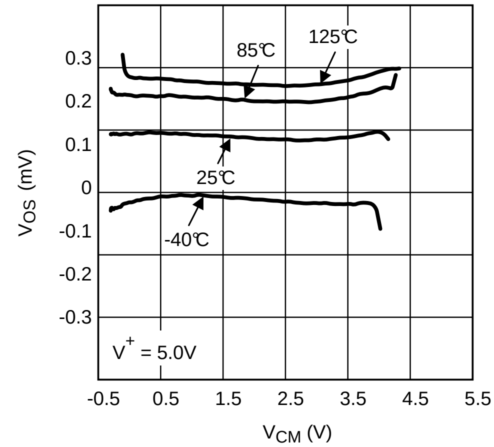

Figure 6.

V_{OS} vs. Supply Voltage

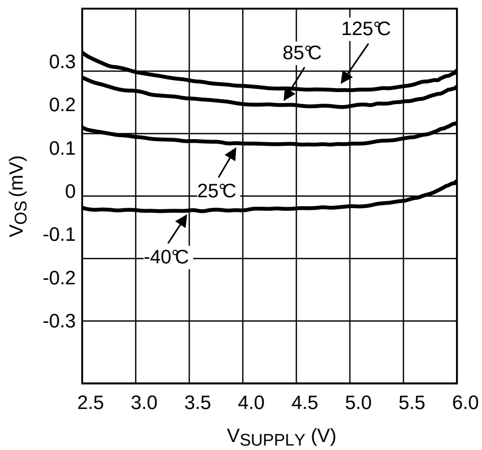

Figure 7.

V_{OS} vs. Temperature

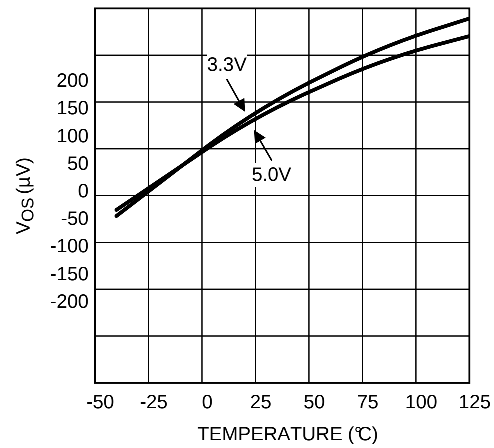

Figure 8.

V_{OS} vs. V_{OUT}

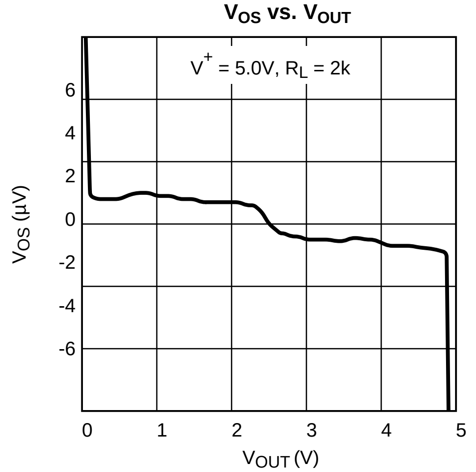

Figure 9.

Input Bias Current vs. V_{CM} at 25°C

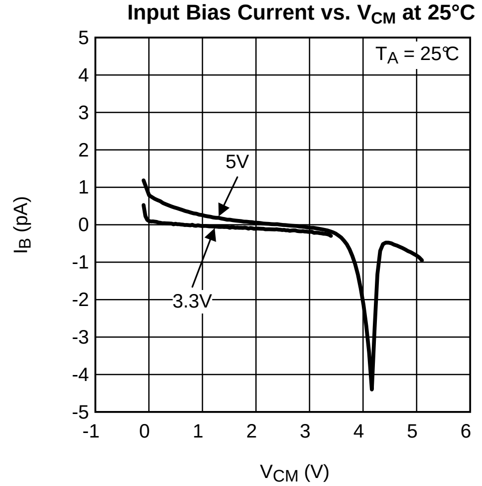

Figure 10.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

Input Bias Current vs. V_{CM} at 85°C

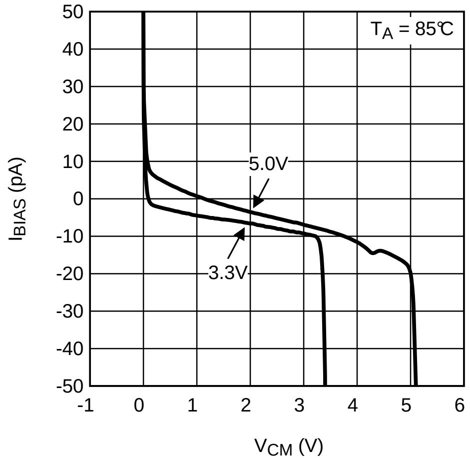

Figure 11.

Input Bias Current vs. V_{CM} at 125°C

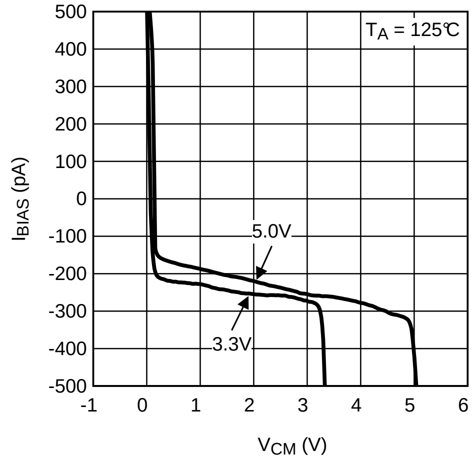

Figure 12.

Supply Current vs. Supply Voltage Single LMV831

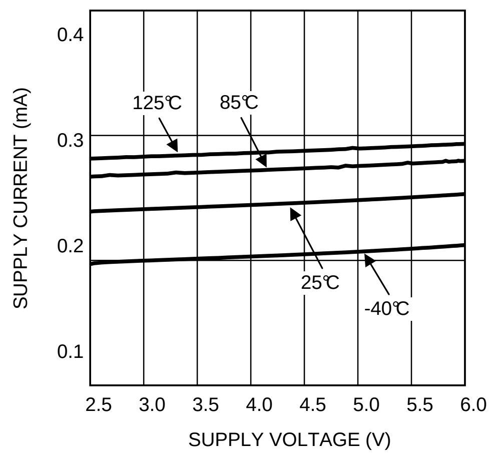

Figure 13.

Supply Current vs. Supply Voltage Dual LMV832

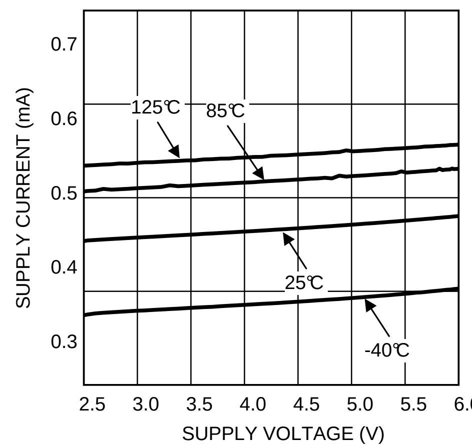

Figure 14.

Supply Current vs. Supply Voltage Quad LMV834

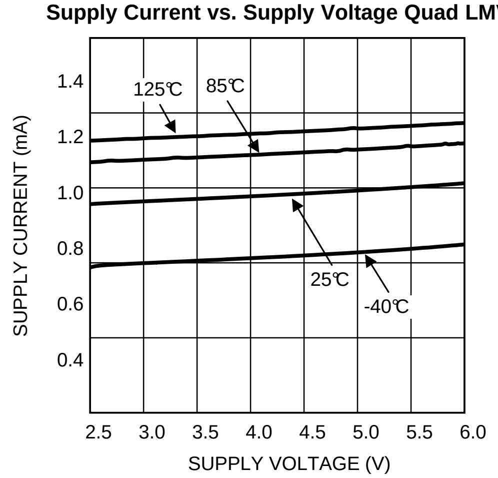

Figure 15.

Supply Current vs. Temperature Single LMV831

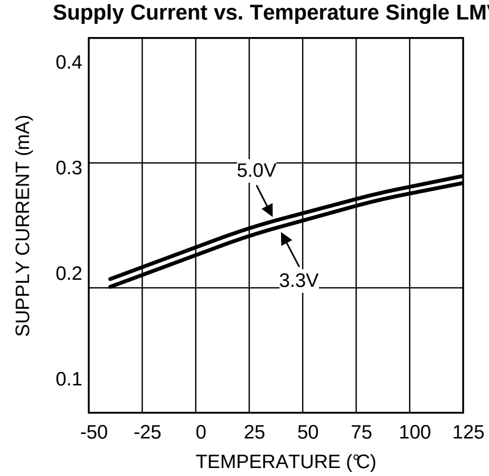

Figure 16.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

Supply Current vs. Temperature Dual LMV832

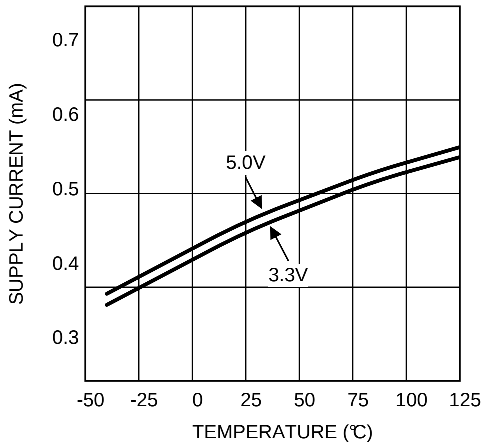

Figure 17.

Supply Current vs. Temperature Quad LMV834

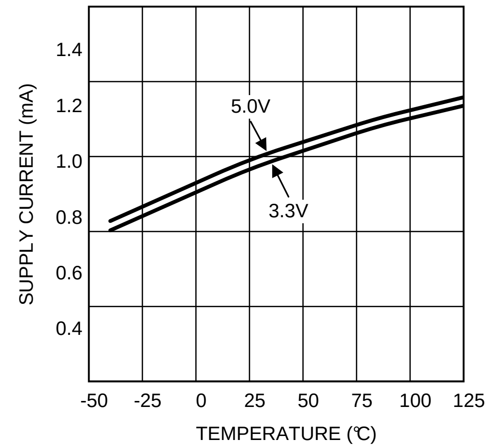

Figure 18.

Sinking Current vs. Supply Voltage

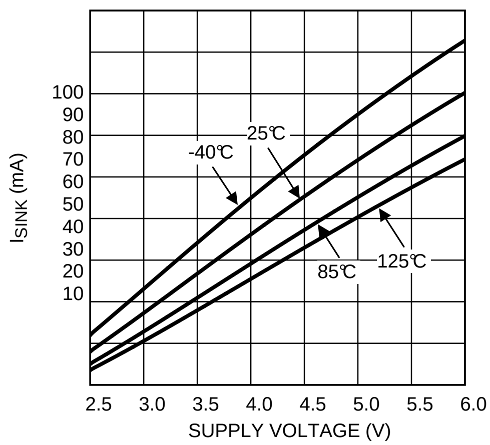

Figure 19.

Sourcing Current vs. Supply Voltage

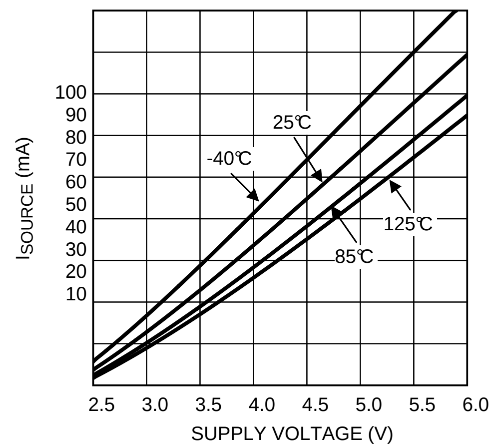

Figure 20.

Output Swing High vs. Supply Voltage R_L = 2 kΩ

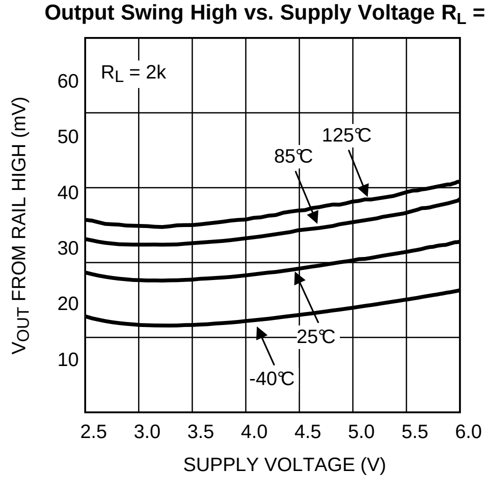

Figure 21.

Output Swing High vs. Supply Voltage R_L = 10 kΩ

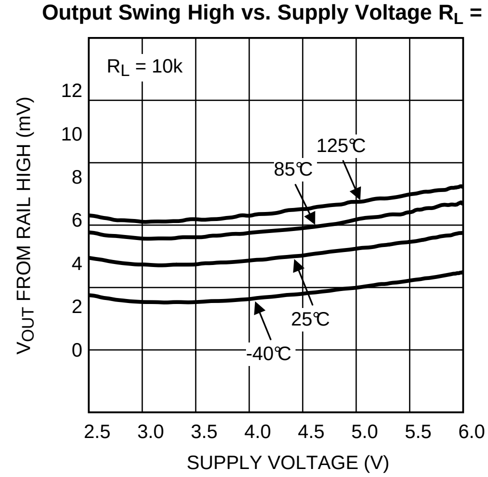

Figure 22.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

Output Swing Low vs. Supply Voltage R_L = 2 kΩ

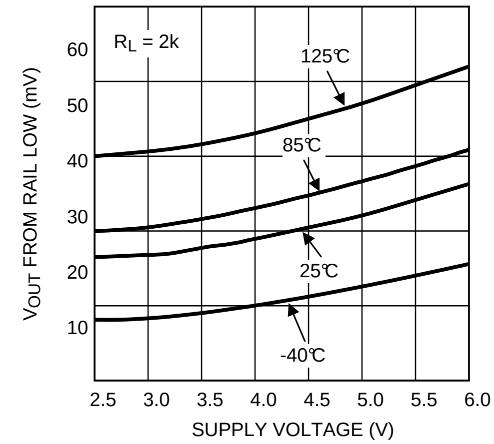

Figure 23.

Output Swing Low vs. Supply Voltage R_L = 10 kΩ

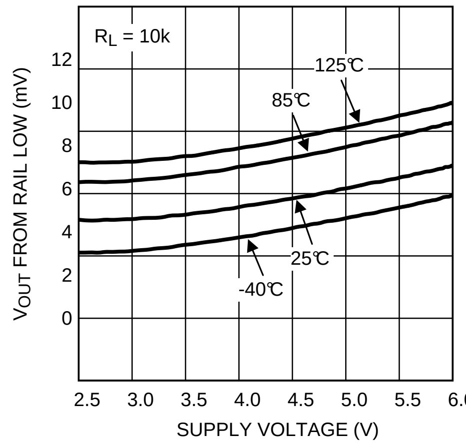

Figure 24.

Output Voltage Swing vs. Load Current at V^+ = 3.3V

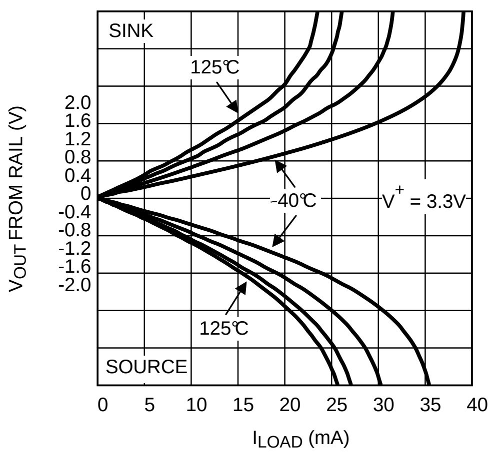

Figure 25.

Output Voltage Swing vs. Load Current at V^+ = 5.0V

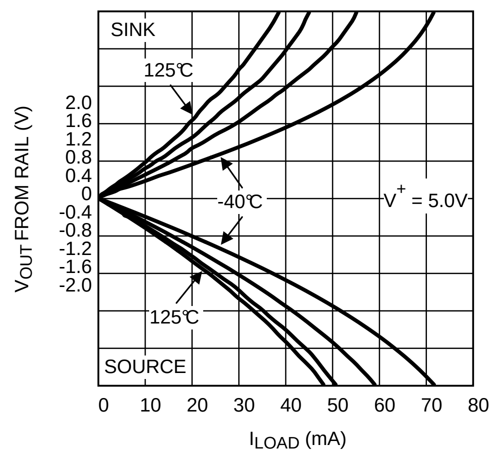

Figure 26.

Open Loop Frequency Response vs. Temperature

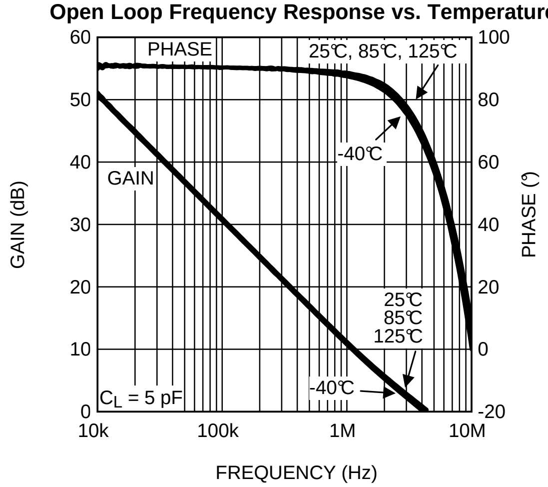

Figure 27.

Open Loop Frequency Response vs. Load Conditions

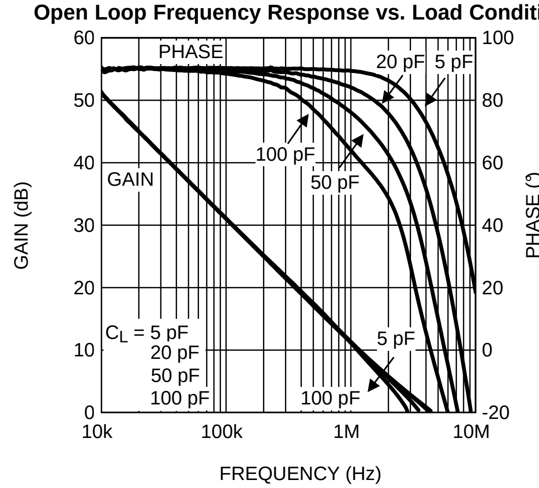

Figure 28.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

Phase Margin vs. Capacitive Load

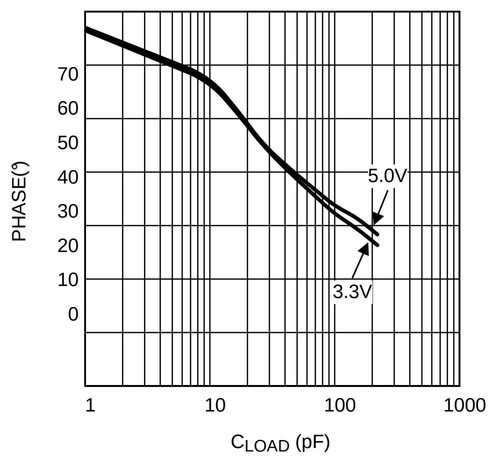

Figure 29.

PSRR vs. Frequency

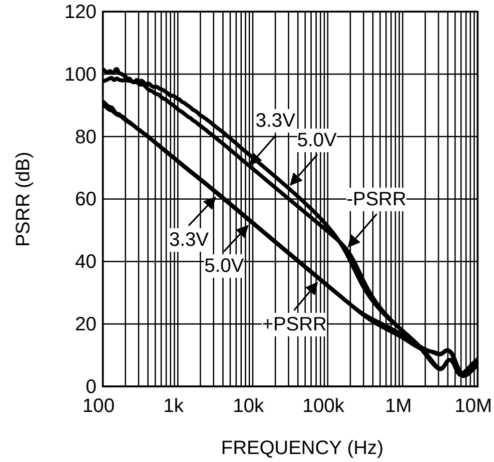

Figure 30.

CMRR vs. Frequency

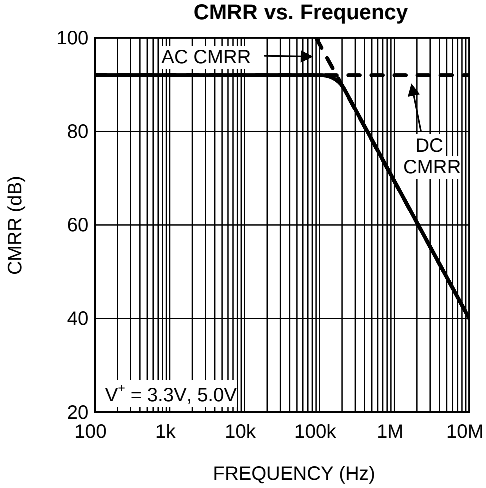

Figure 31.

Channel Separation vs. Frequency

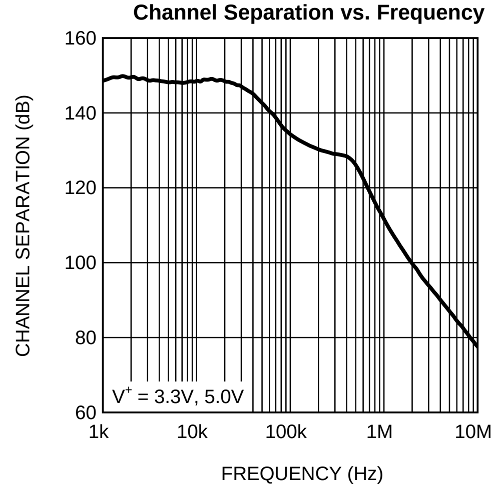

Figure 32.

Large Signal Step Response with Gain = 1

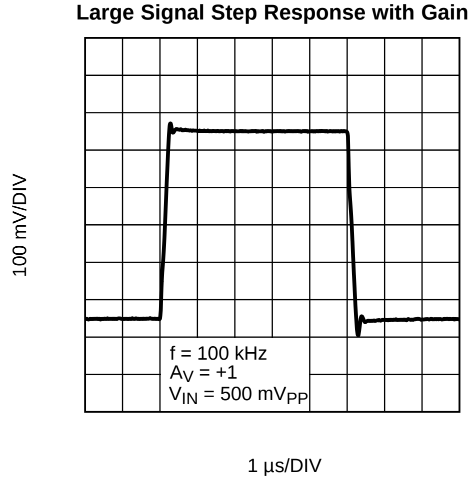

Figure 33.

Large Signal Step Response with Gain = 10

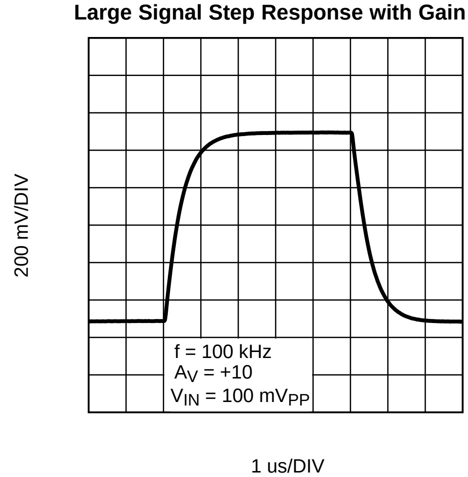

Figure 34.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

Small Signal Step Response with Gain = 1

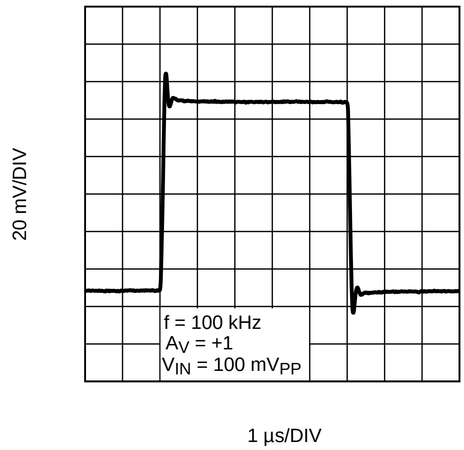

Figure 35.

Small Signal Step Response with Gain = 10

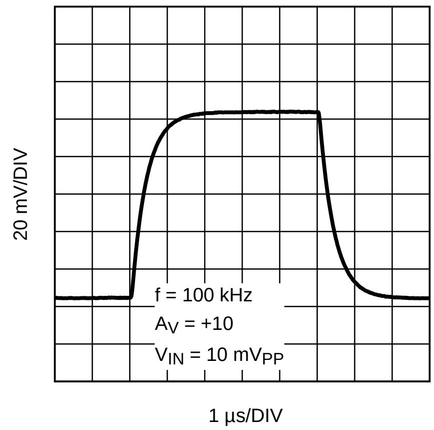

Figure 36.

Slew Rate vs. Supply Voltage

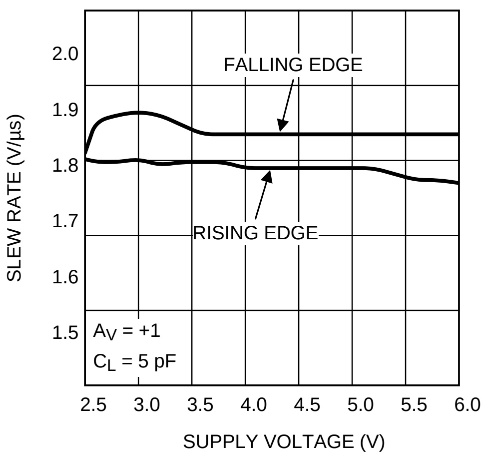

Figure 37.

Input Voltage Noise vs. Frequency

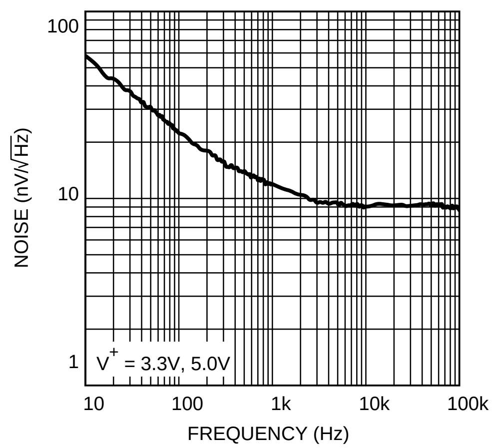

Figure 38.

THD+N vs. Frequency

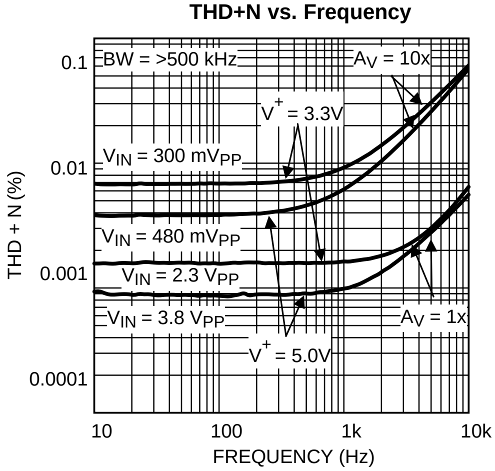

Figure 39.

THD+N vs. Amplitude

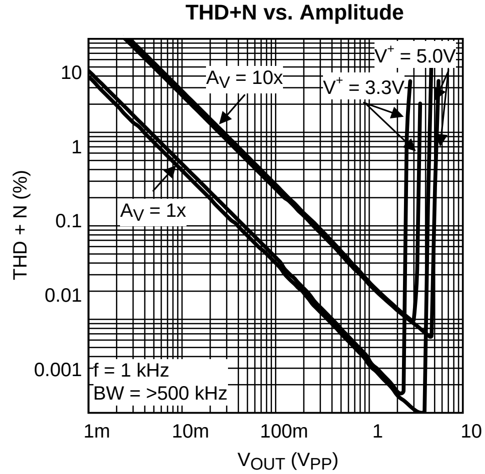

Figure 40.

Typical Performance Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3V, V^- = 0V, Unless otherwise specified.

R_{OUT} vs. Frequency

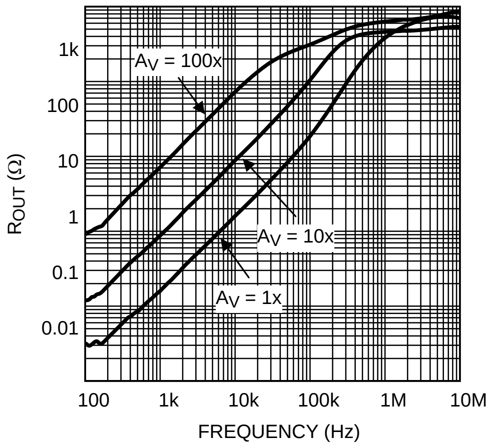

Figure 41.

EMIRR IN+ vs. Power at 400 MHz

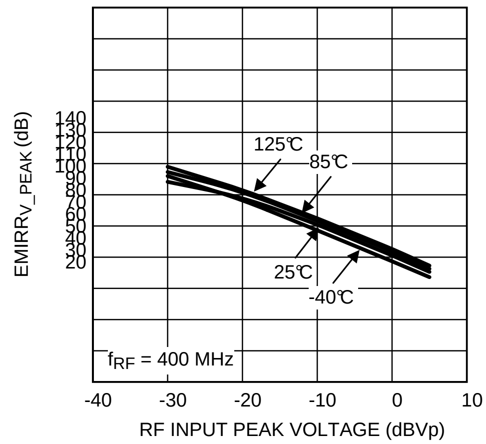

Figure 42.

EMIRR IN+ vs. Power at 900 MHz

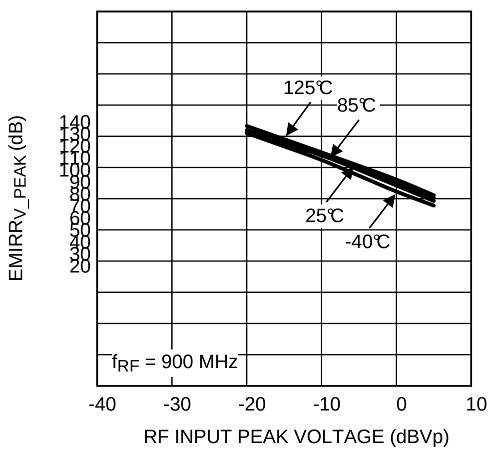

Figure 43.

EMIRR IN+ vs. Power at 1800 MHz

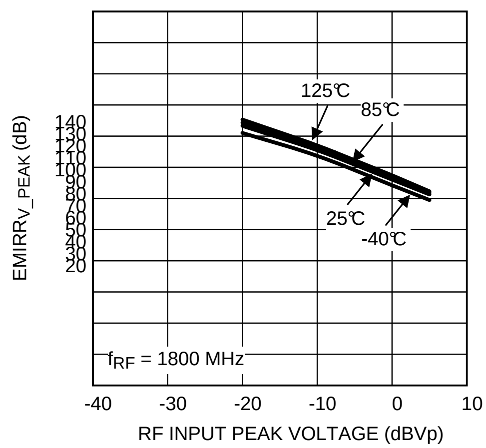

Figure 44.

EMIRR IN+ vs. Power at 2400 MHz

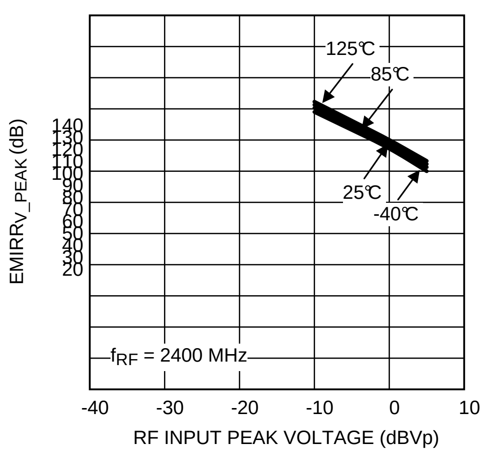

Figure 45.

EMIRR IN+ vs. Frequency

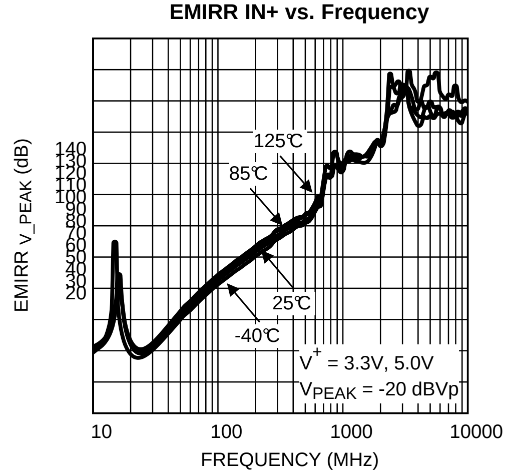

Figure 46.

APPLICATION INFORMATION

INTRODUCTION

The LMV831, LMV832 and LMV834 are operational amplifiers with excellent specifications, such as low offset, low noise and a rail-to-rail output. These specifications make the LMV831, LMV832 and LMV834 great choices for medical and instrumentation applications such as diagnosis equipment. The low supply current is perfectly suited for battery powered equipment. The small packages, SC70 package for the LMV831, the TSSOP package for the dual LMV832 and the TSSOP package for the quad LMV834, make these parts a perfect choice for portable electronics. Additionally, the EMI hardening makes the LMV831, LMV832 or LMV834 a must for almost all op amp applications. Most applications are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The LMV831, LMV832 and LMV834 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding. Using this EMI resistant series of op amps will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

INPUT CHARACTERISTICS

The input common mode voltage range of the LMV831, LMV832 and LMV834 includes ground, and can even sense well below ground. The CMRR level does not degrade for input levels up to 1.2V below the supply voltage. For a supply voltage of 5V, the maximum voltage that should be applied to the input for best CMRR performance is thus 3.8V.

When not configured as unity gain, this input limitation will usually not degrade the effective signal range. The output is rail-to-rail and therefore will introduce no limitations to the signal range.

The typical offset is only 0.25 mV, and the TCV_{OS} is 0.5 μV/°C, specifications close to precision op amps.

CMRR MEASUREMENT

The CMRR measurement results may need some clarification. This is because different setups are used to measure the AC CMRR and the DC CMRR.

The DC CMRR is derived from ΔV_{OS} versus ΔV_{CM}. This value is stated in the tables, and is tested during production testing. The AC CMRR is measured with the test circuit shown in Figure 47.

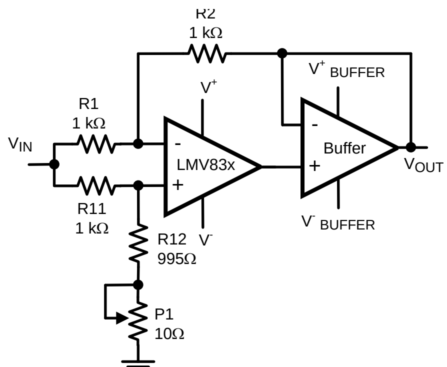

Figure 47. AC CMRR Measurement Setup

The configuration is largely the usually applied balanced configuration. With potentiometer P1, the balance can be tuned to compensate for the DC offset in the DUT. The main difference is the addition of the buffer. This buffer prevents the open-loop output impedance of the DUT from affecting the balance of the feedback network. Now the closed-loop output impedance of the buffer is a part of the balance. As the closed-loop output impedance is much lower, and by careful selection of the buffer also has a larger bandwidth, the total effect is that the CMRR of the DUT can be measured much more accurately. The differences are apparent in the larger measured bandwidth of the AC CMRR.

One artifact from this test circuit is that the low frequency CMRR results appear higher than expected. This is because in the AC CMRR test circuit the potentiometer is used to compensate for the DC mismatches. So, mainly AC mismatch is all that remains. Therefore, the obtained DC CMRR from this AC CMRR test circuit tends to be higher than the actual DC CMRR based on DC measurements.

The CMRR curve in Figure 48 shows a combination of the AC CMRR and the DC CMRR.

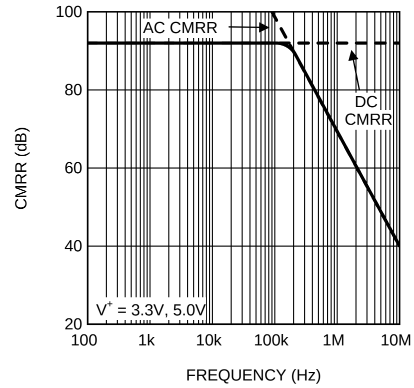

Figure 48. CMRR Curve

OUTPUT CHARACTERISTICS

As already mentioned the output is rail-to-rail. When loading the output with a 10 kΩ resistor the maximum swing of the output is typically 6 mV from the positive and negative rail.

The output of the LMV831/LMV832/LMV834 can drive currents up to 30 mA at 3.3V and even up to 65 mA at 5V

The LMV831/LMV832/LMV834 can be connected as non-inverting unity-gain amplifiers. This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed at the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating. The LMV831/LMV832/LMV834 can directly drive capacitive loads up to 200 pF without any stability issues. In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 49. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

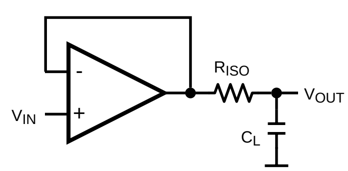

Figure 49. Isolating Capacitive Load

A resistor value of around 150Ω would be sufficient. As an example some values are given in the following table, for 5V.

C_{LOAD}	R_{ISO}
300 pF	165Ω
400 pF	175Ω
500 pF	185Ω

EMIRR

With the increase of RF transmitting devices in the world, the electromagnetic interference (EMI) between those devices and other equipment becomes a bigger challenge. The LMV831, LMV832 and LMV834 are EMI hardened op amps which are specifically designed to overcome electromagnetic interference. Along with EMI hardened op amps, the EMIRR parameter is introduced to unambiguously specify the EMI performance of an op amp. This section presents an overview of EMIRR. A detailed description on this specification for EMI hardened op amps can be found in Application Note AN-1698(SNOA497).

The dimensions of an op amp IC are relatively small compared to the wavelength of the disturbing RF signals. As a result the op amp itself will hardly receive any disturbances. The RF signals interfering with the op amp are dominantly received by the PCB and wiring connected to the op amp. As a result the RF signals on the pins of the op amp can be represented by voltages and currents. This representation significantly simplifies the unambiguous measurement and specification of the EMI performance of an op amp.

RF signals interfere with op amps via the non-linearity of the op amp circuitry. This non-linearity results in the detection of the so called out-of-band signals. The obtained effect is that the amplitude modulation of the out-of-band signal is downconverted into the base band. This base band can easily overlap with the band of the op amp circuit. As an example Figure 50 depicts a typical output signal of a unity-gain connected op amp in the presence of an interfering RF signal. Clearly the output voltage varies in the rhythm of the on-off keying of the RF carrier.

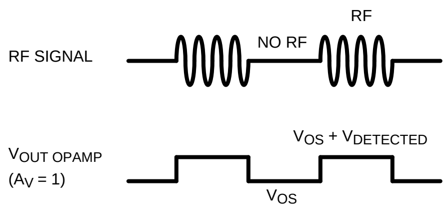

Figure 50. Offset voltage variation due to an interfering RF signal

EMIRR DEFINITION

To identify EMI hardened op amps, a parameter is needed that quantitatively describes the EMI performance of op amps. A quantitative measure enables the comparison and the ranking of op amps on their EMI robustness. Therefore the EMI Rejection Ratio (EMIRR) is introduced. This parameter describes the resulting input-referred offset voltage shift of an op amp as a result of an applied RF carrier (interference) with a certain frequency and level. The definition of EMIRR is given by:

$$EMIRR_{V_{RF\_PEAK}} = 20 \log \left(\frac{V_{RF\_PEAK}}{\Delta V_{OS}} \right)$$

In which

- V_{RF_PEAK} is the amplitude of the applied un-modulated RF signal (V)
- ΔV_{OS} is the resulting input-referred offset voltage shift (V) (1)

The offset voltage depends quadratically on the applied RF level, and therefore, the RF level at which the EMIRR is determined should be specified. The standard level for the RF signal is 100 mV_P. Application Note AN-1698(SNOA497) addresses the conversion of an EMIRR measured for an other signal level than 100 mV_P. The interpretation of the EMIRR parameter is straightforward. When two op amps have an EMIRR which differ by 20 dB, the resulting error signals when used in identical configurations, differ by 20 dB as well. So, the higher the EMIRR, the more robust the op amp.

Coupling an RF Signal to the IN+ Pin

Each of the op amp pins can be tested separately on EMIRR. In this section the measurements on the IN+ pin (which, based on symmetry considerations, also apply to the IN- pin) are discussed. In Application Note AN-1698(SNOA497) the other pins of the op amp are treated as well. For testing the IN+ pin the op amp is connected in the unity gain configuration. Applying the RF signal is straightforward as it can be connected directly to the IN+ pin. As a result the RF signal path has a minimum of components that might affect the RF signal level at the pin. The circuit diagram is shown in Figure 51. The PCB trace from RF_{IN} to the IN+ pin should be a 50Ω stripline in order to match the RF impedance of the cabling and the RF generator. On the PCB a 50Ω termination is used. This 50Ω resistor is also used to set the bias level of the IN+ pin to ground level. For determining the EMIRR, two measurements are needed: one is measuring the DC output level when the RF signal is off; and the other is measuring the DC output level when the RF signal is switched on. The difference of the two DC levels is the output voltage shift as a result of the RF signal. As the op amp is in the unity gain configuration, the input referred offset voltage shift corresponds one-to-one to the measured output voltage shift.

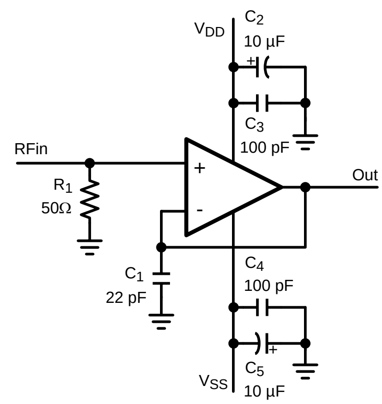

Figure 51. Circuit for coupling the RF signal to IN+

Cell Phone Call

The effect of electromagnetic interference is demonstrated in a setup where a cell phone interferes with a pressure sensor application. The application is shown in Figure 53.

This application needs two op amps and therefore a dual op amp is used. The op amp configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. The op amps are placed in a single supply configuration.

The experiment is performed on two different dual op amps: a typical standard op amp and the LMV832, EMI hardened dual op amp. A cell phone is placed on a fixed position a couple of centimeters from the op amps in the sensor circuit.

When the cell phone is called, the PCB and wiring connected to the op amps receive the RF signal. Subsequently, the op amps detect the RF voltages and currents that end up at their pins. The resulting effect on the output of the second op amp is shown in Figure 52.

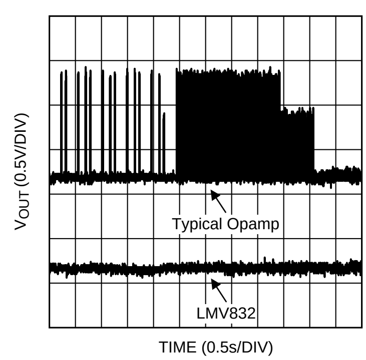

Figure 52. Comparing EMI Robustness

The difference between the two types of dual op amps is clearly visible. The typical standard dual op amp has an output shift (disturbed signal) larger than 1V as a result of the RF signal transmitted by the cell phone. The LMV832, EMI hardened op amp does not show any significant disturbances. This means that the RF signal will not disturb the signal entering the ADC when using the LMV832.

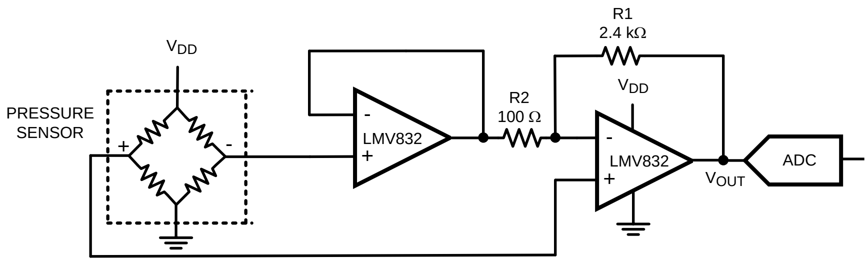

Figure 53. Pressure Sensor Application

DECOUPLING AND LAYOUT

Care must be given when creating a board layout for the op amp. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the op amp. For single supply, place a capacitor between V^+ and V^-. For dual supplies, place one capacitor between V^+ and the board ground, and a second capacitor between ground and V^-. Even with the LMV831/LMV832/LMV834 inherent hardening against EMI, it is still recommended to keep the input traces short and as far as possible from RF sources. Then the RF signals entering the chip are as low as possible, and the remaining EMI can be, almost, completely eliminated in the chip by the EMI reducing features of the LMV831/LMV832/LMV834.

PRESSURE SENSOR APPLICATION

The LMV831/LMV832/LMV834 can be used for pressure sensor applications. Because of their low power the LMV831/LMV832/LMV834 are ideal for portable applications, such as blood pressure measurement devices, or portable barometers. This example describes a universal pressure sensor that can be used as a starting point for different types of sensors and applications.

Pressure Sensor Characteristics

The pressure sensor used in this example functions as a Wheatstone bridge. The value of the resistors in the bridge change when pressure is applied to the sensor. This change of the resistor values will result in a differential output voltage, depending on the sensitivity of the sensor and the applied pressure. The difference between the output at full scale pressure and the output at zero pressure is defined as the span of the pressure sensor. A typical value for the span is 100 mV. A typical value for the resistors in the bridge is 5 kΩ. Loading of the resistor bridge could result in incorrect output voltages of the sensor. Therefore the selection of the circuit configuration, which connects to the sensor, should take into account a minimum loading of the sensor.

Pressure Sensor Example

The configuration shown in Figure 53 is simple, and is very useful for the read out of pressure sensors. With two op amps in this application, the dual LMV832 fits very well. The op amp configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. Given the differential output voltage V_S of the pressure sensor, the output signal of this op amp configuration, V_{OUT}, equals:

$$V_{OUT} = \frac{V_{DD}}{2} - \frac{V_S}{2}\left(1 + 2 \times \frac{R1}{R2}\right) \quad (2)$$

To align the pressure range with the full range of an ADC, the power supply voltage and the span of the pressure sensor are needed. For this example a power supply of 5V is used and the span of the sensor is 100 mV. When a 100Ω resistor is used for R2, and a 2.4 kΩ resistor is used for R1, the maximum voltage at the output is 4.95V and the minimum voltage is 0.05V. This signal is covering almost the full input range of the ADC. Further processing can take place in the microprocessor following the ADC.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV831MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV831MGE/NOPB	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV831MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV832MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV832MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV832MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV834MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV834 MT	Samples
LMV834MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV834 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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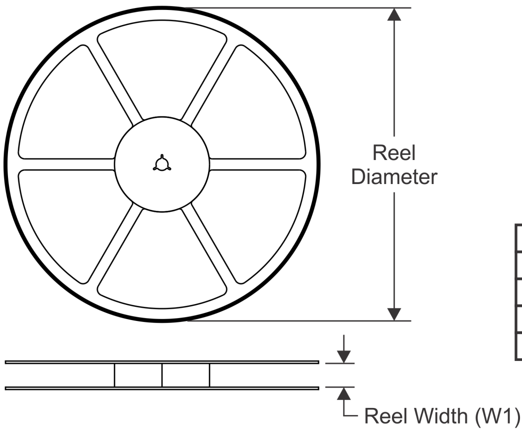
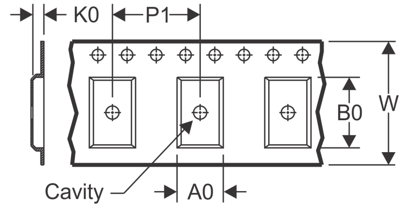
TAPE AND REEL INFORMATION

REEL DIMENSIONS

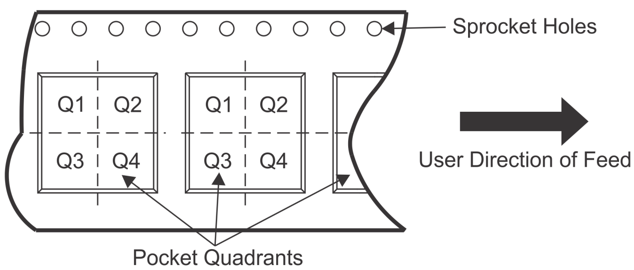


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

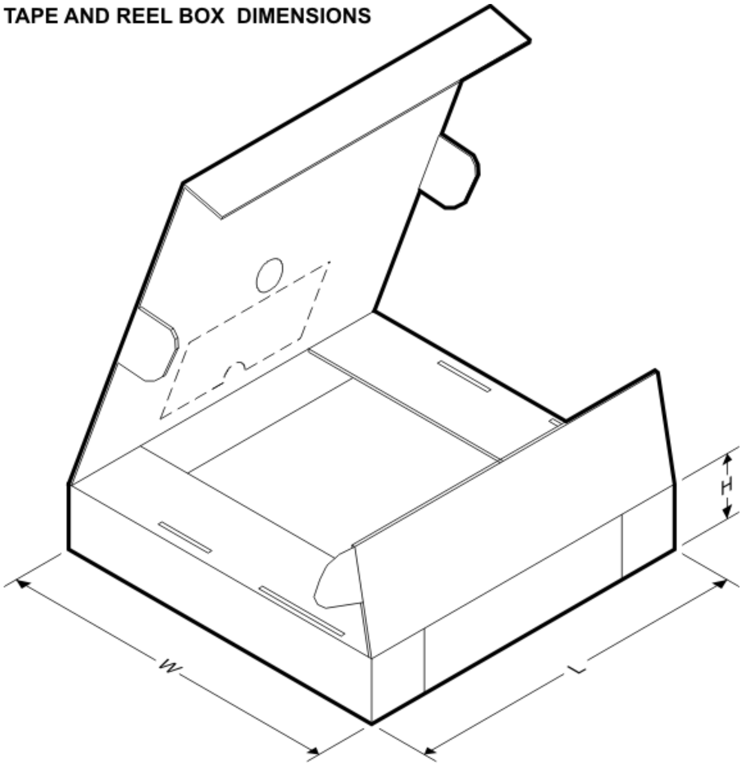
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV831MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV831MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV831MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV832MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV832MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV832MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV834MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

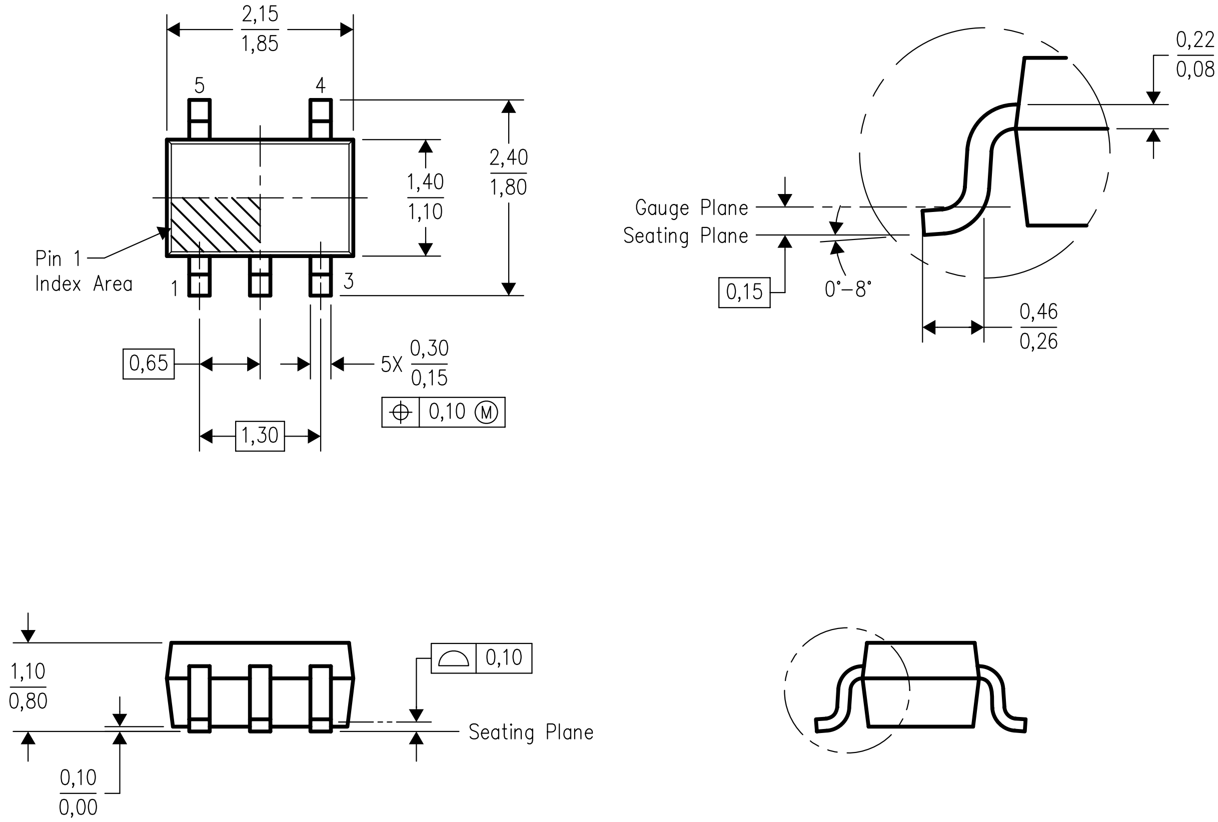
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV831MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV831MGE/NOPB	SC70	DCK	5	250	210.0	185.0	35.0
LMV831MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV832MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV832MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMV832MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV834MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

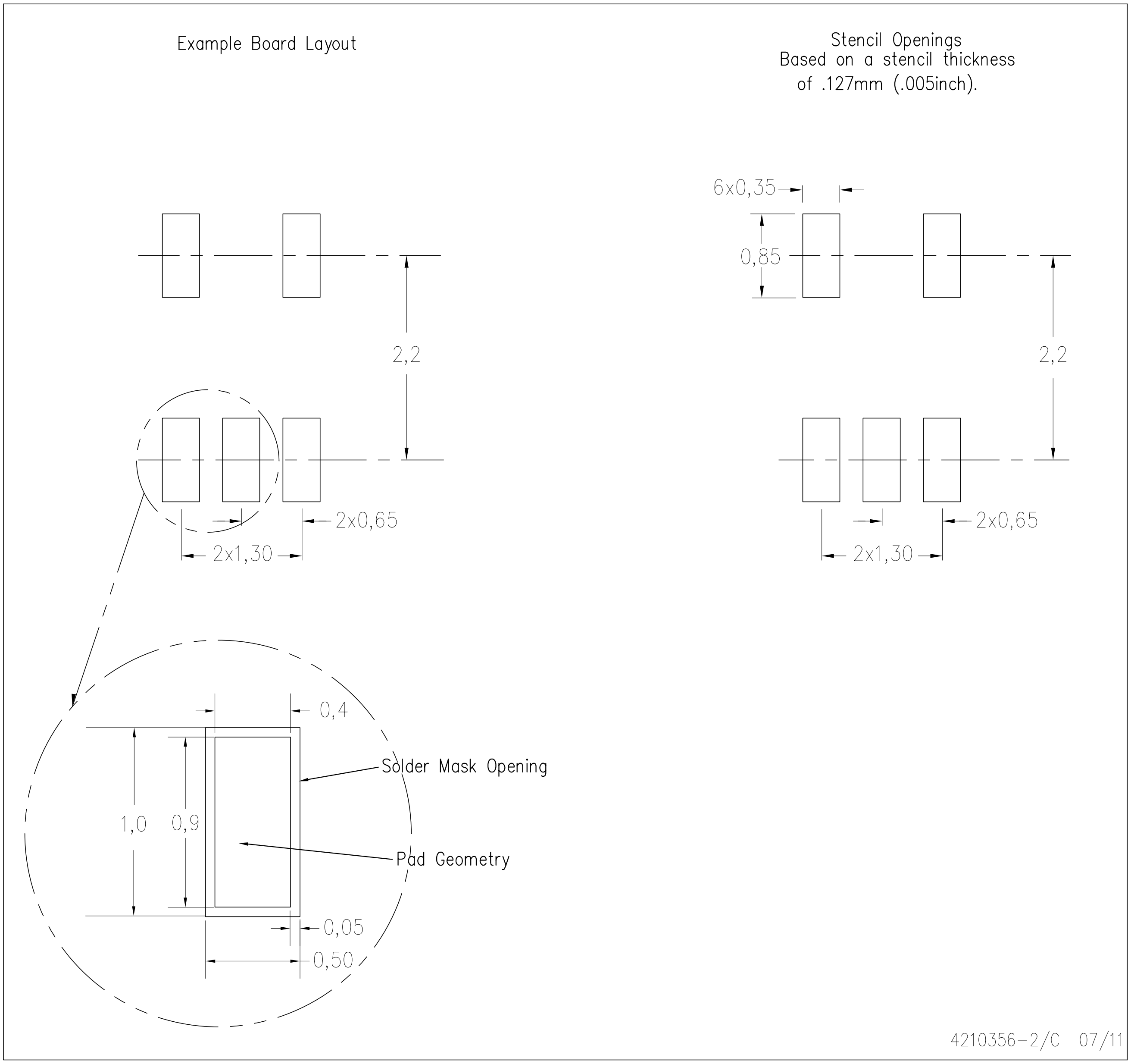
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

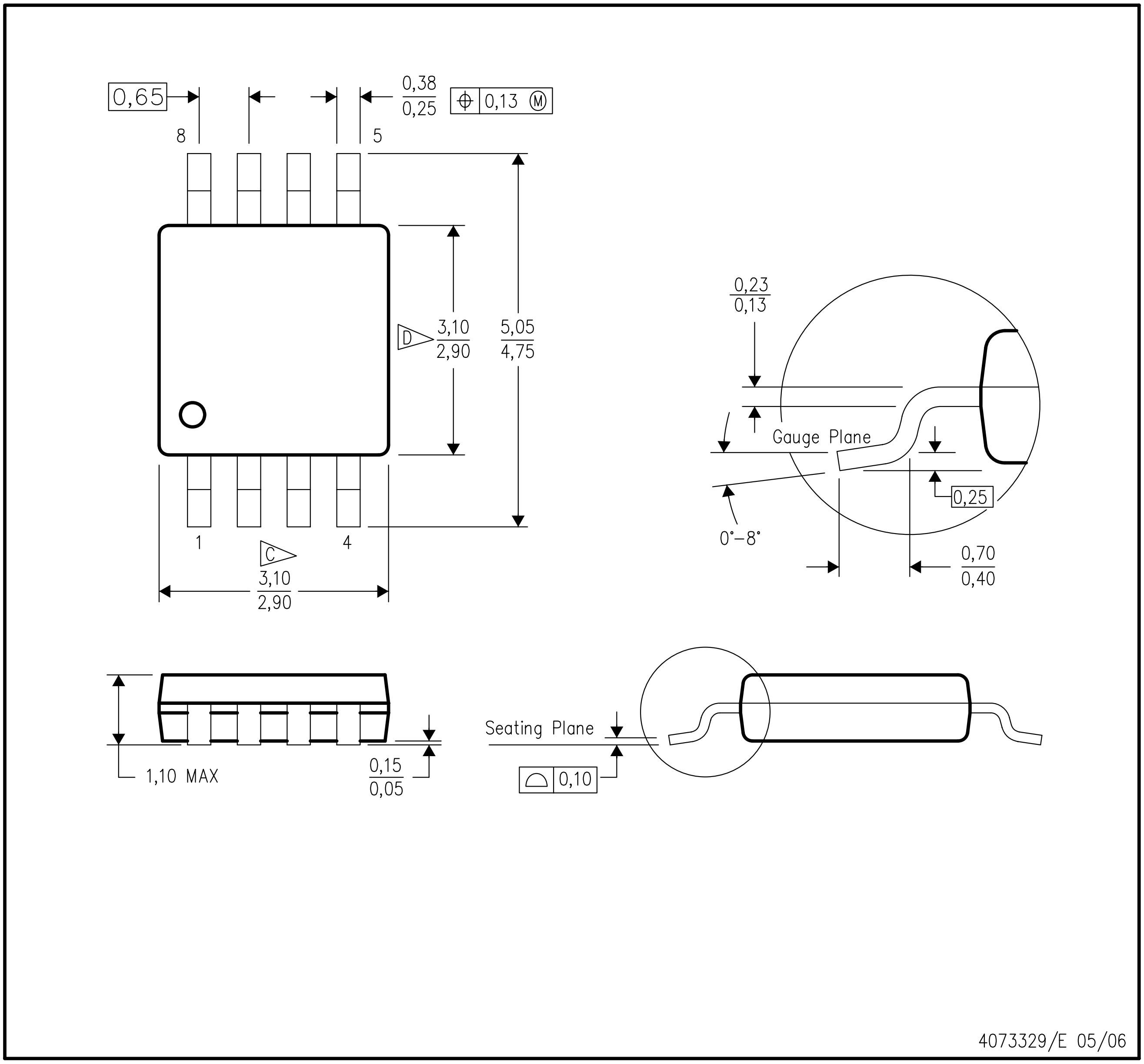
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



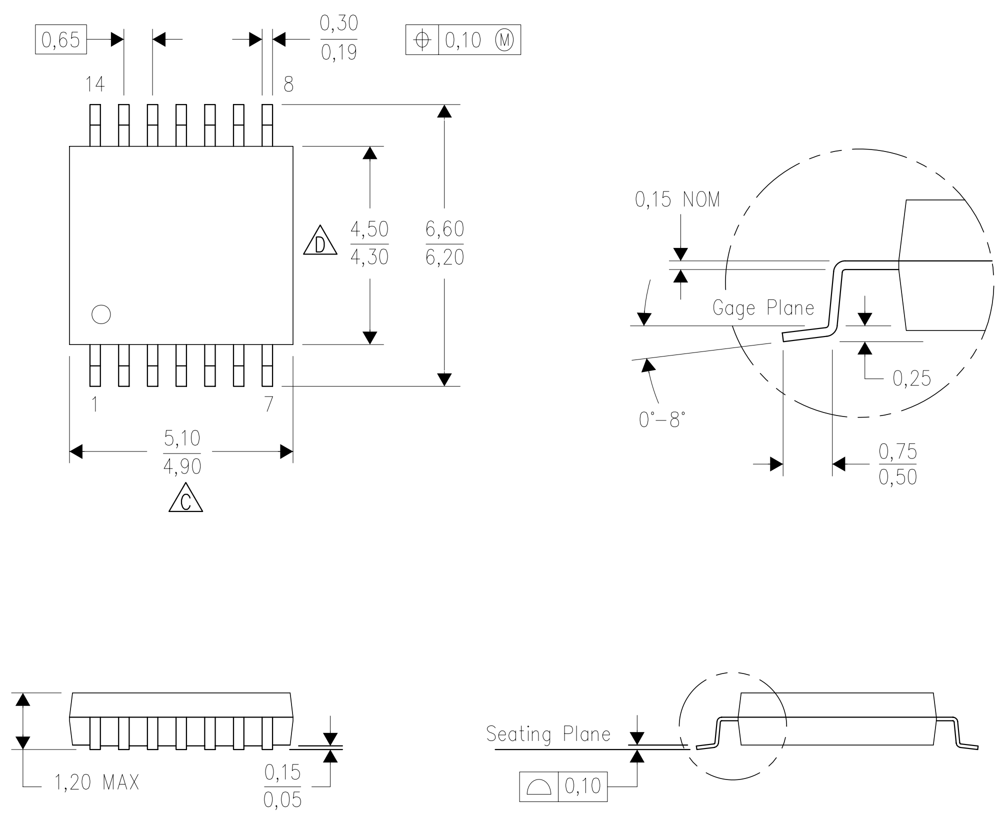
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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