



TMS320F28PLC8x Power Line Communications (PLC) Processors

1 Device Overview

1.1 Features

- System-on-Chip for Power Line Communications
 - Supports PLC Networks Using G3-PLC, PRIME, IEEE-1901.2, ITU G.9903, ITU G.9904 Standards in the CENELEC Frequency Band (35 kHz–90 kHz)
 - Designed to Operate With the AFE031 Analog Front End (AFE) for PLC
- Supports Texas Instruments PLC Software
 - IEEE 1901.2
 - ITU G.9903
 - ITU G.9904
 - PRIME
 - G3-PLC
- TMS320F28PLC84 Includes Key G3-PLC Firmware Routines Loaded into On-chip ROM
 - Opens On-chip Flash Memory for Future Firmware Enhancements
- 32-Bit C28x CPU Architecture Optimized for Orthogonal Frequency-Division Multiplex (OFDM) Communications
 - Viterbi/Complex Math Unit (VCU)
 - 90 MHz
- On-chip Memory
 - 256KB of Flash
 - 100KB of RAM
 - Boot ROM
- Power Supply
 - Single 3.3-V Power Supply
 - Option to Disable On-chip Low-Dropout (LDO) Regulator and Supply 1.8-V Core Voltage With External Regulator
- Communications Peripherals
 - Two Serial Peripheral Interface (SPI) Ports
 - Two Serial Communications Interface (SCI) Ports
 - One Multichannel Buffered Serial Port (McBSP)
 - McBSP Port can Also be Used as SPI
 - One Inter-Integrated-Circuit (I²C) Port
- Analog Subsystem
 - 12-Bit Analog-to-Digital Converters (ADCs), Each With Dual Sample-and-Hold (S/H)
 - ADC Operates at 3.4 MSPS
- 128-Bit Security Key and Lock
 - Protects Secure Memory Blocks
 - Prevents Firmware Reverse Engineering
 - Blocks JTAG Access When Enabled
- 80-Pin PN Low-Profile Quad Flatpack (LQFP)
- Industrial Temperature Range: –40°C to 105°C

1.2 Applications

- Electric Meters
- Power Line Communications Data Concentrators
- Solar Inverters



1.3 Description

The Texas Instruments TMS320F28PLC8x PLC processors are optimized to meet the requirements for AMI networks in Smart Grid installations that will use narrowband power line communications in the CENELEC frequency band. The CENELEC band is defined to be 35 kHz to 90 kHz.

The F28PLC8x processors are designed to execute the entire PLC protocol stack for the supported industry standards. TI supplies these firmware libraries to execute on the F28PLC8x processors with no additional license fees or royalties.

The F28PLC8x processors are also used in PLC data concentrators, which act as neighborhood-area collectors of electricity usage information from multiple end nodes.

The F28PLC8x processors are optimized to work with the AFE031 analog front end for PLC. The AFE031 is an integrated analog front end for narrowband PLC that is capable of driving a transformer-coupled connection to the AC Mains power line. It is ideal for driving high-current, low-impedance lines driving up to 1.9 A into reactive loads. The AFE031 is compliant to CENELEC A, B, C, and D (EN50065-1, -2, -3, -7) frequency bands.

See [Section 7.1.1.2](#) for a list of reference designs, starter kits, and tools.

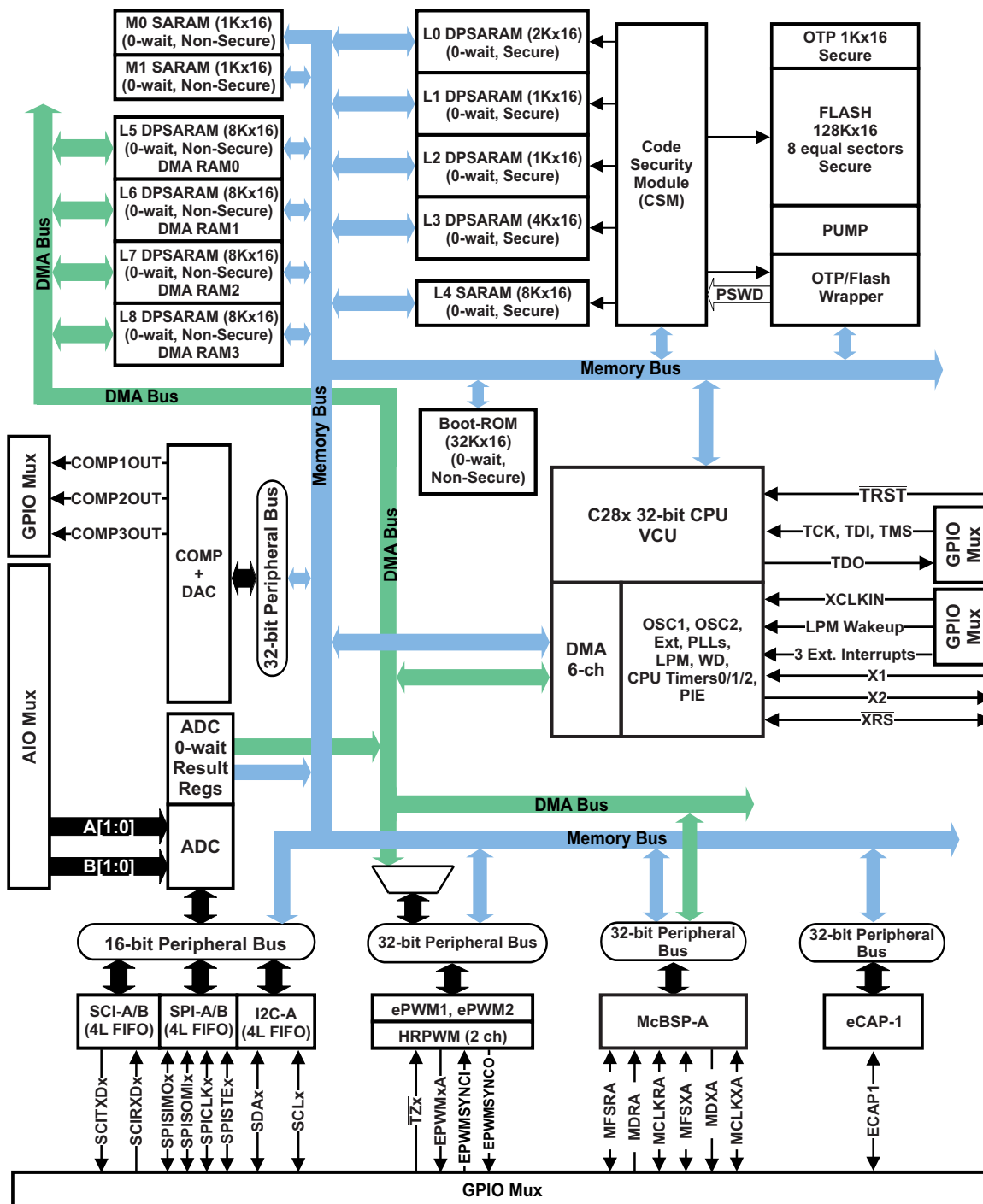
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|------------------|-----------|-------------------|
| TMS320F28PLC84PN | LQFP (80) | 12.0 mm × 12.0 mm |
| TMS320F28PLC83PN | LQFP (80) | 12.0 mm × 12.0 mm |

(1) For more information on these devices, see [Section 8](#), Mechanical Packaging and Orderable Information.

1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the device.



A. Not all peripheral pins are available at the same time due to multiplexing.

Figure 1-1. Functional Block Diagram

1.5 Additional Block Diagrams

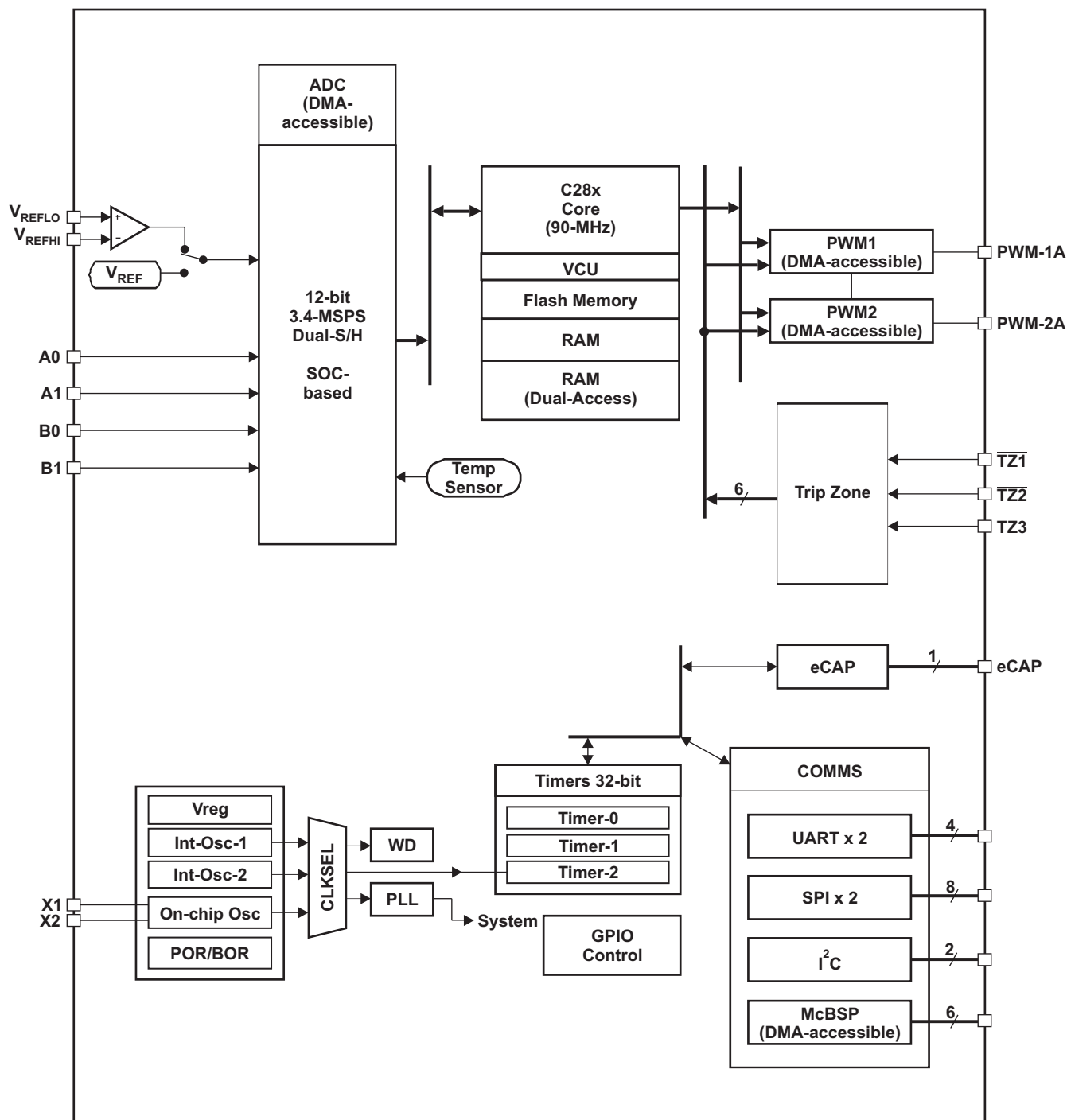


Figure 1-2. Peripheral Blocks

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|----------------|----------|-----------------|
| September 2014 | * | Initial Release |

3 Device Comparison

Table 3-1 lists the features of the F28PLC8x devices.

NOTE

The F28PLC84 device has the same hardware features as the F28PLC83 device. The only difference is that the F28PLC84 has a new ROM code with additional PLC software included.

Table 3-1. Device Comparison

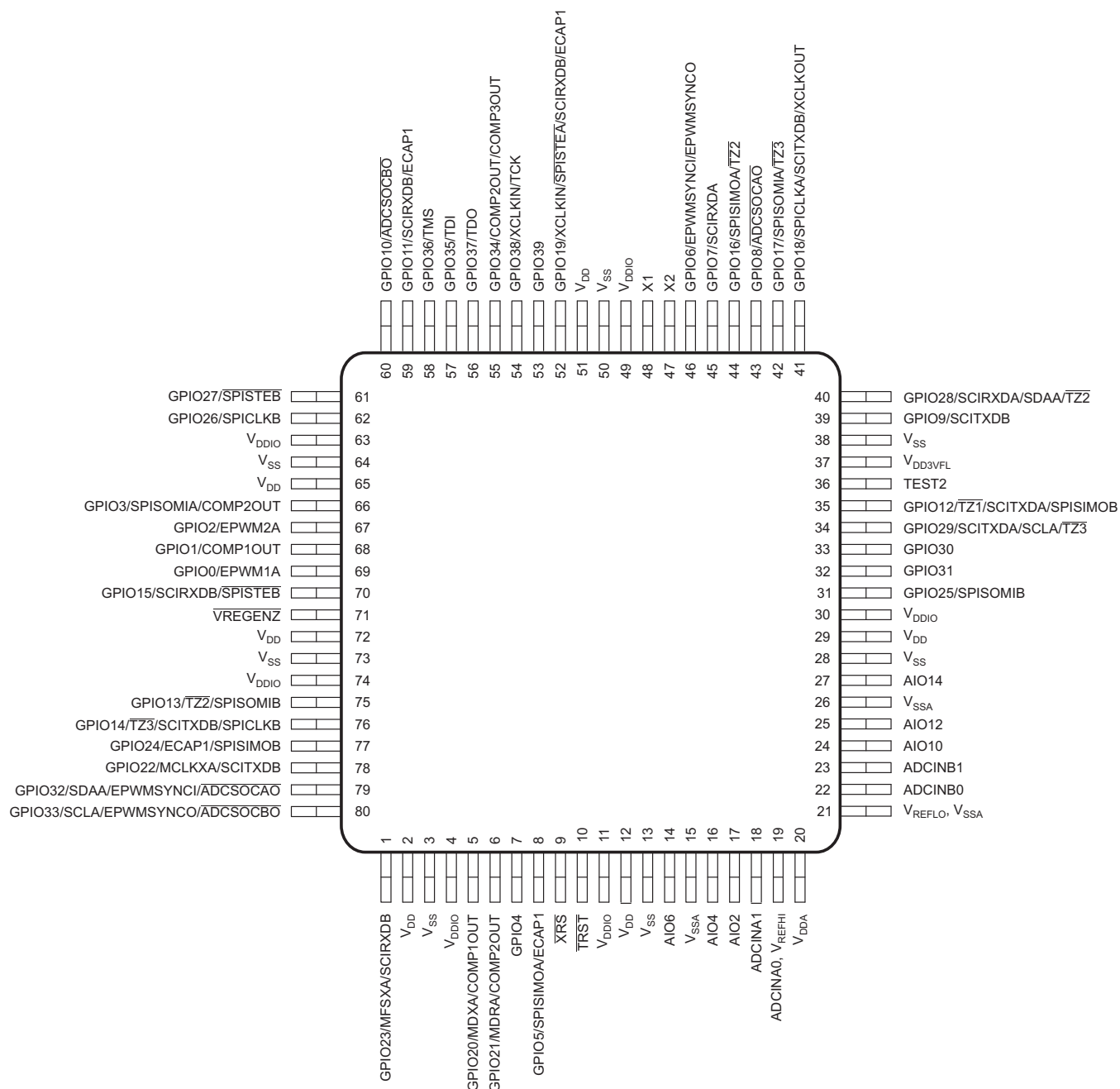
| FEATURE | | TYPE ⁽¹⁾ | F28PLC84 F28PLC83 (90 MHz) |
|--|-------------------------------------|---------------------|----------------------------------|
| Package Type | | | 80-Pin PN |
| Instruction cycle | | – | 11.11 ns |
| VCU | | | Yes |
| 6-Channel Direct Memory Access (DMA) | | 0 | Yes |
| On-chip Flash (16-bit word) | | – | 128K |
| On-chip SARAM (16-bit word) | | – | 50K |
| Code security for on-chip Flash, SARAM, and One-time programmable (OTP) blocks | | – | Yes |
| Boot ROM (32K x 16) | | – | Yes |
| OTP ROM (16-bit word) | | – | 1K |
| Enhanced Pulse Width Modulator (ePWM) channels | | 1 | 2 |
| High-resolution ePWM channels | | 1 | 2 |
| Enhanced Capture (eCAP) inputs | | 0 | 1 |
| Watchdog timer | | – | Yes |
| 12-Bit ADC | MSPS | 3 | 3.4 |
| | Conversion Time | | 289 ns |
| | Channels | | 4 |
| | Temperature Sensor | | Yes |
| | Dual Sample-and-Hold | | Yes |
| 32-Bit CPU timers | | – | 3 |
| Comparators with Integrated DACs | | 0 | 3 |
| I ² C | | 0 | 1 |
| McBSP | | 1 | 1 |
| SPI | | 1 | 2 |
| SCI | | 0 | 2 |
| 2-pin Oscillator | | | 1 |
| 0-pin Oscillator | | | 2 |
| I/O pins (shared) | General-Purpose Input/Output (GPIO) | – | 40 |
| | Analog Input/Output (AIO) | – | 6 |
| External interrupts | | – | 3 |
| Supply voltage (nominal) | | – | 3.3 V |
| Temperature options | T: –40°C to 105°C | – | Yes |
| Product status ⁽²⁾ | | – | TMS |

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) and in the peripheral reference guides.

(2) See [Section 7.1.2](#), Device and Development Support Tool Nomenclature, for descriptions of device stages. The "TMS" product status denotes a fully qualified production device.

4 Terminal Configuration and Functions

Figure 4-1 shows the pin assignments on the 80-pin PN package.



- A. Pin 19: V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN device and their use is mutually exclusive to one another.
Pin 21: V_{REFLO} is always connected to V_{SSA} on the 80-pin PN device.

Figure 4-1. 80-Pin PN Package (Top View)

4.1 Signal Descriptions

Table 4-1 describes the signals. With the exception of the JTAG pins, the GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Inputs are not 5-V tolerant. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups on the PWM pins are not enabled at reset. The pullups on other GPIO pins are enabled upon reset. The AIO pins do not have an internal pullup.

NOTE: When the on-chip voltage regulator (VREG) is used, the GPIO19, GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 pins could glitch during power up. If this behavior is unacceptable in an application, 1.8 V could be supplied externally. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered prior to the 1.9-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

Table 4-1. Signal Descriptions⁽¹⁾

| TERMINAL | | I/O/Z | DESCRIPTION |
|--------------------------|---------------|-------|--|
| NAME | PN PIN NO. | | |
| JTAG | | | |
| $\overline{\text{TRST}}$ | 10 | I | JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active-high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-k Ω resistor generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debugger and the application. (↓) |
| TCK | See GPIO38 | I | See GPIO38. JTAG test clock with internal pullup. (↑) |
| TMS | See GPIO36 | I | See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑) |
| TDI | See GPIO35 | I | See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑) |
| TDO | See GPIO37 | O/Z | See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8-mA drive) |
| FLASH | | | |
| V _{DD3VFL} | 37 | | 3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times. |
| TEST2 | 36 | I/O | Test Pin. Reserved for TI. Must be left unconnected. |

(1) I = Input, O = Output, Z = High Impedance, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown

Table 4-1. Signal Descriptions⁽¹⁾ (continued)

| TERMINAL | | I/O/Z | DESCRIPTION |
|-------------------------|--------------------------------|-------|---|
| NAME | PN PIN NO. | | |
| CLOCK | | | |
| XCLKOUT | See GPIO18 | O/Z | See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. The value of XCLKOUT is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propagate to the pin. |
| XCLKIN | See GPIO19 and GPIO38 | I | See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled via bit 14 in the CLKCTL register. If a crystal/resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. NOTE: Designs that use the GPIO38/XCLKIN/TCK pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This action is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device. |
| X1 | 48 | I | On-chip crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, this pin must be tied to GND. |
| X2 | 47 | O | On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, X2 must be left unconnected. |
| RESET | | | |
| $\overline{\text{XRS}}$ | 9 | I/OD | Device Reset (in) and Watchdog Reset (out). The F28PLC8x device has a built-in power-on reset (POR) and brown-out reset (BOR) circuitry. During a power-on or brown-out condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the device when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 k Ω and 10 k Ω should be placed between $\overline{\text{XRS}}$ and V_{DDIO} . If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup. (†) |

Table 4-1. Signal Descriptions⁽¹⁾ (continued)

| TERMINAL | | I/O/Z | DESCRIPTION |
|----------------------------------|------------|-------|--|
| NAME | PN PIN NO. | | |
| ADC, COMPARATOR, ANALOG I/O | | | |
| AIO6 | 14 | I/O | Digital AIO 6 |
| AIO4 | 16 | I/O | Digital AIO 4 |
| AIO2 | 17 | I/O | Digital AIO 2 |
| ADCINA1 | 18 | I | ADC Group A, Channel 1 input |
| ADCINA0 | 19 | I | ADC Group A, Channel 0 input. NOTE: V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN device and their use is mutually exclusive to one another. |
| V_{REFHI} | 19 | | ADC External Reference – only used when in ADC external reference mode. See Section 5.7.4.1.1 . NOTE: V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN device and their use is mutually exclusive to one another. |
| AIO14 | 27 | I/O | Digital AIO 14 |
| AIO12 | 25 | I/O | Digital AIO12 |
| AIO10 | 24 | I/O | Digital AIO 10 |
| ADCINB1 | 23 | I | ADC Group B, Channel 1 input |
| ADCINB0 | 22 | I | ADC Group B, Channel 0 input |
| V_{REFLO} | 21 | | NOTE: V_{REFLO} is always connected to V_{SSA} on the 80-pin PN device. |
| CPU AND I/O POWER | | | |
| V_{DDA} | 20 | | Analog Power Pin. Tie with a 2.2- μ F capacitor (typical) close to the pin. |
| V_{SSA} | 15 | | Analog Ground Pin. NOTE: V_{REFLO} is always connected to V_{SSA} on the 80-pin PN device. |
| V_{SSA} | 21 | | |
| V_{SSA} | 26 | | |
| V_{DD} | 2 | | CPU and Logic Digital Power Pins. When using internal VREG, place one 1.2- μ F capacitor between each V_{DD} pin and ground. Higher value capacitors may be used. |
| V_{DD} | 12 | | |
| V_{DD} | 29 | | |
| V_{DD} | 51 | | |
| V_{DD} | 65 | | |
| V_{DD} | 72 | | |
| V_{DDIO} | 4 | | Digital I/O and Flash Power Pin – Single Supply source when VREG is enabled. |
| V_{DDIO} | 11 | | |
| V_{DDIO} | 30 | | |
| V_{DDIO} | 49 | | |
| V_{DDIO} | 63 | | |
| V_{DDIO} | 74 | | |
| V_{SS} | 3 | | Digital Ground Pins |
| V_{SS} | 13 | | |
| V_{SS} | 28 | | |
| V_{SS} | 38 | | |
| V_{SS} | 50 | | |
| V_{SS} | 64 | | |
| V_{SS} | 73 | | |
| VOLTAGE REGULATOR CONTROL SIGNAL | | | |
| $\overline{VREGENZ}$ | 71 | I | Internal VREG Enable/Disable – pull low to enable VREG, pull high to disable VREG. |

Table 4-1. Signal Descriptions⁽¹⁾ (continued)

| TERMINAL | | I/O/Z | DESCRIPTION |
|--|---------------|------------------------|--|
| NAME | PN PIN NO. | | |
| GPIO AND PERIPHERAL SIGNALS ⁽¹⁾ | | | |
| GPIO0 EPWM1A | 69 | I/O/Z O | General-purpose input/output 0 Enhanced PWM1 Output A and High-resolution Pulse Width Modulator (HRPWM) channel |
| GPIO1 COMP1OUT | 68 | I/O/Z O | General-purpose input/output 1 Direct output of Comparator 1 |
| GPIO2 EPWM2A | 67 | I/O/Z O | General-purpose input/output 2 Enhanced PWM2 Output A and HRPWM channel |
| GPIO3 SPISOMIA COMP2OUT | 66 | I/O/Z I/O O | General-purpose input/output 3 SPI-A slave out, master in Direct output of Comparator 2 |
| GPIO4 | 7 | I/O/Z | General-purpose input/output 4 |
| GPIO5 SPISIMOA ECAP1 | 8 | I/O/Z I/O I/O | General-purpose input/output 5 SPI-A slave in, master out Enhanced Capture input/output 1 |
| GPIO6 EPWMSYNCl EPWMSYNCO | 46 | I/O/Z I O | General-purpose input/output 6 External ePWM sync pulse input External ePWM sync pulse output |
| GPIO7 SCIRXDA | 45 | I/O/Z I | General-purpose input/output 7 SCI-A receive data |
| GPIO8 Reserved ADCSOCAO | 43 | I/O/Z – O | General-purpose input/output 8 Reserved ADC start-of-conversion A |
| GPIO9 SCITXDB | 39 | I/O/Z O | General-purpose input/output 9 SCI-B transmit data |
| GPIO10 Reserved ADCSOCBO | 60 | I/O/Z – O | General-purpose input/output 10 Reserved ADC start-of-conversion B |
| GPIO11 SCIRXDB ECAP1 | 59 | I/O/Z I I/O | General-purpose input/output 11 SCI-B receive data Enhanced Capture input/output 1 |
| GPIO12 TZ1 SCITXDA SPISIMOB | 35 | I/O/Z I O I/O | General-purpose input/output 12 Trip Zone input 1 SCI-A transmit data SPI-B slave in, master out |
| GPIO13 TZ2 Reserved SPISOMIB | 75 | I/O/Z I – I/O | General-purpose input/output 13 Trip Zone input 2 Reserved SPI-B slave out, master in |
| GPIO14 TZ3 SCITXDB SPICLKB | 76 | I/O/Z I O I/O | General-purpose input/output 14 Trip zone input 3 SCI-B transmit data SPI-B clock input/output |

(1) The GPIO function (shown in bold italics) is the default at reset. The peripheral signals that are listed under them are alternate functions. For JTAG pins that have the GPIO functionality multiplexed, the input path to the GPIO block is always valid. The output path from the GPIO block and the path to the JTAG block from a pin is enabled or disabled based on the condition of the TRST signal.

Table 4-1. Signal Descriptions⁽¹⁾ (continued)

| TERMINAL | | I/O/Z | DESCRIPTION |
|--|---------------|-------------------------------|--|
| NAME | PN PIN NO. | | |
| GPIO15 SCIRXDB $\overline{\text{SPISTEB}}$ | 70 | I/O/Z I I/O | General-purpose input/output 15 SCI-B receive data SPI-B slave transmit enable input/output |
| GPIO16 SPISIMOA Reserved $\overline{\text{TZ2}}$ | 44 | I/O/Z I/O – I | General-purpose input/output 16 SPI-A slave in, master out Reserved Trip Zone input 2 |
| GPIO17 SPISOMIA Reserved $\overline{\text{TZ3}}$ | 42 | I/O/Z I/O – I | General-purpose input/output 17 SPI-A slave out, master in Reserved Trip zone input 3 |
| GPIO18 SPICKLA SCITXDB XCLKOUT | 41 | I/O/Z I/O O O/Z | General-purpose input/output 18 SPI-A clock input/output SCI-B transmit data Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. The value of XCLKOUT is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propagate to the pin. |
| GPIO19 XCLKIN $\overline{\text{SPISTEA}}$ SCIRXDB ECAP1 | 52 | I/O/Z I I/O I I/O | General-purpose input/output 19 External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if this path is being used for the other peripheral functions. SPI-A slave transmit enable input/output SCI-B receive data Enhanced Capture input/output 1 |
| GPIO20 MDXA COMP1OUT | 5 | I/O/Z O O | General-purpose input/output 20 McBSP transmit serial data Direct output of Comparator 1 |
| GPIO21 MDRA COMP2OUT | 6 | I/O/Z I O | General-purpose input/output 21 McBSP receive serial data Direct output of Comparator 2 |
| GPIO22 MCLKXA SCITXDB | 78 | I/O/Z I/O O | General-purpose input/output 22 McBSP transmit clock SCI-B transmit data |
| GPIO23 MFSXA SCIRXDB | 1 | I/O/Z I/O I | General-purpose input/output 23 McBSP transmit frame synch SCI-B receive data |
| GPIO24 ECAP1 SPISIMOB | 77 | I/O/Z I/O I/O | General-purpose input/output 24 Enhanced Capture input/output 1 SPI-B slave in, master out |
| GPIO25 SPISOMIB | 31 | I/O/Z I/O | General-purpose input/output 25 SPI-B slave out, master in |

Table 4-1. Signal Descriptions⁽¹⁾ (continued)

| TERMINAL | | I/O/Z | DESCRIPTION |
|--|------------|-------------------------|---|
| NAME | PN PIN NO. | | |
| GPIO26 SPICLKB | 62 | I/O/Z I/O | General-purpose input/output 26 SPI-B clock input/output |
| GPIO27 $\overline{\text{SPISTEB}}$ | 61 | I/O/Z I/O | General-purpose input/output 27 SPI-B slave transmit enable input/output |
| GPIO28 SCIRXDA SDAA $\overline{\text{TZ2}}$ | 40 | I/O/Z I I/OD I | General-purpose input/output 28 SCI-A receive data I ² C data open-drain bidirectional port Trip zone input 2 |
| GPIO29 SCITXDA SCLA $\overline{\text{TZ3}}$ | 34 | I/O/Z O I/OD I | General-purpose input/output 29 SCI-A transmit data I ² C clock open-drain bidirectional port Trip zone input 3 |
| GPIO30 | 33 | I/O/Z | General-purpose input/output 30 |
| GPIO31 | 32 | I/O/Z | General-purpose input/output 31 |
| GPIO32 SDAA EPWMSYNCI $\overline{\text{ADCSOCAO}}$ | 79 | I/O/Z I/OD I O | General-purpose input/output 32 I ² C data open-drain bidirectional port Enhanced PWM external sync pulse input ADC start-of-conversion A |
| GPIO33 SCLA EPWMSYNCO $\overline{\text{ADCSOCBO}}$ | 80 | I/O/Z I/OD O O | General-purpose input/output 33 I ² C clock open-drain bidirectional port Enhanced PWM external synch pulse output ADC start-of-conversion B |
| GPIO34 COMP2OUT COMP3OUT | 55 | I/O/Z O O | General-purpose input/output 34 Direct output of Comparator 2 Direct output of Comparator 3 |
| GPIO35 TDI | 57 | I/O/Z I | General-purpose input/output 35 JTAG test data input with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. |
| GPIO36 TMS | 58 | I/O/Z I | General-purpose input/output 36 JTAG test-mode select with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. |
| GPIO37 TDO | 56 | I/O/Z O/Z | General-purpose input/output 37 JTAG scan out, test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive). |
| GPIO38 XCLKIN TCK | 54 | I/O/Z I I | General-purpose input/output 38 External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if this path is being used for the other functions. JTAG test clock with internal pullup |
| GPIO39 | 53 | I/O/Z | General-purpose input/output 39 |

4.2 Pin Multiplexing

Table 4-2. GPIOA MUX^{(1) (2)}

| | DEFAULT AT RESET PRIMARY I/O FUNCTION | PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 | PERIPHERAL SELECTION 3 |
|--------------------------|---|---------------------------|---------------------------|---------------------------|
| GPAMUX1 REGISTER BITS | (GPAMUX1 BITS = 00) | (GPAMUX1 BITS = 01) | (GPAMUX1 BITS = 10) | (GPAMUX1 BITS = 11) |
| 1-0 | GPIO0 | EPWM1A (O) | Reserved | Reserved |
| 3-2 | GPIO1 | Reserved | Reserved | COMP1OUT (O) |
| 5-4 | GPIO2 | EPWM2A (O) | Reserved | Reserved |
| 7-6 | GPIO3 | Reserved | SPISOMIA (I/O) | COMP2OUT (O) |
| 9-8 | GPIO4 | Reserved | Reserved | Reserved |
| 11-10 | GPIO5 | Reserved | SPISIMOA (I/O) | ECAP1 (I/O) |
| 13-12 | GPIO6 | Reserved | EPWMSYNCl (I) | EPWMSYNCO (O) |
| 15-14 | GPIO7 | Reserved | SCIRXDA (I) | Reserved |
| 17-16 | GPIO8 | Reserved | Reserved | ADCSOCAO (O) |
| 19-18 | GPIO9 | Reserved | SCITXDB (O) | Reserved |
| 21-20 | GPIO10 | Reserved | Reserved | ADCSOCBO (O) |
| 23-22 | GPIO11 | Reserved | SCIRXDB (I) | ECAP1 (I/O) |
| 25-24 | GPIO12 | TZ1 (I) | SCITXDA (O) | SPISIMOB (I/O) |
| 27-26 | GPIO13 | TZ2 (I) | Reserved | SPISOMIB (I/O) |
| 29-28 | GPIO14 | TZ3 (I) | SCITXDB (O) | SPICLKB (I/O) |
| 31-30 | GPIO15 | Reserved | SCIRXDB (I) | SPISTEB (I/O) |
| GPAMUX2 REGISTER BITS | (GPAMUX2 BITS = 00) | (GPAMUX2 BITS = 01) | (GPAMUX2 BITS = 10) | (GPAMUX2 BITS = 11) |
| 1-0 | GPIO16 | SPISIMOA (I/O) | Reserved | TZ2 (I) |
| 3-2 | GPIO17 | SPISOMIA (I/O) | Reserved | TZ3 (I) |
| 5-4 | GPIO18 | SPICLKA (I/O) | SCITXDB (O) | XCLKOUT (O) |
| 7-6 | GPIO19/XCLKIN | SPISTEA (I/O) | SCIRXDB (I) | ECAP1 (I/O) |
| 9-8 | GPIO20 | Reserved | MDXA (O) | COMP1OUT (O) |
| 11-10 | GPIO21 | Reserved | MDRA (I) | COMP2OUT (O) |
| 13-12 | GPIO22 | Reserved | MCLKXA (I/O) | SCITXDB (O) |
| 15-14 | GPIO23 | Reserved | MFSXA (I/O) | SCIRXDB (I) |
| 17-16 | GPIO24 | ECAP1 (I/O) | Reserved | SPISIMOB (I/O) |
| 19-18 | GPIO25 | Reserved | Reserved | SPISOMIB (I/O) |
| 21-20 | GPIO26 | Reserved | Reserved | SPICLKB (I/O) |
| 23-22 | GPIO27 | Reserved | Reserved | SPISTEB (I/O) |
| 25-24 | GPIO28 | SCIRXDA (I) | SDAA (I/OD) | TZ2 (I) |
| 27-26 | GPIO29 | SCITXDA (O) | SCLA (I/OD) | TZ3 (I) |
| 29-28 | GPIO30 | Reserved | Reserved | Reserved |
| 31-30 | GPIO31 | Reserved | Reserved | Reserved |

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should the Reserved GPxMUX1/2 register setting be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

(2) I = Input, O = Output, OD = Open Drain

Table 4-3. GPIOB MUX⁽¹⁾⁽²⁾

| | DEFAULT AT RESET PRIMARY I/O FUNCTION | PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 | PERIPHERAL SELECTION 3 |
|--------------------------|--|---------------------------|---------------------------|---------------------------|
| GPBMUX1 REGISTER BITS | (GPBMUX1 BITS = 00) | (GPBMUX1 BITS = 01) | (GPBMUX1 BITS = 10) | (GPBMUX1 BITS = 11) |
| 1-0 | GPIO32 | SDAA (I/OD) | EPWMSYNCl (I) | ADCSOCAO (O) |
| 3-2 | GPIO33 | SCLA (I/OD) | EPWMSYNCO (O) | ADCSOCBO (O) |
| 5-4 | GPIO34 | COMP2OUT (O) | Reserved | COMP3OUT (O) |
| 7-6 | GPIO35 (TDI) | Reserved | Reserved | Reserved |
| 9-8 | GPIO36 (TMS) | Reserved | Reserved | Reserved |
| 11-10 | GPIO37 (TDO) | Reserved | Reserved | Reserved |
| 13-12 | GPIO38/XCLKIN (TCK) | Reserved | Reserved | Reserved |
| 15-14 | GPIO39 | Reserved | Reserved | Reserved |
| 17-16 | Reserved | Reserved | Reserved | Reserved |
| 19-18 | Reserved | Reserved | Reserved | Reserved |
| 21-20 | Reserved | Reserved | Reserved | Reserved |
| 23-22 | Reserved | Reserved | Reserved | Reserved |
| 25-24 | Reserved | Reserved | Reserved | Reserved |
| 27-26 | Reserved | Reserved | Reserved | Reserved |
| 29-28 | Reserved | Reserved | Reserved | Reserved |
| 31-30 | Reserved | Reserved | Reserved | Reserved |

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should the Reserved GPxMUX1/2 register setting be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

(2) I = Input, O = Output, OD = Open Drain

Table 4-4. Analog MUX⁽¹⁾

| | | DEFAULT AT RESET |
|-----------------------|---------------------------------|--|
| | AIOx AND PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3 |
| AIOMUX1 REGISTER BITS | AIOMUX1 BITS = 0,x | AIOMUX1 BITS = 1,x |
| 1-0 | ADCINA0 (I) | ADCINA0 (I) |
| 3-2 | ADCINA1 (I) | ADCINA1 (I) |
| 5-4 | AIO2 (I/O) | Reserved |
| 7-6 | Reserved | Reserved |
| 9-8 | AIO4 (I/O) | Reserved |
| 11-10 | Reserved | Reserved |
| 13-12 | AIO6 (I/O) | Reserved |
| 15-14 | Reserved | Reserved |
| 17-16 | ADCINB0 (I) | ADCINB0 (I) |
| 19-18 | ADCINB1 (I) | ADCINB1 (I) |
| 21-20 | AIO10 (I/O) | Reserved |
| 23-22 | Reserved | Reserved |
| 25-24 | AIO12 (I/O) | Reserved |
| 27-26 | Reserved | Reserved |
| 29-28 | AIO14 (I/O) | Reserved |
| 31-30 | Reserved | Reserved |

(1) I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings^{(1) (2)}

| | | |
|--|---------------------------|-----------------|
| Supply voltage range, V_{DDIO} (I/O and Flash) | with respect to V_{SS} | –0.3 V to 4.6 V |
| Supply voltage range, V_{DD} | with respect to V_{SS} | –0.3 V to 2.5 V |
| Analog voltage range, V_{DDA} | with respect to V_{SSA} | –0.3 V to 4.6 V |
| Input voltage range, V_{IN} (3.3 V) | | –0.3 V to 4.6 V |
| Output voltage range, V_O | | –0.3 V to 4.6 V |
| Input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{DDIO}$) ⁽³⁾ | | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$) | | ±20 mA |
| Junction temperature range, T_J ⁽⁴⁾ | | –40°C to 125°C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS} , unless otherwise noted.
- (3) Continuous clamp current per pin is ± 2 mA.
- (4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* ([SPRA953](#)).

5.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|-----------|--|---|------|-----|------|
| T_{stg} | Storage temperature range ⁽¹⁾ | | –65 | 150 | °C |
| V_{ESD} | Electrostatic discharge (ESD) ⁽²⁾ performance | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽³⁾ | –2 | 2 | kV |
| | | Charged Device Model (CDM), per JESD22-C101 ⁽⁴⁾ | –500 | 500 | V |

- (1) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* ([SPRA953](#)).
- (2) ESD measures device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
- (3) JEDEC publication JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (4) JEDEC publication JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|------------------------|----------------|-----|------------------|------|
| Device supply voltage, I/O, $V_{DDIO}^{(1)}$ | | 2.97 | 3.3 | 3.63 | V |
| Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally) | | 1.71 | 1.8 | 1.995 | V |
| Supply ground, V_{SS} | | | 0 | | V |
| Analog supply voltage, $V_{DDA}^{(1)}$ | | 2.97 | 3.3 | 3.63 | V |
| Analog ground, V_{SSA} | | | 0 | | V |
| Device clock frequency (system clock) | | 2 | | 90 | MHz |
| High-level input voltage, V_{IH} (3.3 V) | | 2 | | $V_{DDIO} + 0.3$ | V |
| Low-level input voltage, V_{IL} (3.3 V) | | $V_{SS} - 0.3$ | | 0.8 | V |
| High-level output source current, $V_{OH} = V_{OH(MIN)}$, I_{OH} | All GPIO/AIO pins | | | -4 | mA |
| | Group 2 ⁽²⁾ | | | -8 | mA |
| Low-level output sink current, $V_{OL} = V_{OL(MAX)}$, I_{OL} | All GPIO/AIO pins | | | 4 | mA |
| | Group 2 ⁽²⁾ | | | 8 | mA |
| Junction temperature, T_J | T version | -40 | | 105 | °C |

(1) V_{DDIO} and V_{DDA} should be maintained within approximately 0.3 V of each other.

(2) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37.

5.4 Electrical Characteristics⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|---|---|--|-------------------------|------|------|------|------|
| V _{OH} | High-level output voltage | I _{OH} = I _{OH} MAX | | 2.4 | | | V | |
| | | I _{OH} = 50 μA | | V _{DDIO} − 0.2 | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | 0.4 | | | V | |
| I _{IL} | Input current (low level) | Pin with pullup enabled | V _{DDIO} = 3.3 V, V _{IN} = 0 V | All GPIO | −80 | −140 | −205 | μA |
| | | | | \overline{XRS} pin | −230 | −300 | −375 | |
| | | Pin with pulldown enabled | V _{DDIO} = 3.3 V, V _{IN} = 0 V | ±2 | | | | |
| I _{IH} | Input current (high level) | Pin with pullup enabled | V _{DDIO} = 3.3 V, V _{IN} = V _{DDIO} | ±2 | | | μA | |
| | | Pin with pulldown enabled | V _{DDIO} = 3.3 V, V _{IN} = V _{DDIO} | 28 | 50 | 80 | | |
| I _{OZ} | Output current, pullup or pulldown disabled | V _O = V _{DDIO} or 0 V | | ±2 | | | μA | |
| C _I | Input capacitance | | | 2 | | | pF | |
| | V _{DDIO} BOR trip point | Falling V _{DDIO} | | 2.50 | 2.78 | 2.96 | V | |
| | V _{DDIO} BOR hysteresis | | | 35 | | | mV | |
| | Supervisor reset release delay time | Time after BOR/POR/OVR event is removed to \overline{XRS} release | | 400 | | 800 | μs | |
| | VREG V _{DD} output | Internal VREG on | | 1.9 | | | V | |

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

5.5 Thermal Resistance Characteristics for PN Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|---------------------------------|---|---------------------|-------------------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 7.9 | 0 |
| R θ_{JB} | Junction-to-board thermal resistance | 15.6 | 0 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 41.1 | 0 |
| | | 31.2 | 150 |
| | | 29.7 | 250 |
| | | 27.5 | 500 |
| Psi $_{JT}$ | Junction-to-package top | 0.4 | 0 |
| | | 0.6 | 150 |
| | | 0.7 | 250 |
| | | 0.9 | 500 |
| Psi $_{JB}$ | Junction-to-board | 15.3 | 0 |
| | | 14.6 | 150 |
| | | 14.4 | 250 |
| | | 14.1 | 500 |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

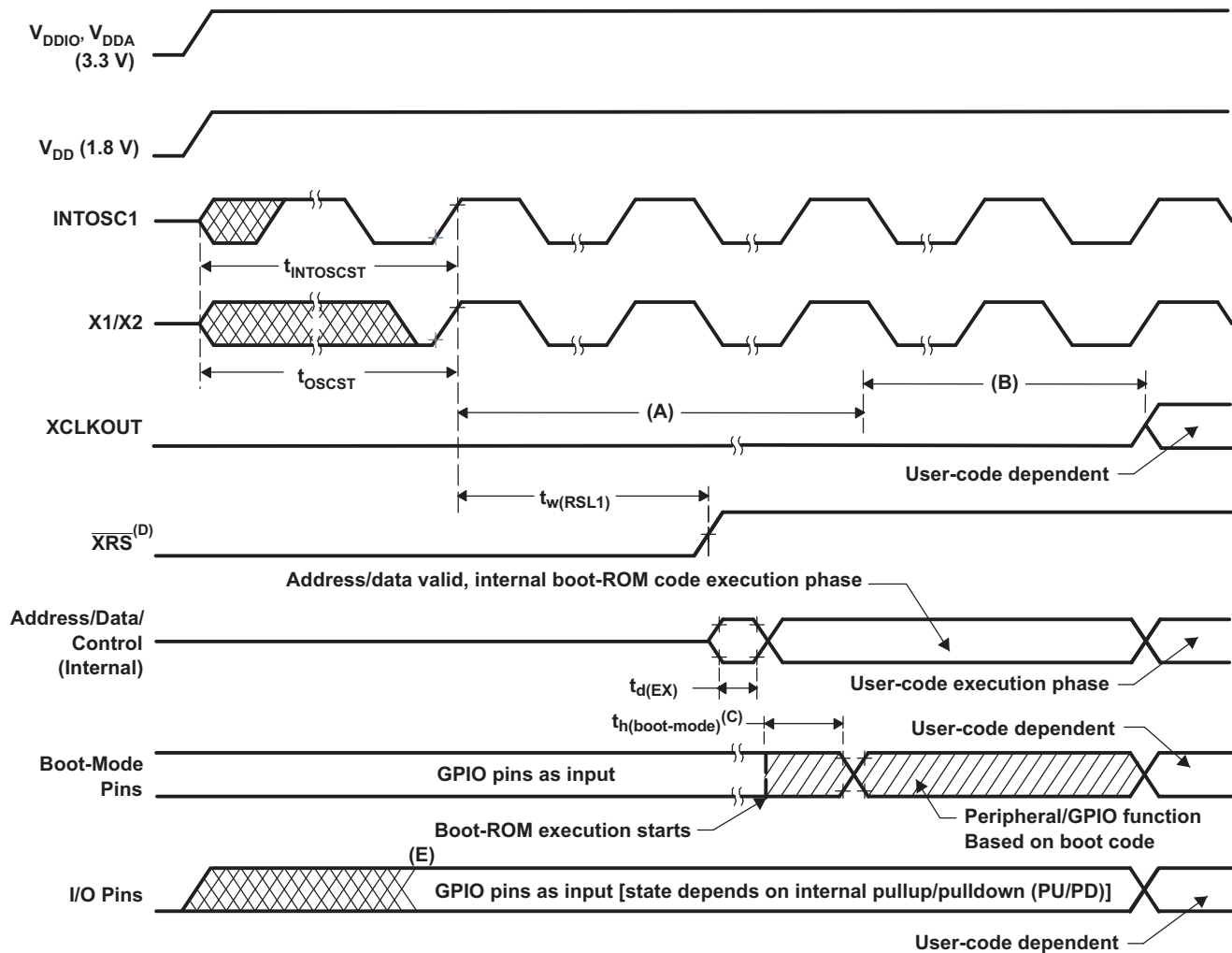
5.6 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *IC Package Thermal Metrics* ([SPRA953](#)) helps to understand the thermal metrics and definitions.

5.7 Timing and Switching Characteristics

5.7.1 Power Supply Sequencing

There is no power sequencing requirement needed to ensure the device is in the proper state after reset or to prevent the I/Os from glitching during power up/down (GPIO19, GPIO26–27, GPIO34–38 do not have glitch-free I/Os). No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, this value is 0.7 V above V_{DDA}) prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



- Upon power up, SYSCLKOUT is OSCCLK/4. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before SYSCLKOUT appears at XCLKOUT. XCLKOUT = OSCCLK/16 during this phase.
- Boot ROM configures the DIVSEL bits for /1 operation. XCLKOUT = OSCCLK/4 during this phase. Note that XCLKOUT will not be visible at the pin until explicitly configured by user code.
- After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.
- Using the XRS pin is optional due to the on-chip power-on reset circuitry.
- The internal pullup/pulldown will take effect when BOR is driven high.

Figure 5-1. Power-on Reset

5.7.2 Reset Timing

Table 5-1. Reset ($\overline{\text{XRS}}$) Timing Requirements

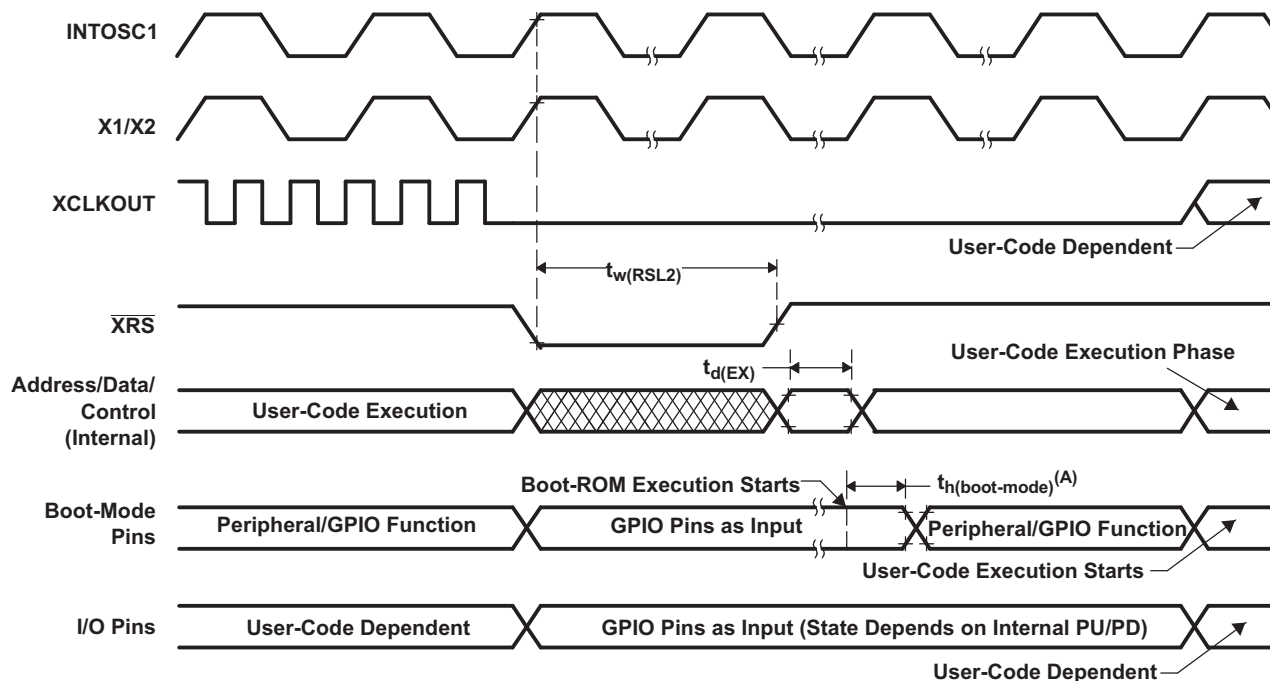
| | | MIN | MAX | UNIT |
|---------------------------|---|---------------------------|-----|--------|
| $t_{h(\text{boot-mode})}$ | Hold time for boot-mode pins | 1000 $t_{c(\text{SCO})}$ | | cycles |
| $t_{w(\text{RSL2})}$ | Pulse duration, $\overline{\text{XRS}}$ low on warm reset | 32 $t_{c(\text{OSCCLK})}$ | | cycles |

Table 5-2. Reset ($\overline{\text{XRS}}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|--------------------------|-----|----------------------------|-----|---------------|
| $t_{w(\text{RSL1})}$ | | 600 | | μs |
| $t_{w(\text{WDRS})}$ | | 512 $t_{c(\text{OSCCLK})}$ | | cycles |
| $t_{d(\text{EX})}$ | | 32 $t_{c(\text{OSCCLK})}$ | | cycles |
| t_{INTOSCST} | | 3 | | μs |
| $t_{\text{OSCST}}^{(1)}$ | 1 | 10 | | ms |

(1) Dependent on crystal/resonator and board design.



- A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 5-2. Warm Reset

Figure 5-3 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and $\text{SYSCLKOUT} = \text{OSCCLK} \times 2$. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, $\text{SYSCLKOUT} = \text{OSCCLK}/2$. After the PLL lock-up is complete, SYSCLKOUT reflects the new operating frequency, $\text{OSCCLK} \times 4$.

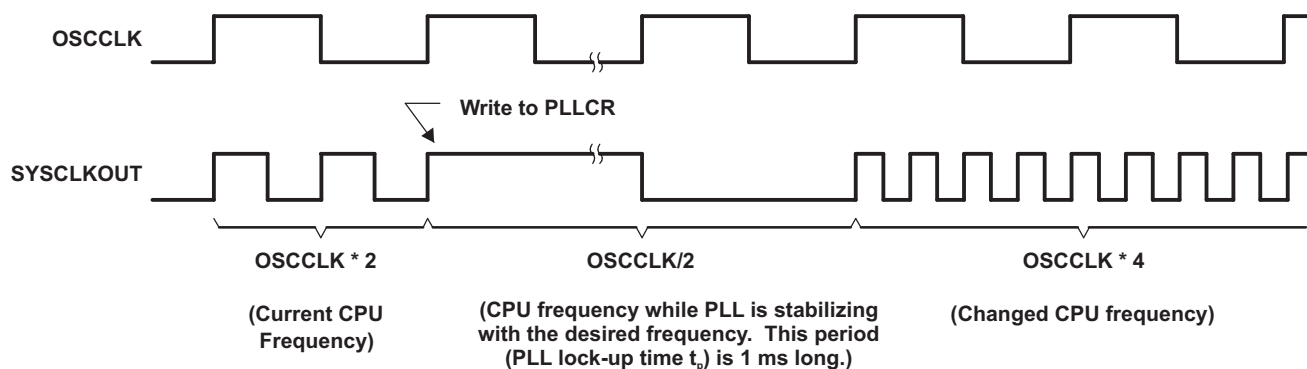


Figure 5-3. Example of Effect of Writing Into PLLCR Register

5.7.3 Clock Specifications

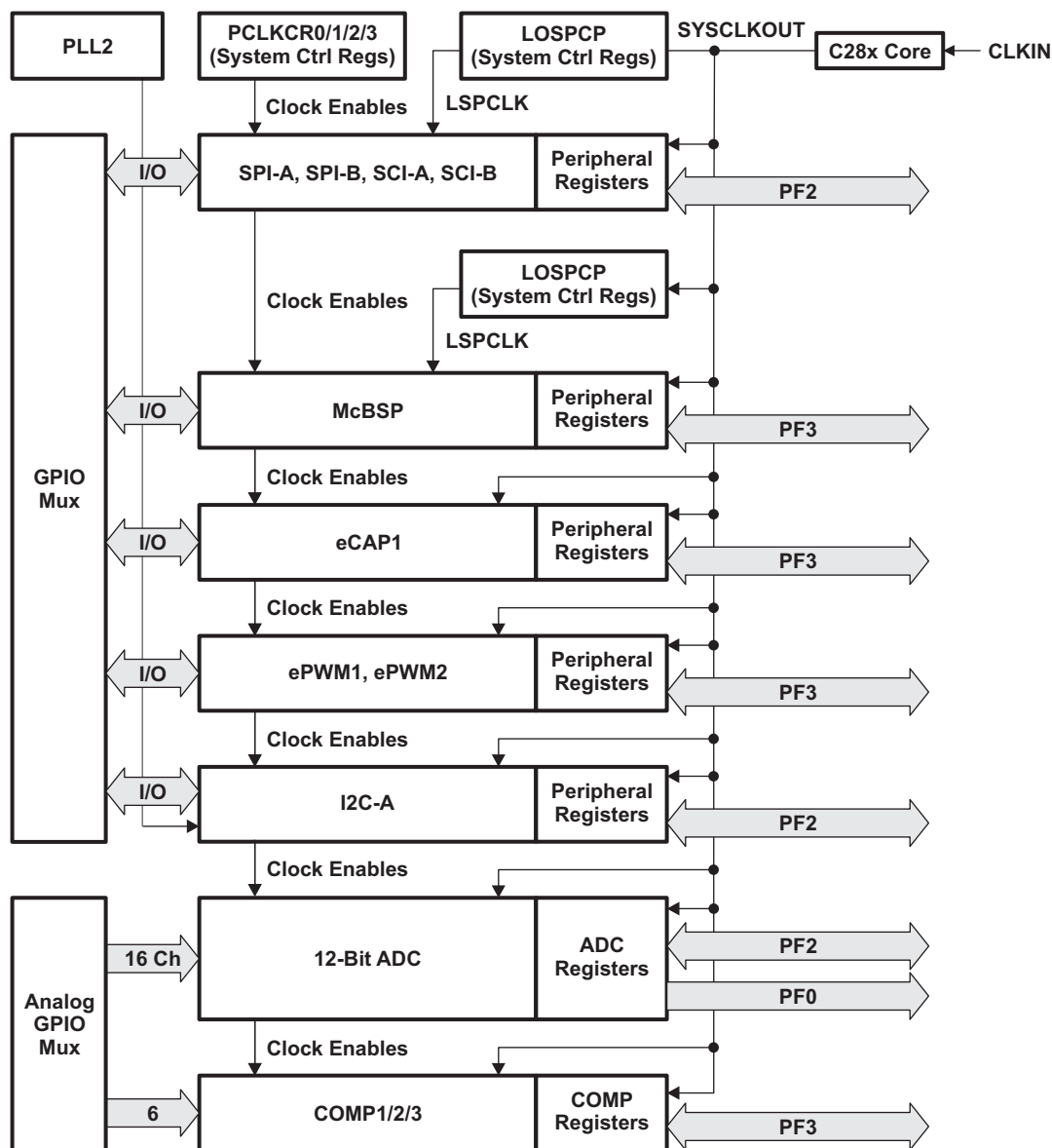
This section describes the oscillator and clocking mechanisms, the watchdog function and the low power modes.

Table 5-3. PLL, Clocking, Watchdog, and Low-Power Mode Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION ⁽¹⁾ |
|-------------|-----------|------------|---|
| BORCFG | 0x00 0985 | 1 | BOR Configuration Register |
| XCLK | 0x00 7010 | 1 | XCLKOUT Control |
| PLLSTS | 0x00 7011 | 1 | PLL Status Register |
| CLKCTL | 0x00 7012 | 1 | Clock Control Register |
| PLLLOCKPRD | 0x00 7013 | 1 | PLL Lock Period |
| INTOSC1TRIM | 0x00 7014 | 1 | Internal Oscillator 1 Trim Register |
| INTOSC2TRIM | 0x00 7016 | 1 | Internal Oscillator 2 Trim Register |
| PCLKCR2 | 0x00 7019 | 1 | Peripheral Clock Control Register 2 |
| LOSPCP | 0x00 701B | 1 | Low-Speed Peripheral Clock Prescaler Register |
| PCLKCR0 | 0x00 701C | 1 | Peripheral Clock Control Register 0 |
| PCLKCR1 | 0x00 701D | 1 | Peripheral Clock Control Register 1 |
| LPMCR0 | 0x00 701E | 1 | Low Power Mode Control Register 0 |
| PCLKCR3 | 0x00 7020 | 1 | Peripheral Clock Control Register 3 |
| PLLCR | 0x00 7021 | 1 | PLL Control Register |
| SCSR | 0x00 7022 | 1 | System Control and Status Register |
| WDCNTR | 0x00 7023 | 1 | Watchdog Counter Register |
| WDKEY | 0x00 7025 | 1 | Watchdog Reset Key Register |
| WDCR | 0x00 7029 | 1 | Watchdog Control Register |
| JTAGDEBUG | 0x00 702A | 1 | JTAG Port Debug Register |
| PLL2CTL | 0x00 7030 | 1 | PLL2 Configuration Register |
| PLL2MULT | 0x00 7032 | 1 | PLL2 Multiplier Register |
| PLL2STS | 0x00 7034 | 1 | PLL2 Lock Status Register |
| SYSCLK2CNTR | 0x00 7036 | 1 | SYSCLK2 Clock Counter Register |
| EPWMCFG | 0x00 703A | 1 | ePWM DMA Configuration Register |

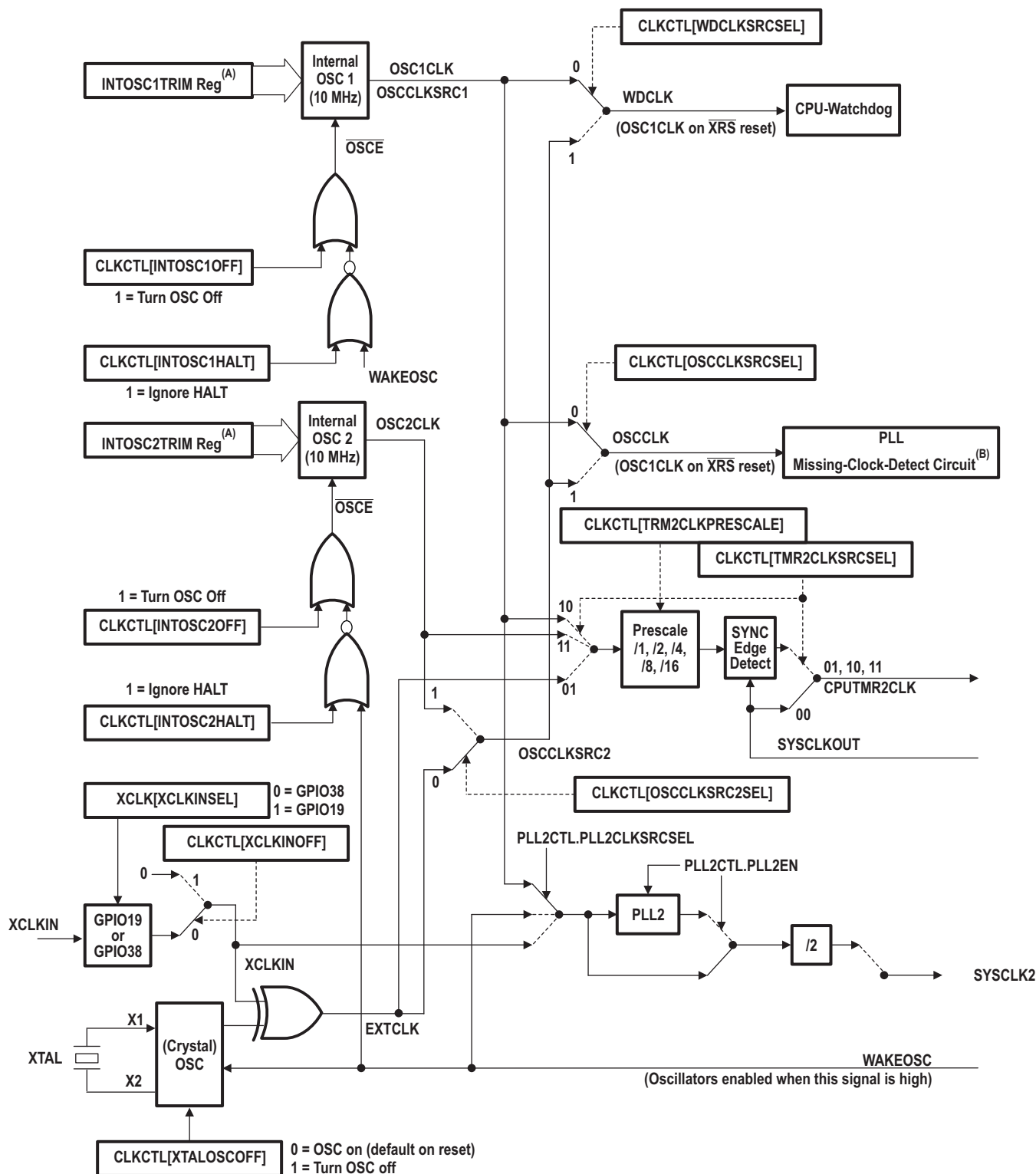
(1) All registers in this table are EALLOW protected.

Figure 5-4 shows the various clock domains that are discussed. Figure 5-5 shows the various clock sources (both internal and external) that can provide a clock for device operation.



- A. CLKIN is the clock into the CPU. CLKIN is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 5-4. Clock and Reset Domains



- A. Register loaded from TI OTP-based calibration function.
B. See [Section 5.7.3.5](#) for details on missing clock detection.

Figure 5-5. Clock Tree

5.7.3.1 Internal Zero Pin Oscillators

The F28PLC8x device contains two independent internal zero pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See [Section 5.7.3.8](#) for more information on these oscillators.

5.7.3.2 Crystal Oscillator Option

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in [Table 5-4](#). Furthermore, ESR range = 30 to 150 Ω .

Table 5-4. Typical Specifications for External Quartz Crystal⁽¹⁾

| FREQUENCY (MHz) | R_d (Ω) | C_{L1} (pF) | C_{L2} (pF) |
|-----------------|--------------------|---------------|---------------|
| 5 | 2200 | 18 | 18 |
| 10 | 470 | 15 | 15 |
| 15 | 0 | 15 | 15 |
| 20 | 0 | 12 | 12 |

(1) C_{shunt} should be less than or equal to 5 pF.

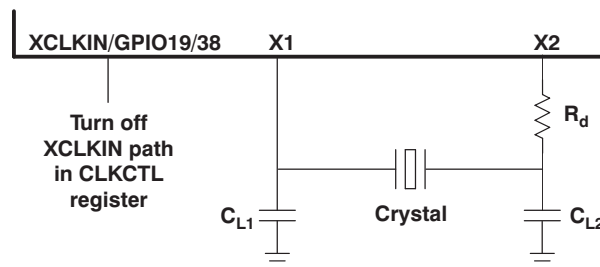


Figure 5-6. Using the On-chip Crystal Oscillator

NOTE

1. C_{L1} and C_{L2} are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the crystal's load capacitance.
2. The load capacitance of the crystal is described in the crystal specifications of the manufacturers.
3. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the F28PLC8x chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

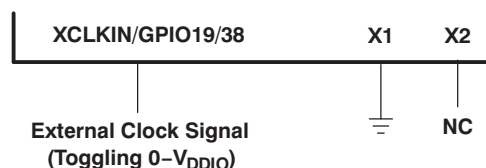


Figure 5-7. Using a 3.3-V External Oscillator

5.7.3.3 PLL-Based Clock Module

The F28PLC8x device has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 5-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. The watchdog module can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 5-5. PLL Settings

| PLLCR[DIV] VALUE ⁽¹⁾ (2) | SYSCLKOUT (CLKIN) | | |
|-------------------------------------|--|--------------------|--------------------|
| | PLLSTS[DIVSEL] = 0 or 1 ⁽³⁾ | PLLSTS[DIVSEL] = 2 | PLLSTS[DIVSEL] = 3 |
| 00000 (PLL bypass) | OSCCLK/4 (Default) ⁽¹⁾ | OSCCLK/2 | OSCCLK |
| 00001 | (OSCCLK * 1)/4 | (OSCCLK * 1)/2 | (OSCCLK * 1)/1 |
| 00010 | (OSCCLK * 2)/4 | (OSCCLK * 2)/2 | (OSCCLK * 2)/1 |
| 00011 | (OSCCLK * 3)/4 | (OSCCLK * 3)/2 | (OSCCLK * 3)/1 |
| 00100 | (OSCCLK * 4)/4 | (OSCCLK * 4)/2 | (OSCCLK * 4)/1 |
| 00101 | (OSCCLK * 5)/4 | (OSCCLK * 5)/2 | (OSCCLK * 5)/1 |
| 00110 | (OSCCLK * 6)/4 | (OSCCLK * 6)/2 | (OSCCLK * 6)/1 |
| 00111 | (OSCCLK * 7)/4 | (OSCCLK * 7)/2 | (OSCCLK * 7)/1 |
| 01000 | (OSCCLK * 8)/4 | (OSCCLK * 8)/2 | (OSCCLK * 8)/1 |
| 01001 | (OSCCLK * 9)/4 | (OSCCLK * 9)/2 | (OSCCLK * 9)/1 |
| 01010 | (OSCCLK * 10)/4 | (OSCCLK * 10)/2 | (OSCCLK * 10)/1 |
| 01011 | (OSCCLK * 11)/4 | (OSCCLK * 11)/2 | (OSCCLK * 11)/1 |
| 01100 | (OSCCLK * 12)/4 | (OSCCLK * 12)/2 | (OSCCLK * 12)/1 |
| 01101 | (OSCCLK * 13)/4 | (OSCCLK * 13)/2 | (OSCCLK * 13)/1 |
| 01110 | (OSCCLK * 14)/4 | (OSCCLK * 14)/2 | (OSCCLK * 14)/1 |
| 01111 | (OSCCLK * 15)/4 | (OSCCLK * 15)/2 | (OSCCLK * 15)/1 |
| 10000 | (OSCCLK * 16)/4 | (OSCCLK * 16)/2 | (OSCCLK * 16)/1 |
| 10001 | (OSCCLK * 17)/4 | (OSCCLK * 17)/2 | (OSCCLK * 17)/1 |
| 10010 | (OSCCLK * 18)/4 | (OSCCLK * 18)/2 | (OSCCLK * 18)/1 |

- (1) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{\text{XRS}}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
- (2) This register is EALLOW protected.
- (3) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes the PLLSTS[DIVSEL] configuration to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.

Table 5-6. CLKIN Divide Options

| PLLSTS [DIVSEL] | CLKIN DIVIDE |
|-----------------|--------------|
| 0 | /4 |
| 1 | /4 |
| 2 | /2 |
| 3 | /1 |

The PLL-based clock module provides four modes of operation:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** INTOSC1 is the on-chip internal oscillator 1. INTOSC1 can provide the clock for the Watchdog block, core and CPU-Timer 2
- **INTOSC2 (Internal Zero-pin Oscillator 2):** INTOSC2 is the on-chip internal oscillator 2. INTOSC2 can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins.
- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows the oscillator to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. Note that the XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 via the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 5-7. Possible PLL Configuration Modes

| PLL MODE | REMARKS | PLLSTS[DIVSEL] | CLKIN AND SYSCCLKOUT |
|------------|---|----------------|--|
| PLL Off | Invoked by the user setting the PLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. The PLL block being disabled can be useful in reducing system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN. | 0, 1 2 3 | OSCCLK/4 OSCCLK/2 OSCCLK/1 |
| PLL Bypass | PLL Bypass is the default PLL configuration upon power-up or after an external reset (XRS). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off. | 0, 1 2 3 | OSCCLK/4 OSCCLK/2 OSCCLK/1 |
| PLL Enable | Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks. | 0, 1 2 3 | OSCCLK * n/4 OSCCLK * n/2 OSCCLK * n/1 |

5.7.3.4 Phase-Locked Loop Module (PLL2)

In addition to the main system PLL, the F28PLC8x device also contains a second PLL (PLL2). The PLL supports multipliers of 1 to 15 and has a fixed divide-by-two on its output.

PLL2 may be clocked from the following three sources by modifying the PLL2CLKSRCSEL bits appropriately in the PLL2CTL register:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** INTOSC1 is the on-chip internal oscillator 1 and provides a 10-MHz clock.
- **Crystal/Resonator Operation:** The (crystal) oscillator enables the use of an external crystal or resonator attached to the device to provide the time base. The crystal or resonator is connected to the X1/X2 pins.
- **External Clock Source Operation:** This mode allows the reference clock to be derived from an external single-ended clock source connected to either GPIO19 or GPIO38. The XCLKINSEL bit in the XCLK register should be set appropriately to enable the selected GPIO to drive XCLKIN.

5.7.3.5 Loss of Input Clock (NMI Watchdog Function)

The F28PLC8x device may be clocked from either one of the internal zero-pin oscillators (INTOSC1 or INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1–5 MHz.

When the limp mode is activated, a CLOCKFAIL signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when the counter overflows. In addition to this action, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. [Figure 5-8](#) shows the interrupt mechanisms involved.

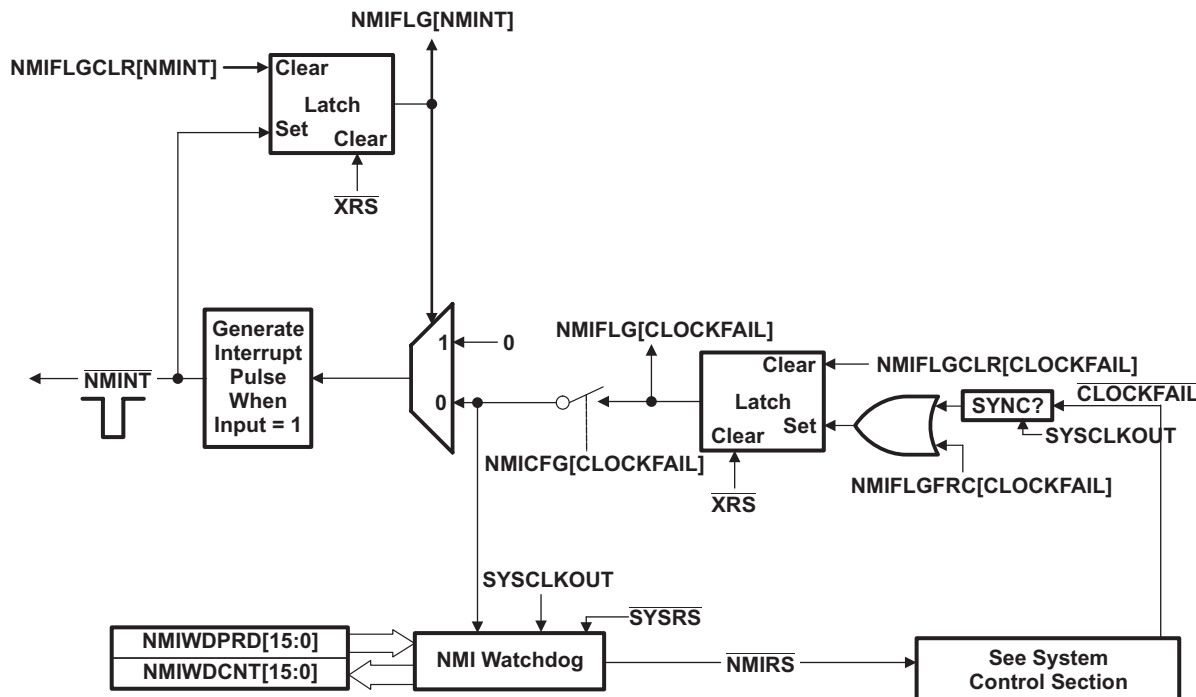


Figure 5-8. NMI-Watchdog

5.7.3.6 CPU-Watchdog Module

The CPU-watchdog module on the F28PLC8x device is similar to the one used on the 281x, 280x, and 283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this occurrence, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. [Figure 5-9](#) shows the various functional blocks within the watchdog module.

Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (that is, the watchdog counter does not change with the limp-mode clock).

NOTE

The CPU-watchdog is different from the NMI watchdog. The CPU-watchdog is the legacy watchdog that is present in all 28x devices.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the F28PLC8x device will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the device, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent the capacitor from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.

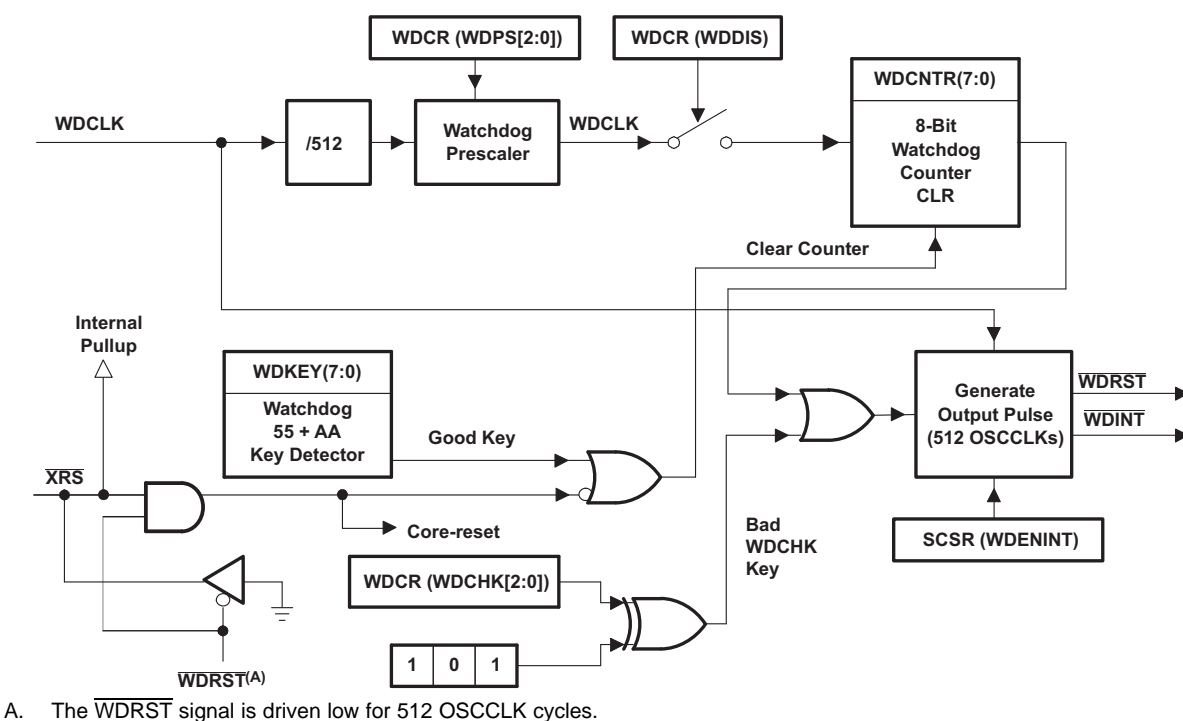


Figure 5-9. CPU-Watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The $\overline{\text{WDINT}}$ signal is fed to the low-power mode (LPM) block so that the signal can wake the device from STANDBY (if enabled). See [Section 5.7.3.7, Low-power Modes Block](#), for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the Peripheral Interrupt Expansion (PIE), to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

5.7.3.7 Low-power Modes Block

Table 5-8 summarizes the various modes.

Table 5-8. Low-power Modes

| MODE | LPMCR0(1:0) | OSCCLK | CLKIN | SYSCCLKOUT | EXIT ⁽¹⁾ |
|---------------------|-------------|--|-------|------------|--|
| IDLE | 00 | On | On | On | \overline{XRS} , CPU-watchdog interrupt, any enabled interrupt |
| STANDBY | 01 | On (CPU-watchdog still running) | Off | Off | \overline{XRS} , CPU-watchdog interrupt, GPIO Port A signal, debugger ⁽²⁾ |
| HALT ⁽³⁾ | 1X | Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.) | Off | Off | \overline{XRS} , GPIO Port A signal, debugger ⁽²⁾ , CPU-watchdog |

- (1) The Exit column lists which signals or under what conditions the low power mode is exited. A low signal, on any of the signals, exits the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low power mode.
- (2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
- (3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

- IDLE Mode:** This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.
- STANDBY Mode:** Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signals will wake the device in the GPIOLPMSEL register. The selected signals are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.
- HALT Mode:** CPU-watchdog, \overline{XRS} , and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed.

5.7.3.8 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the F28PLC8x device. [Table 5-9](#) lists the cycle times of various clocks.

Table 5-9. F28PLC8x Clock Table and Nomenclature

| | | MIN | NOM | MAX | UNIT |
|-----------------------|------------------------------|-------|---------------------|-----|------|
| SYSCLKOUT | $t_{c(SCO)}$, Cycle time | 11.11 | | 500 | ns |
| | Frequency | 2 | | 90 | MHz |
| LSPCLK ⁽¹⁾ | $t_{c(LCO)}$, Cycle time | 11.11 | 44.4 ⁽²⁾ | | ns |
| | Frequency | | 22.5 ⁽²⁾ | 90 | MHz |
| ADC clock | $t_{c(ADCCLK)}$, Cycle time | 22.22 | | | ns |
| | Frequency | | | 45 | MHz |

(1) Lower LSPCLK will reduce device power consumption.

(2) This value is the default reset value if SYSCLKOUT = 90 MHz.

Table 5-10. Device Clocking Requirements/Characteristics

| | | MIN | NOM | MAX | UNIT |
|---|--------------------------------|-------|--------|------|------|
| On-chip oscillator (X1/X2 pins) (Crystal/Resonator) | $t_{c(OSC)}$, Cycle time | 50 | | 200 | ns |
| | Frequency | 5 | | 20 | MHz |
| External oscillator/clock source (XCLKIN pin) — PLL Enabled | $t_{c(CI)}$, Cycle time (C8) | 33.3 | | 200 | ns |
| | Frequency | 5 | | 30 | MHz |
| External oscillator/clock source (XCLKIN pin) — PLL Disabled | $t_{c(CI)}$, Cycle time (C8) | 11.11 | | 250 | ns |
| | Frequency | 4 | | 90 | MHz |
| Limp mode SYSCLKOUT (with /2 enabled) | Frequency range | | 1 to 5 | | MHz |
| XCLKOUT | $t_{c(XCO)}$, Cycle time (C1) | 44.44 | | 2000 | ns |
| | Frequency | 0.5 | | 22.5 | MHz |
| PLL lock time ⁽¹⁾ | t_p | | | 1 | ms |

(1) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles. If the zero-pin internal oscillators (10 MHz) are used as the clock source, then the PLLLOCKPRD register must be written with a value of 10,000 (minimum).

Table 5-11. Internal Zero-Pin Oscillator (INTOSC1, INTOSC2) Characteristics

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|-----------|-----|--------|------|--------|
| Internal zero-pin oscillator 1 (INTOSC1) at 30°C ⁽¹⁾⁽²⁾ | Frequency | | 10.000 | | MHz |
| Internal zero-pin oscillator 2 (INTOSC2) at 30°C ⁽¹⁾⁽²⁾ | Frequency | | 10.000 | | MHz |
| Step size (coarse trim) | | | 55 | | kHz |
| Step size (fine trim) | | | 14 | | kHz |
| Temperature drift ⁽³⁾ | | | 3.03 | 4.85 | kHz/°C |
| Voltage (V _{DD}) drift ⁽³⁾ | | | 175 | | Hz/mV |

- (1) In order to achieve better oscillator accuracy (10 MHz ± 1% or better) than shown, refer to the *Oscillator Compensation Guide Application Report* ([SPRAB84](#)).
- (2) Frequency range ensured only when VREG is enabled, $\overline{\text{VREGEN}} = V_{\text{SS}}$.
- (3) Output frequency of the internal oscillators follows the direction of both the temperature gradient and voltage (V_{DD}) gradient. For example:
- Increase in temperature will cause the output frequency to increase per the temperature coefficient.
 - Decrease in voltage (V_{DD}) will cause the output frequency to decrease per the voltage coefficient.

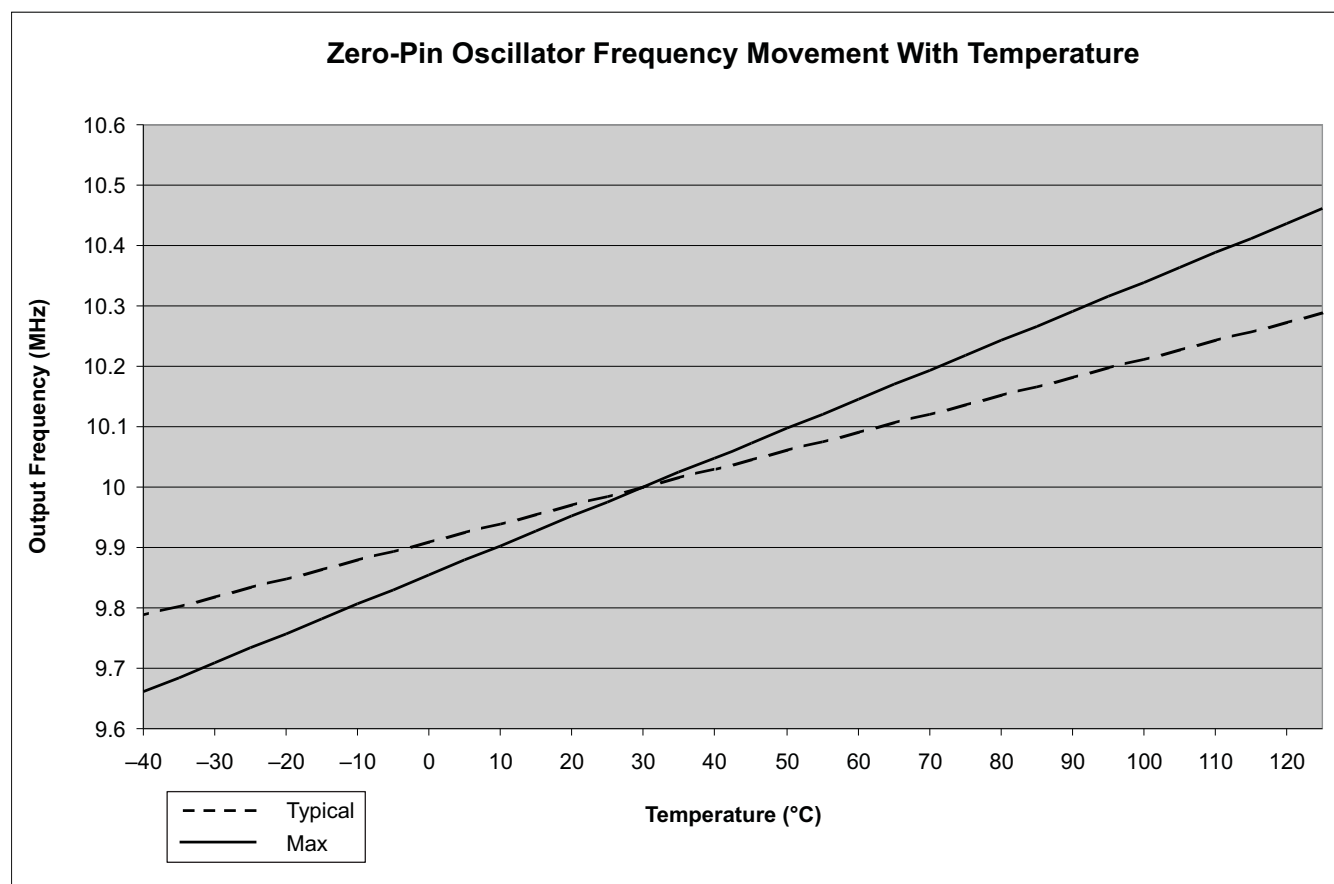


Figure 5-10. Zero-Pin Oscillator Frequency Movement With Temperature

5.7.3.9 Clock Requirements and Characteristics

Table 5-12. XCLKIN Timing Requirements - PLL Enabled

| NO. | | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| C9 | $t_{f(CI)}$ Fall time, XCLKIN | | 6 | ns |
| C10 | $t_{r(CI)}$ Rise time, XCLKIN | | 6 | ns |
| C11 | $t_{w(CIL)}$ Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$ | 45% | 55% | |
| C12 | $t_{w(CIH)}$ Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$ | 45% | 55% | |

Table 5-13. XCLKIN Timing Requirements - PLL Disabled

| NO. | | MIN | MAX | UNIT |
|-----|---|------------------|-----|------|
| C9 | $t_{f(CI)}$ Fall time, XCLKIN | Up to 20 MHz | 6 | ns |
| | | 20 MHz to 90 MHz | 2 | |
| C10 | $t_{r(CI)}$ Rise time, XCLKIN | Up to 20 MHz | 6 | ns |
| | | 20 MHz to 90 MHz | 2 | |
| C11 | $t_{w(CIL)}$ Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$ | 45% | 55% | |
| C12 | $t_{w(CIH)}$ Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$ | 45% | 55% | |

The possible configuration modes are shown in [Table 5-7](#).

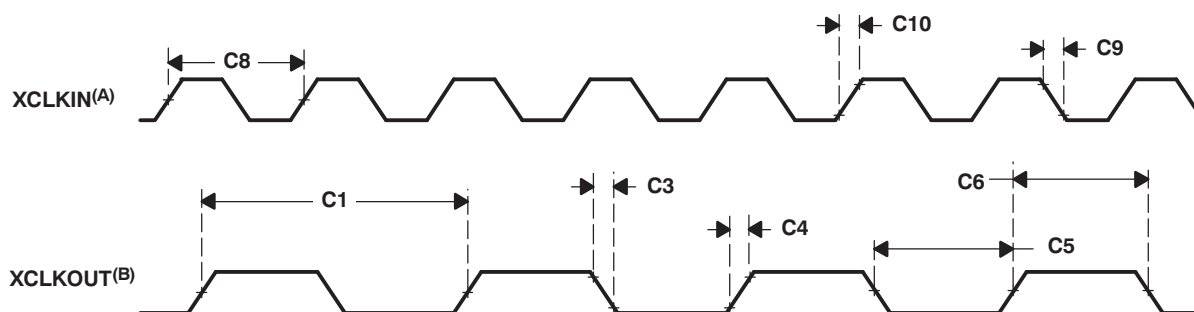
Table 5-14. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)⁽¹⁾⁽²⁾

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|--|-------|-------|------|
| C3 | $t_{f(XCO)}$ Fall time, XCLKOUT | | 5 | ns |
| C4 | $t_{r(XCO)}$ Rise time, XCLKOUT | | 5 | ns |
| C5 | $t_{w(XCOL)}$ Pulse duration, XCLKOUT low | H – 2 | H + 2 | ns |
| C6 | $t_{w(XCOH)}$ Pulse duration, XCLKOUT high | H – 2 | H + 2 | ns |

(1) A load of 40 pF is assumed for these parameters.

(2) $H = 0.5t_{c(XCO)}$



- A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.
- B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 5-11. Clock Timing

5.7.4 Peripherals

5.7.4.1 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on F280x/F2833x. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions. [Figure 5-12](#) shows the interaction of the analog module with the rest of the F28PLCx system.

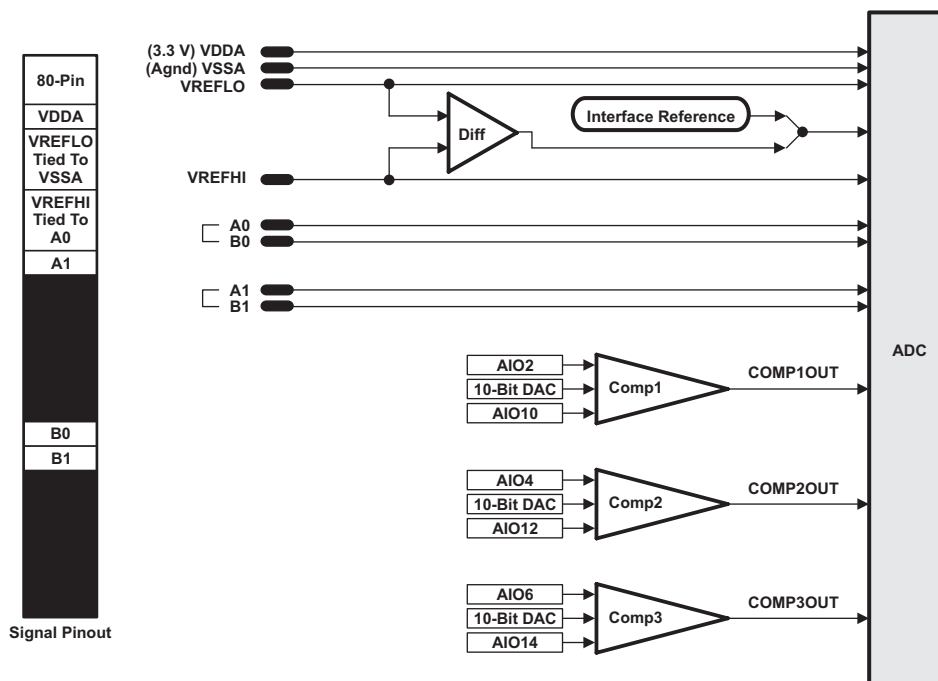


Figure 5-12. Analog Pin Configurations

5.7.4.1.1 Analog-to-Digital Converter

5.7.4.1.1.1 Features

The core of the ADC contains a single 12-bit converter fed by two sample-and-hold circuits. The sample-and-hold circuits can be sampled simultaneously or sequentially. These, in turn, are fed by a total of up to 16 analog input channels. The converter can be configured to run with an internal bandgap reference to create true-voltage based conversions or with a pair of external voltage references (V_{REFHI}/V_{REFLO}) to create ratiometric-based conversions.

Contrary to previous ADC types, this ADC is not sequencer-based. The user can easily create a series of conversions from a single trigger. However, the basic principle of operation is centered around the configurations of individual conversions, called SOC, or Start-Of-Conversions.

Functions of the ADC module include:

- 12-bit ADC core with built-in dual sample-and-hold (S/H)
- Simultaneous sampling or sequential sampling modes
- Full range analog input: 0 V to 3.3 V fixed, or V_{REFHI}/V_{REFLO} ratiometric. The digital value of the input analog voltage is derived by:
 - Internal Reference ($V_{REFLO} = V_{SSA}$. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \leq 0 \text{ V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{3.3} \quad \text{when } 0 \text{ V} < \text{input} < 3.3 \text{ V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \geq 3.3 \text{ V}$$

- External Reference (V_{REFHI}/V_{REFLO} connected to external references. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \leq 0 \text{ V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}} \quad \text{when } 0 \text{ V} < \text{input} < V_{REFHI}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \geq V_{REFHI}$$

- Up to 16-channel, multiplexed inputs
- 16 SOC, configurable for trigger, sample window, and channel
- 16 result registers (individually addressable) to store conversion values
- Multiple trigger sources
 - S/W – software immediate start
 - ePWM 1, ePWM2
 - GPIO XINT2
 - CPU Timer 0, CPU Timer 1, CPU Timer 2
 - ADCINT1, ADCINT2
- 9 flexible PIE interrupts, can configure interrupt request after any conversion

Table 5-15. ADC Configuration and Control Registers

| REGISTER NAME | ADDRESS | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION |
|---------------------------|-----------------|------------|------------------|--|
| ADCCTL1 | 0x7100 | 1 | Yes | Control 1 Register |
| ADCCTL2 | 0x7101 | 1 | Yes | Control 2 Register |
| ADCINTFLG | 0x7104 | 1 | No | Interrupt Flag Register |
| ADCINTFLGCLR | 0x7105 | 1 | No | Interrupt Flag Clear Register |
| ADCINTOVF | 0x7106 | 1 | No | Interrupt Overflow Register |
| ADCINTOVFCLR | 0x7107 | 1 | No | Interrupt Overflow Clear Register |
| INTSEL1N2 | 0x7108 | 1 | Yes | Interrupt 1 and 2 Selection Register |
| INTSEL3N4 | 0x7109 | 1 | Yes | Interrupt 3 and 4 Selection Register |
| INTSEL5N6 | 0x710A | 1 | Yes | Interrupt 5 and 6 Selection Register |
| INTSEL7N8 | 0x710B | 1 | Yes | Interrupt 7 and 8 Selection Register |
| INTSEL9N10 | 0x710C | 1 | Yes | Interrupt 9 Selection Register (reserved Interrupt 10 Selection) |
| SOCPRCTL | 0x7110 | 1 | Yes | SOC Priority Control Register |
| ADCSAMPLEMODE | 0x7112 | 1 | Yes | Sampling Mode Register |
| ADCINTSOCSEL1 | 0x7114 | 1 | Yes | Interrupt SOC Selection 1 Register (for 8 channels) |
| ADCINTSOCSEL2 | 0x7115 | 1 | Yes | Interrupt SOC Selection 2 Register (for 8 channels) |
| ADCSOCFLG1 | 0x7118 | 1 | No | SOC Flag 1 Register (for 16 channels) |
| ADCSOCFRC1 | 0x711A | 1 | No | SOC Force 1 Register (for 16 channels) |
| ADCSOCOVF1 | 0x711C | 1 | No | SOC Overflow 1 Register (for 16 channels) |
| ADCSOCOVFCLR1 | 0x711E | 1 | No | SOC Overflow Clear 1 Register (for 16 channels) |
| ADCSOC0CTL to ADCSOC15CTL | 0x7120 – 0x712F | 1 | Yes | SOC0 Control Register to SOC15 Control Register |
| ADCREFTTRIM | 0x7140 | 1 | Yes | Reference Trim Register |
| ADCOFFTRIM | 0x7141 | 1 | Yes | Offset Trim Register |
| COMPHYSTCTL | 0x714C | 1 | Yes | Comparator Hysteresis Control Register |
| ADCREV | 0x714F | 1 | No | Revision Register |

Table 5-16. ADC Result Registers (Mapped to PF0)

| REGISTER NAME | ADDRESS | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION |
|---------------------------|---------------|------------|------------------|---|
| ADCRESULT0 to ADCRESULT15 | 0xB00 – 0xB0F | 1 | No | ADC Result 0 Register to ADC Result 15 Register |

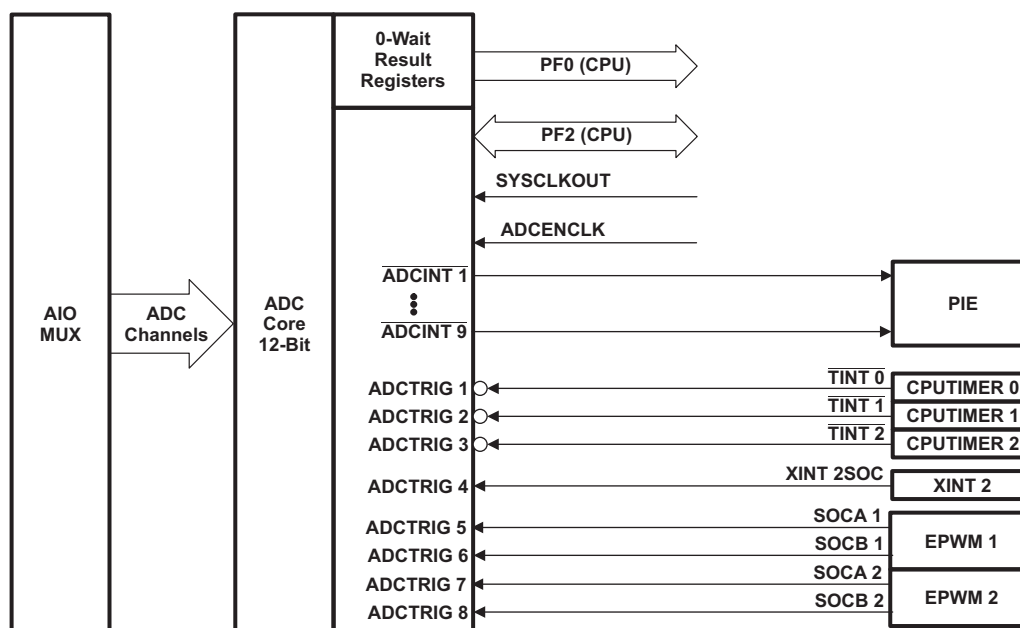


Figure 5-13. ADC Connections

ADC Connections if the ADC is Not Used

TI recommends that the connections for the analog power pins be kept, even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DDA} – Connect to V_{DDIO}
- V_{SSA} – Connect to V_{SS}
- V_{REFLO} – Connect to V_{SS}
- $ADCINAn$, $ADCINBn$, V_{REFHI} – Connect to V_{SSA}

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground (V_{SSA}).

NOTE: Unused ADCIN pins that are multiplexed with AIO function should not be directly connected to analog ground. They should be grounded through a 1-k Ω resistor. Grounding through a 1-k Ω resistor is to prevent an errant code from configuring these pins as AIO outputs and driving grounded pins to a logic-high state.

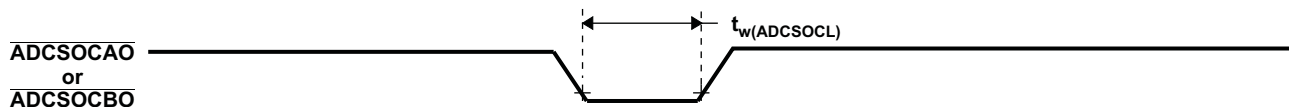
When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

5.7.4.1.1.2 ADC Start-of-Conversion Electrical Data/Timing

Table 5-17. External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|------------------|---|----------------|-----|--------|
| $t_{w(ADCSOCL)}$ | Pulse duration, $\overline{ADCSOCxO}$ low | $32t_{c(HCO)}$ | | cycles |


Figure 5-14. $\overline{ADCSOCxO}$ or $\overline{ADCSOCBO}$ Timing

5.7.4.1.1.3 ADC Electrical Data/Timing

Table 5-18. ADC Electrical Characteristics

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|--|-------------|------|-------------|------------|
| DC SPECIFICATIONS | | | | | |
| Resolution | | 12 | | | Bits |
| ADC clock | 90-MHz device | 0.001 | | 45 | MHz |
| Sample Window | | 7 | | 64 | ADC Clocks |
| ACCURACY | | | | | |
| INL (Integral nonlinearity) ⁽¹⁾ | | –4 | | 4 | LSB |
| DNL (Differential nonlinearity), no missing codes | | –1 | | 1.5 | LSB |
| Offset error ⁽²⁾ | Executing a single self-recalibration | –20 | | 20 | LSB |
| | Executing periodic self-recalibration ⁽³⁾ | –4 | | 4 | |
| Overall gain error with internal reference | | –60 | | 60 | LSB |
| Overall gain error with external reference | | –40 | | 40 | LSB |
| Channel-to-channel offset variation | | –4 | | 4 | LSB |
| Channel-to-channel gain variation | | –4 | | 4 | LSB |
| ADC temperature coefficient with internal reference | | | –50 | | ppm/°C |
| ADC temperature coefficient with external reference | | | –20 | | ppm/°C |
| V_{REFLO} | | | –100 | | μA |
| V_{REFHI} | | | 100 | | μA |
| ANALOG INPUT | | | | | |
| Analog input voltage with internal reference | | 0 | | 3.3 | V |
| Analog input voltage with external reference | | V_{REFLO} | | V_{REFHI} | V |
| V_{REFLO} input voltage ⁽⁴⁾ | | V_{SSA} | | 0.66 | V |
| V_{REFHI} input voltage ⁽⁵⁾ | | 2.64 | | V_{DDA} | V |
| | with $V_{REFLO} = V_{SSA}$ | 1.98 | | V_{DDA} | |
| Input capacitance | | | 5 | | pF |
| Input leakage current | | | ±2 | | μA |

(1) INL will degrade when the ADC input voltage goes above V_{DDA} .

(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and $V_{REFHI} - V_{REFLO}$ for external reference.

(3) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error.

(4) V_{REFLO} is always connected to V_{SSA} on the 80-pin PN device.

(5) V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes. Since V_{REFHI} is tied to ADCINA0 on the 80-pin PN device, the input signal on ADCINA0 must not exceed V_{DDA} .

Table 5-19. ADC Power Modes

| ADC OPERATING MODE | CONDITIONS | I _{DDA} | UNITS |
|-------------------------------|--|------------------|-------|
| Mode A – Operating Mode | ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 1) | 16 | mA |
| Mode B – Quick Wake Mode | ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 0) | 4 | mA |
| Mode C – Comparator-Only Mode | ADC Clock Enabled Bandgap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0) | 1.5 | mA |
| Mode D – Off Mode | ADC Clock Enabled Bandgap On (ADCBGPWD = 0) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0) | 0.075 | mA |

5.7.4.1.1.3.1 Internal Temperature Sensor**Table 5-20. Temperature Sensor Coefficient**

| PARAMETER ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|--------------------------|---|-----|------------------------|-----|--------|
| T _{SLOPE} | Degrees C of temperature movement per measured ADC LSB change of the temperature sensor | | 0.18 ⁽²⁾⁽³⁾ | | °C/LSB |
| T _{OFFSET} | ADC output at 0°C of the temperature sensor | | 1750 | | LSB |

- (1) The temperature sensor slope and offset are given in terms of ADC LSBs using the internal reference of the ADC. Values must be adjusted accordingly in external reference mode to the external reference voltage.
- (2) ADC temperature coefficient is accounted for in this specification
- (3) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.

5.7.4.1.1.3.2 ADC Power-Up Control Bit Timing

Table 5-21. ADC Power-Up Delays

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|--|-----|-----|------|
| $t_{d(PWD)}$ | Delay time for the ADC to be stable after power up | | 1 | ms |

(1) Timings maintain compatibility to the ADC module. The F28PLCx ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.

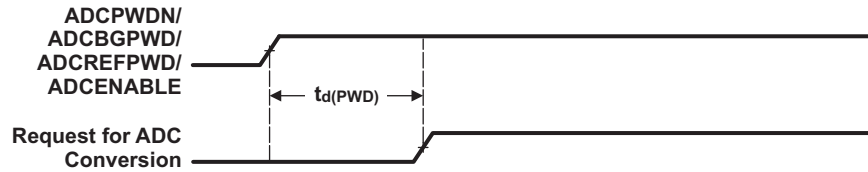
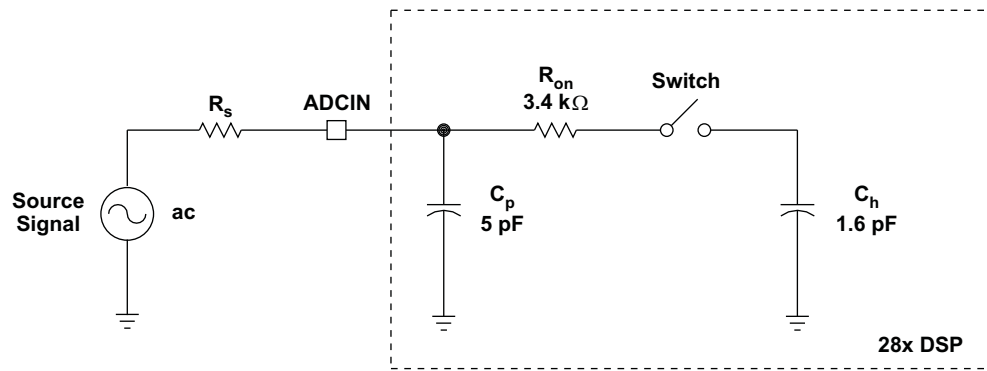


Figure 5-15. ADC Conversion Timing



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 3.4 kΩ

Sampling Capacitor (C_h): 1.6 pF

Parasitic Capacitance (C_p): 5 pF

Source Resistance (R_s): 50 Ω

Figure 5-16. ADC Input Impedance Model

5.7.4.1.1.3.3 ADC Sequential and Simultaneous Timings

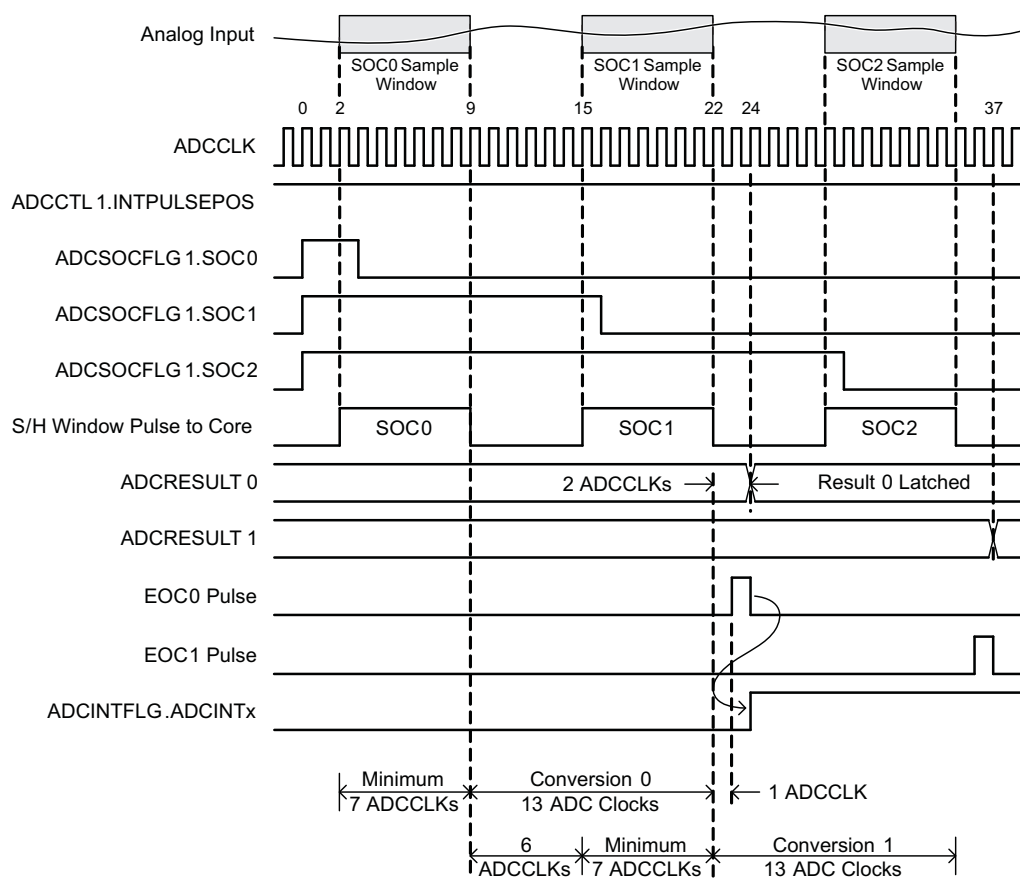


Figure 5-17. Timing Example for Sequential Mode / Late Interrupt Pulse

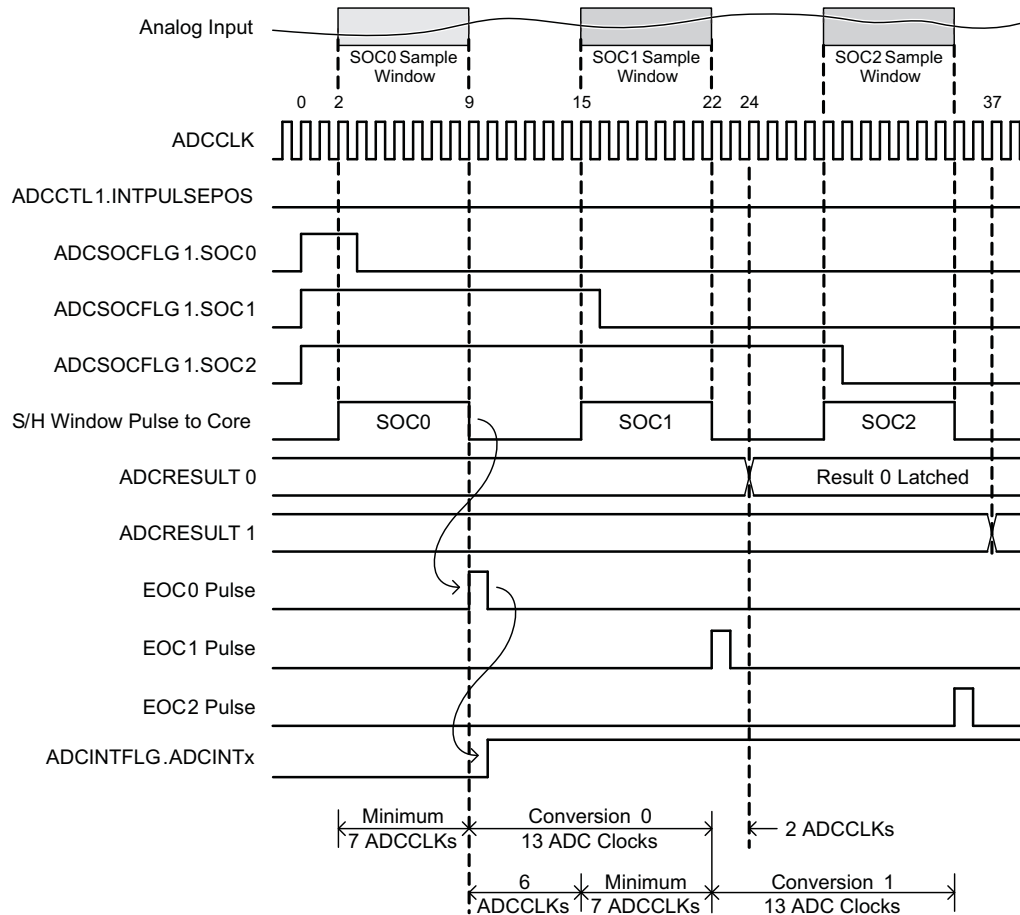


Figure 5-18. Timing Example for Sequential Mode / Early Interrupt Pulse

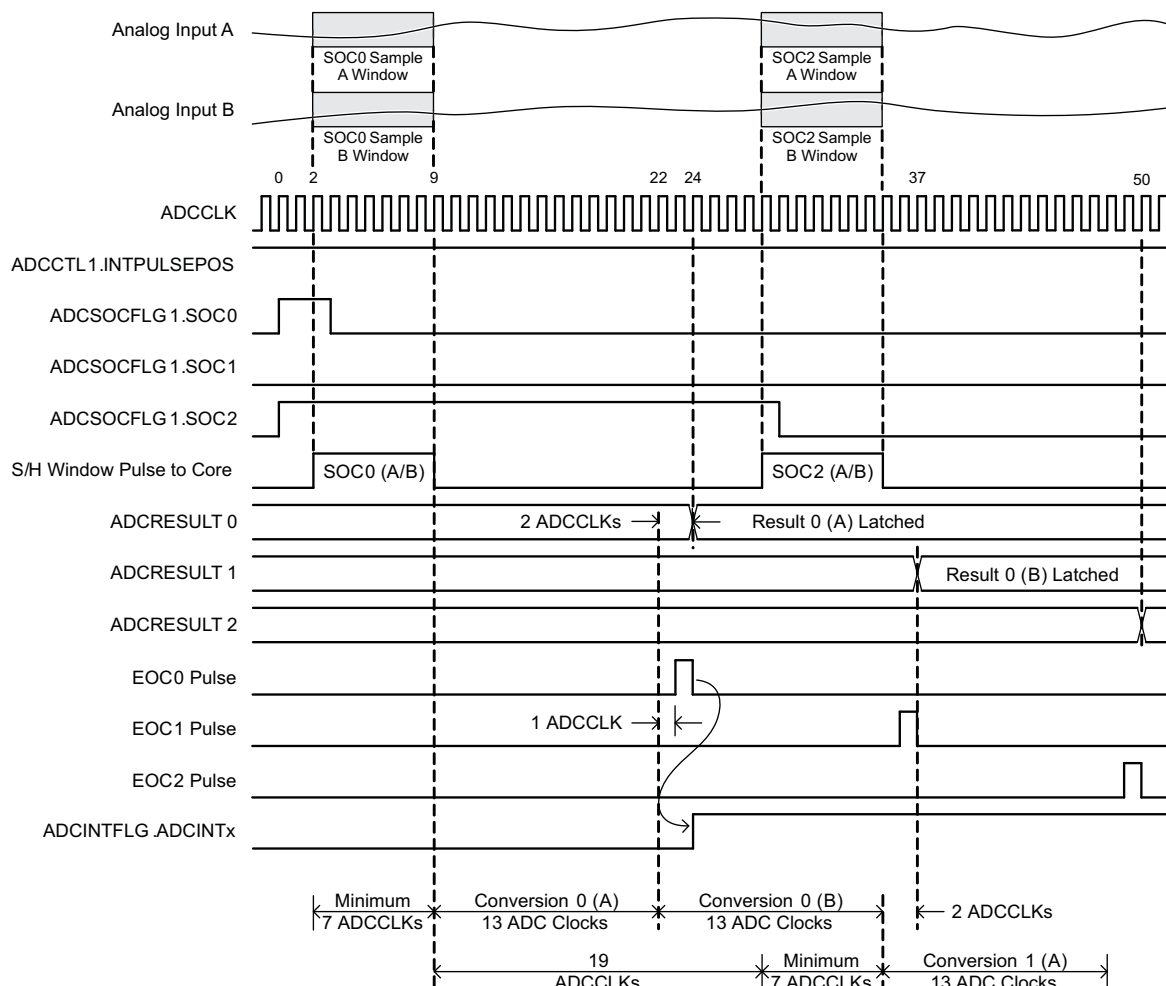


Figure 5-19. Timing Example for Simultaneous Mode / Late Interrupt Pulse

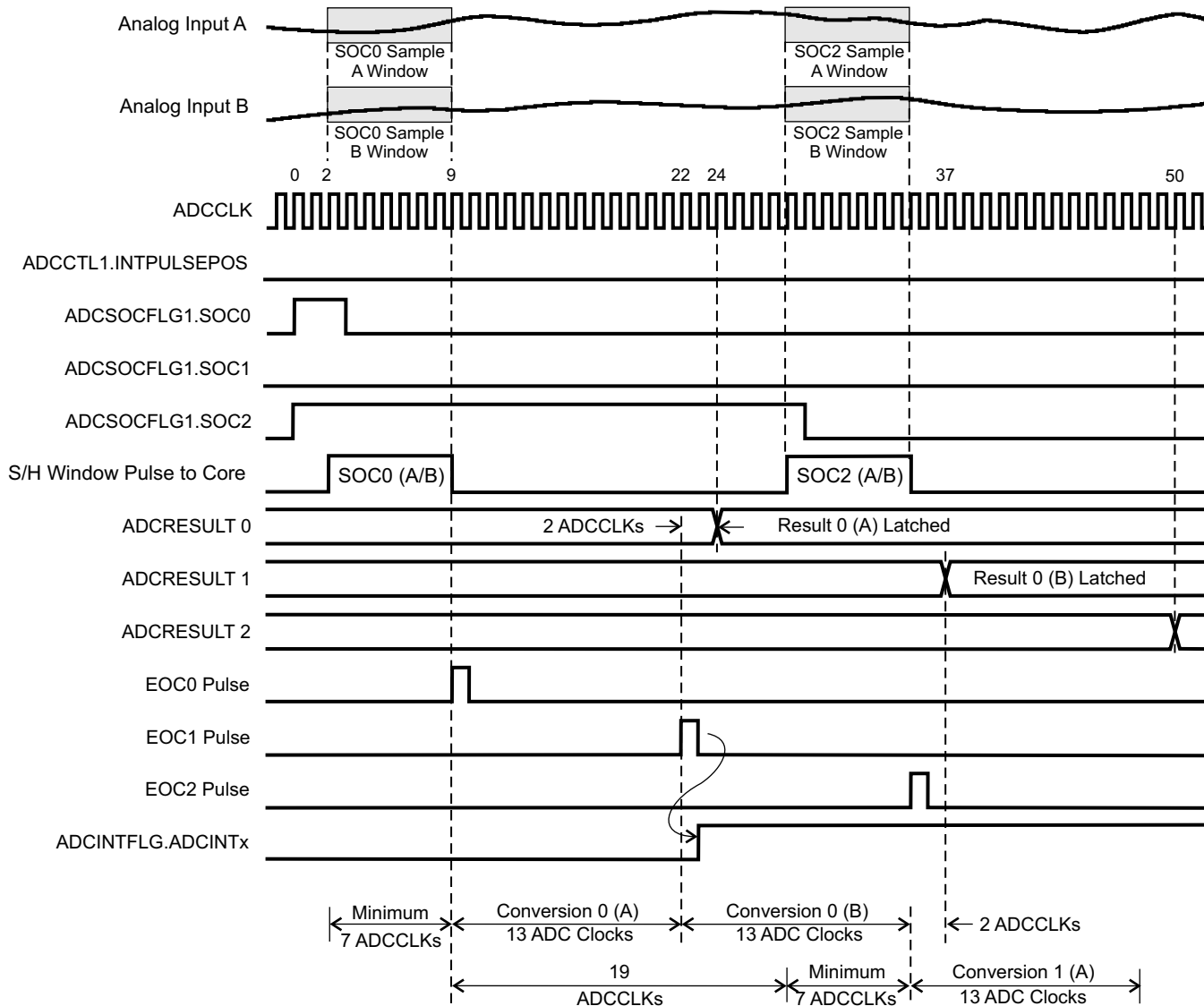


Figure 5-20. Timing Example for Simultaneous Mode / Early Interrupt Pulse

5.7.4.1.2 ADC MUX

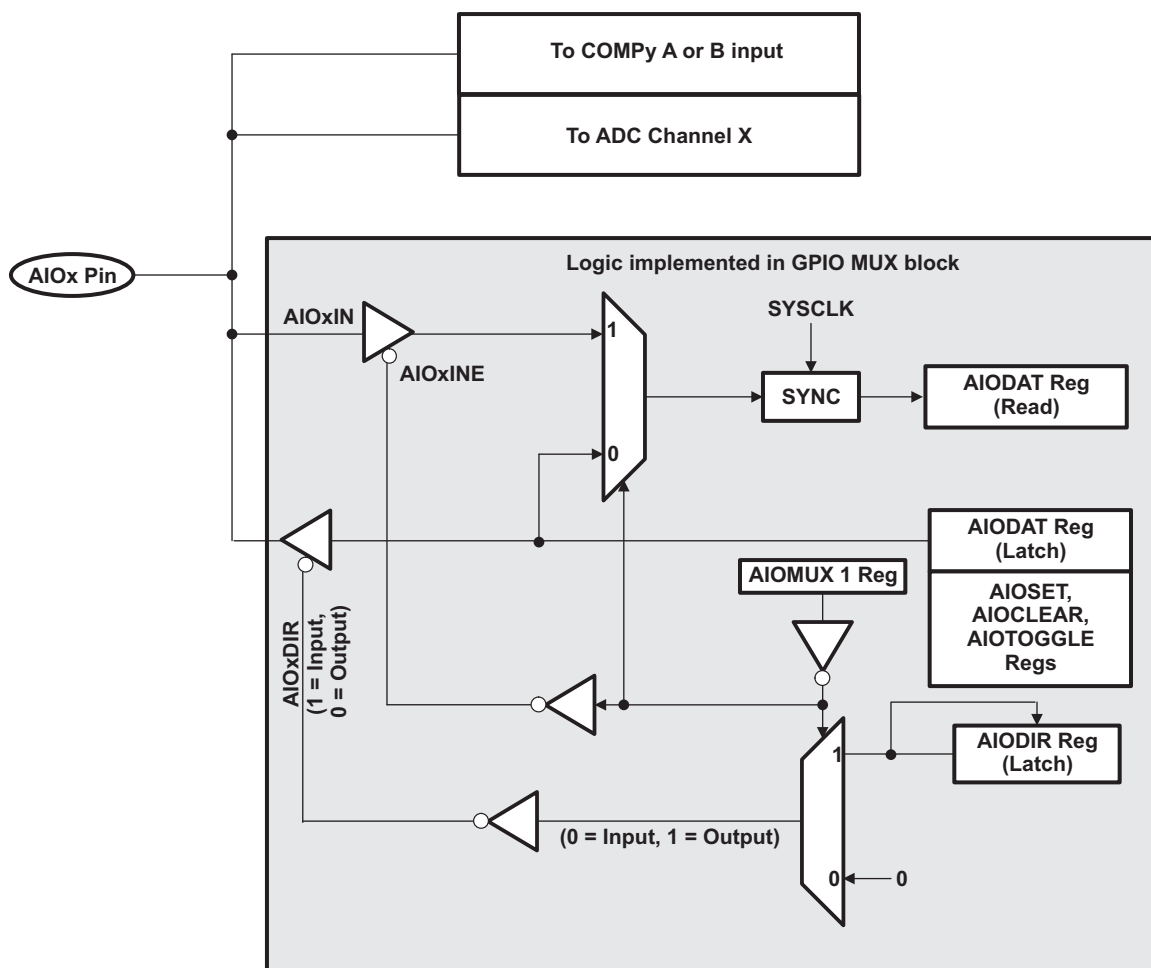


Figure 5-21. AlOx Pin Multiplexing

The ADC channel and Comparator functions are always available. The digital I/O function is available only when the respective bit in the AIOMUX1 register is 0. In this mode, reading the AIODAT register reflects the actual pin state.

The digital I/O function is disabled when the respective bit in the AIOMUX1 register is 1. In this mode, reading the AIODAT register reflects the output latch of the AIODAT register and the input digital I/O buffer is disabled to prevent analog signals from generating noise.

On reset, the digital function is disabled. If the pin is used as an analog input, users should keep the AIO function disabled for that pin.

5.7.4.1.3 Comparator Block

Figure 5-22 shows the interaction of the Comparator modules with the rest of the system.

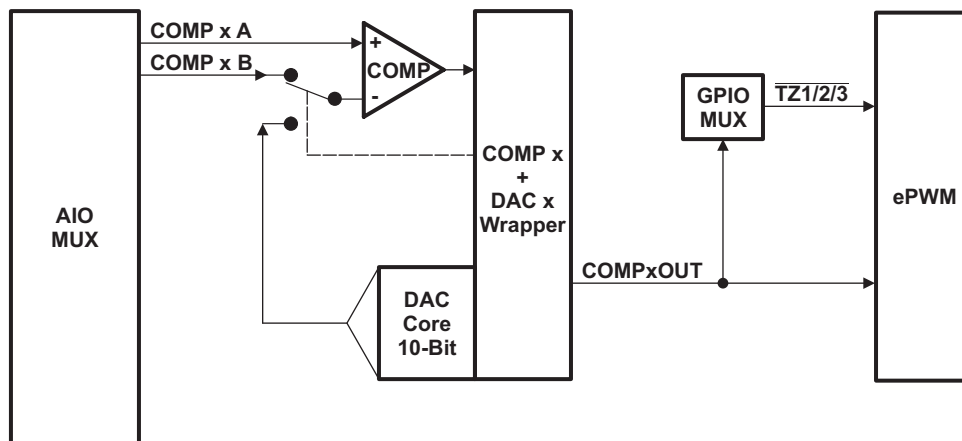


Figure 5-22. Comparator Block Diagram

Table 5-22 lists the Comparator Control Registers.

Table 5-22. Comparator Control Registers

| REGISTER NAME | COMP1 ADDRESS | COMP2 ADDRESS | COMP3 ADDRESS | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION |
|-------------------|---------------|---------------|---------------|------------|------------------|--|
| COMPCTL | 0x6400 | 0x6420 | 0x6440 | 1 | Yes | Comparator Control Register |
| COMPSTS | 0x6402 | 0x6422 | 0x6442 | 1 | No | Comparator Status Register |
| DACCTL | 0x6404 | 0x6424 | 0x6444 | 1 | Yes | DAC Control Register |
| DACVAL | 0x6406 | 0x6426 | 0x6446 | 1 | No | DAC Value Register |
| RAMPMAXREF_ACTIVE | 0x6408 | 0x6428 | 0x6448 | 1 | No | Ramp Generator Maximum Reference (Active) Register |
| RAMPMAXREF_SHDW | 0x640A | 0x642A | 0x644A | 1 | No | Ramp Generator Maximum Reference (Shadow) Register |
| RAMPDECVAL_ACTIVE | 0x640C | 0x642C | 0x644C | 1 | No | Ramp Generator Decrement Value (Active) Register |
| RAMPDECVAL_SHDW | 0x640E | 0x642E | 0x644E | 1 | No | Ramp Generator Decrement Value (Shadow) Register |
| RAMPSTS | 0x6410 | 0x6430 | 0x6450 | 1 | No | Ramp Generator Status Register |

5.7.4.1.3.1 On-Chip Comparator/DAC Electrical Data/Timing

Table 5-23. Electrical Characteristics of the Comparator/DAC

| CHARACTERISTIC | MIN | TYP | MAX | UNITS |
|---|-----|---------------------|-----|-------|
| Comparator | | | | |
| Comparator Input Range | | $V_{SSA} - V_{DDA}$ | | V |
| Comparator response time to PWM Trip Zone (Async) | | 30 | | ns |
| Input Offset | | ± 5 | | mV |
| Input Hysteresis ⁽¹⁾ | | 35 | | mV |
| DAC | | | | |
| DAC Output Range | | $V_{SSA} - V_{DDA}$ | | V |
| DAC resolution | | 10 | | bits |
| DAC settling time | | See Figure 5-23 | | |
| DAC Gain | | -1.5% | | |
| DAC Offset | | 10 | | mV |
| Monotonic | | Yes | | |
| INL | | ± 3 | | LSB |

- (1) Hysteresis on the comparator inputs is achieved with a Schmidt trigger configuration, which results in an effective 100-k Ω feedback resistance between the output of the comparator and the non-inverting input of the comparator.

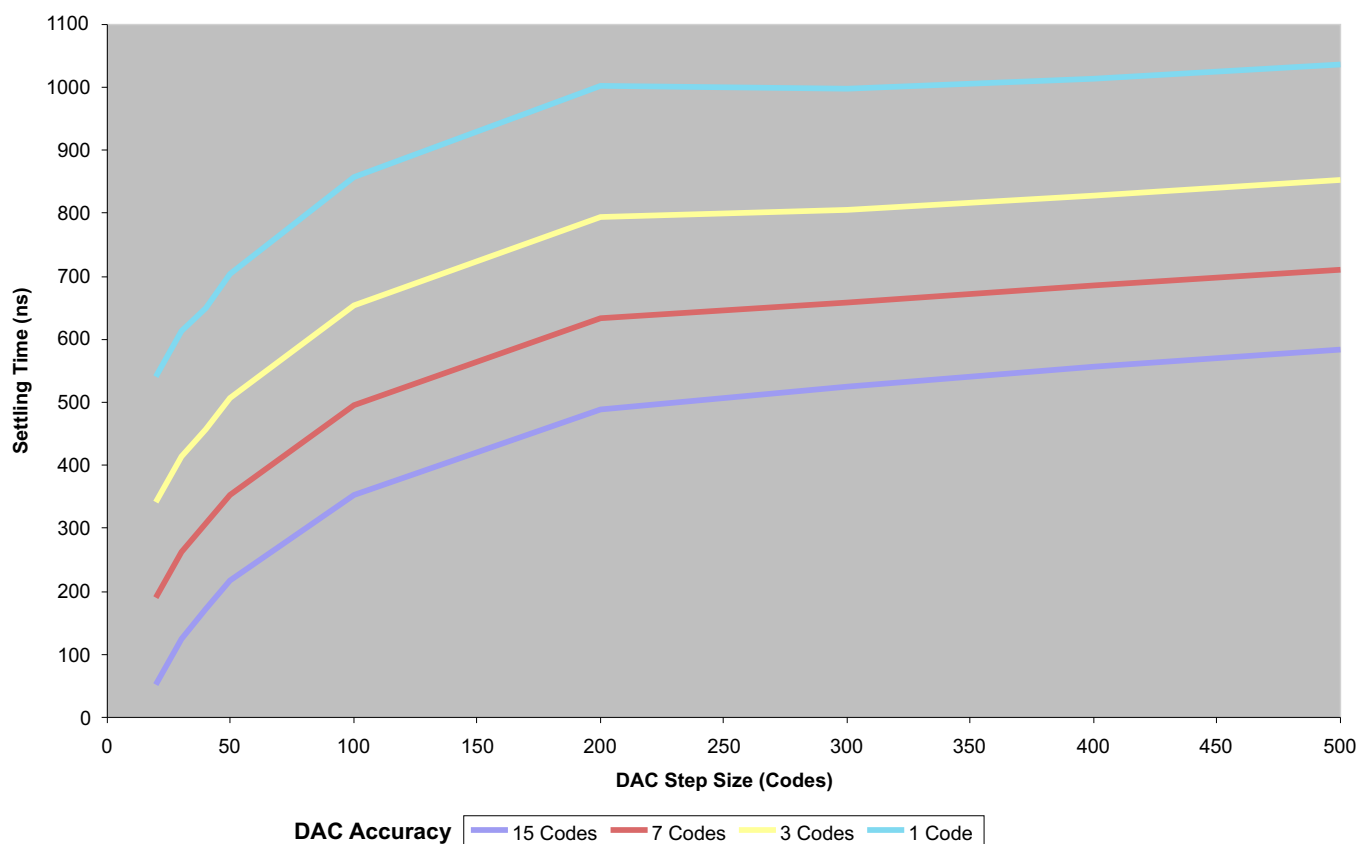


Figure 5-23. DAC Settling Time

5.7.4.2 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ± 1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,
$$N = \frac{(\text{SINAD} - 1.76)}{6.02}$$
 it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

5.7.4.3 Serial Peripheral Interface Module

The device includes the four-pin SPI module. Two SPI modules are available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the device and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
 - SPISOMI: SPI slave-output/master-input pin
 - SPISIMO: SPI slave-input/master-output pin
 - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
 - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave
Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR} = 0, 1, 2$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bi-directional 3 wire SPI mode support
- Audio data receive support via $\overline{\text{SPISTE}}$ inversion

The SPI port operation is configured and controlled by the registers listed in [Table 5-24](#) and [Table 5-25](#).

Table 5-24. SPI-A Registers

| NAME | ADDRESS | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION ⁽¹⁾ |
|----------|---------|------------|------------------|---|
| SPICCR | 0x7040 | 1 | No | SPI-A Configuration Control Register |
| SPICTL | 0x7041 | 1 | No | SPI-A Operation Control Register |
| SPISTS | 0x7042 | 1 | No | SPI-A Status Register |
| SPIBRR | 0x7044 | 1 | No | SPI-A Baud Rate Register |
| SPIRXEMU | 0x7046 | 1 | No | SPI-A Receive Emulation Buffer Register |
| SPIRXBUF | 0x7047 | 1 | No | SPI-A Serial Input Buffer Register |
| SPITXBUF | 0x7048 | 1 | No | SPI-A Serial Output Buffer Register |
| SPIDAT | 0x7049 | 1 | No | SPI-A Serial Data Register |
| SPIFFTX | 0x704A | 1 | No | SPI-A FIFO Transmit Register |
| SPIFFRX | 0x704B | 1 | No | SPI-A FIFO Receive Register |
| SPIFFCT | 0x704C | 1 | No | SPI-A FIFO Control Register |
| SPIPRI | 0x704F | 1 | No | SPI-A Priority Control Register |

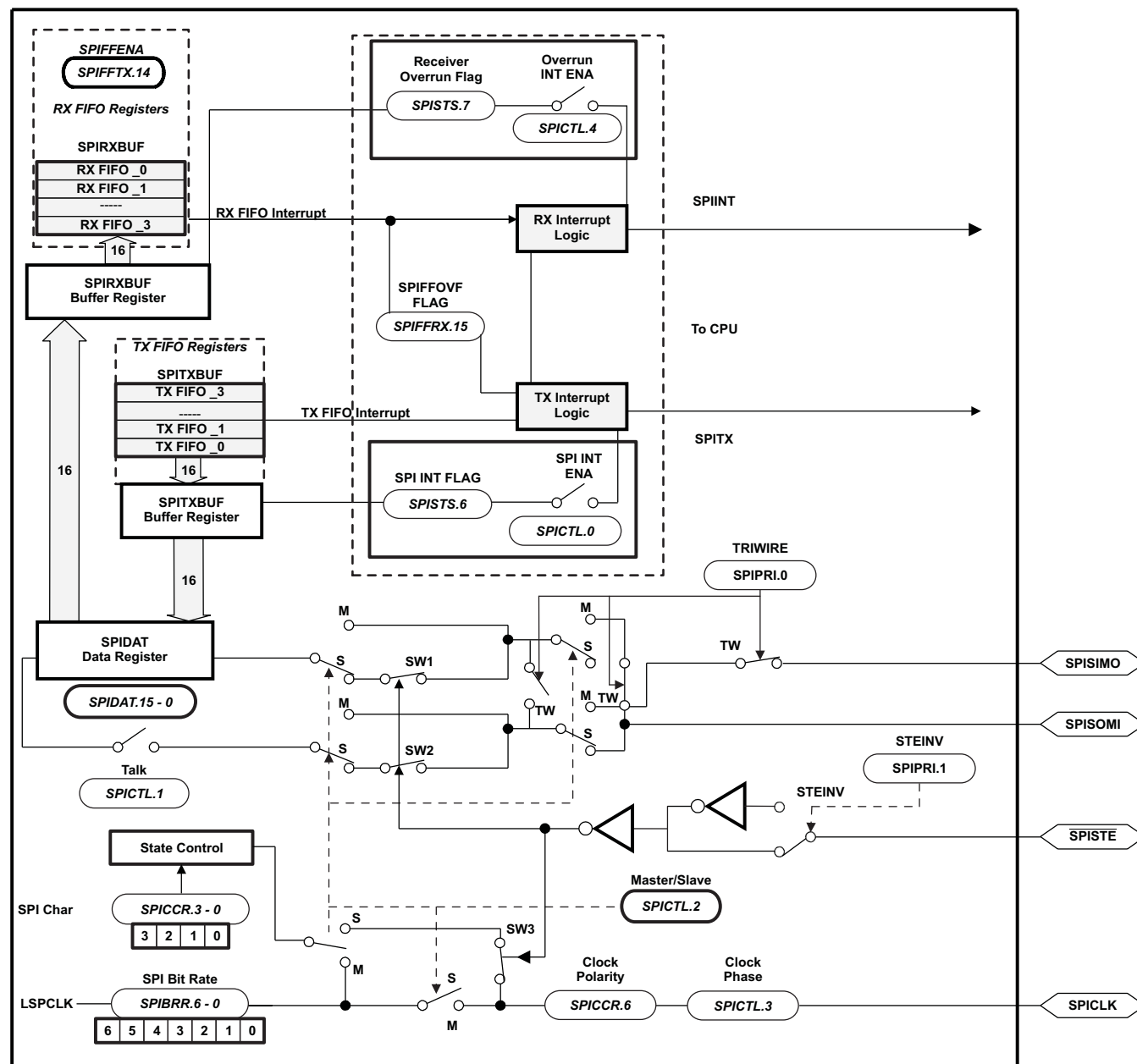
(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 5-25. SPI-B Registers

| NAME | ADDRESS | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION ⁽¹⁾ |
|----------|---------|------------|------------------|---|
| SPICCR | 0x7740 | 1 | No | SPI-B Configuration Control Register |
| SPICTL | 0x7741 | 1 | No | SPI-B Operation Control Register |
| SPISTS | 0x7742 | 1 | No | SPI-B Status Register |
| SPIBRR | 0x7744 | 1 | No | SPI-B Baud Rate Register |
| SPIRXEMU | 0x7746 | 1 | No | SPI-B Receive Emulation Buffer Register |
| SPIRXBUF | 0x7747 | 1 | No | SPI-B Serial Input Buffer Register |
| SPITXBUF | 0x7748 | 1 | No | SPI-B Serial Output Buffer Register |
| SPIDAT | 0x7749 | 1 | No | SPI-B Serial Data Register |
| SPIFFTX | 0x774A | 1 | No | SPI-B FIFO Transmit Register |
| SPIFFRX | 0x774B | 1 | No | SPI-B FIFO Receive Register |
| SPIFFCT | 0x774C | 1 | No | SPI-B FIFO Control Register |
| SPIPRI | 0x774F | 1 | No | SPI-B Priority Control Register |

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 5-24 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 5-24. SPI Module Block Diagram (Slave Mode)

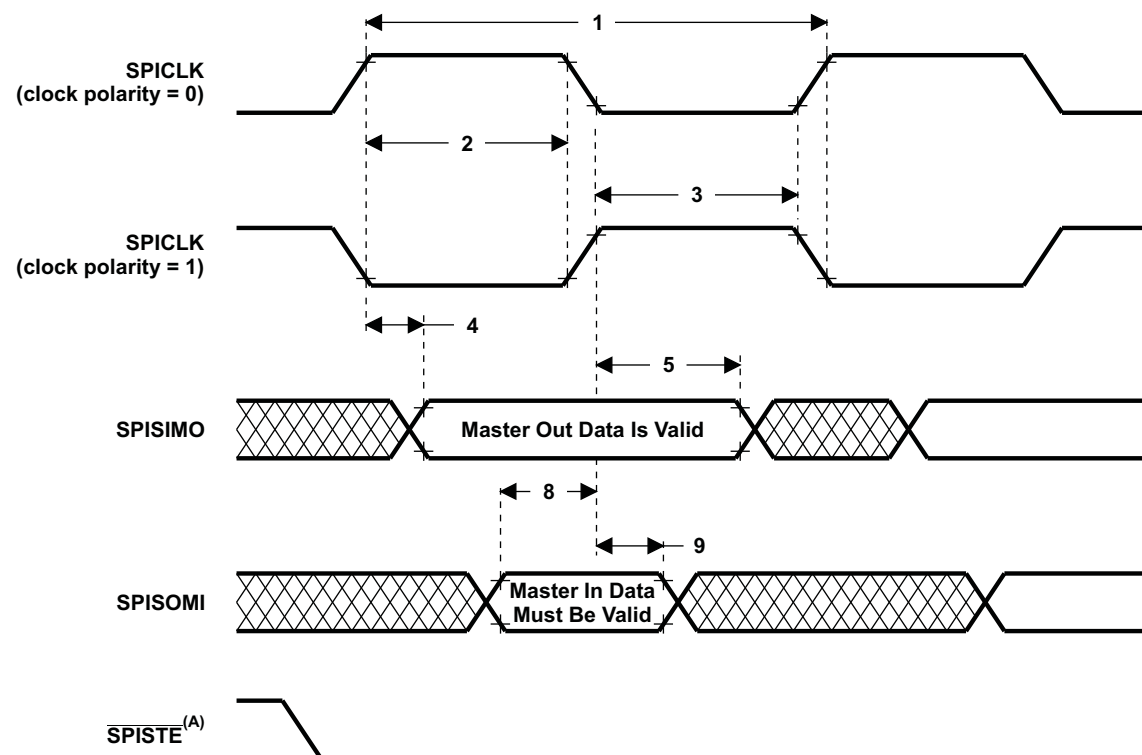
5.7.4.3.1 SPI Master Mode Electrical Data/Timing

Table 5-26 lists the master mode timing (clock phase = 0) and Table 5-27 lists the master mode timing (clock phase = 1). Figure 5-25 and Figure 5-26 show the timing waveforms.

Table 5-26. SPI Master Mode External Timing (Clock Phase = 0)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

| NO. | | | SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2 | | SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3 | | UNIT |
|-----|----------------------|---|---|------------------|--|----------------------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | $4t_{c(LCO)}$ | $128t_{c(LCO)}$ | $5t_{c(LCO)}$ | $127t_{c(LCO)}$ | ns |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$ | |
| 3 | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$ | |
| 4 | $t_{d(SPCH-SIMO)M}$ | Delay time, SPICLK high to SPISIMO valid (clock polarity = 0) | | 10 | | 10 | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPICLK low to SPISIMO valid (clock polarity = 1) | | 10 | | 10 | |
| 5 | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | | |
| 8 | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 26 | | 26 | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 26 | | 26 | | |
| 9 | $t_{v(SPCL-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0) | $0.25t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | | ns |
| | $t_{v(SPCH-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1) | $0.25t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | | |

- (1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
- (2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
- (3) $t_{c(LCO)}$ = LSPCLK cycle time
- (4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
- (5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).



- A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{\text{C(SPC)}}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{\text{C(SPC)}}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-25. SPI Master Mode External Timing (Clock Phase = 0)

Table 5-27. SPI Master Mode External Timing (Clock Phase = 1)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

| NO. | | | SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2 | | SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3 | | UNIT |
|-----|----------------------|--|---|------------------|--|----------------------------------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | $4t_{c(LCO)}$ | $128t_{c(LCO)}$ | $5t_{c(LCO)}$ | $127t_{c(LCO)}$ | ns |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LCO)}$ | |
| 3 | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | $0.5t_{c(SPC)M}$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LCO)}$ | |
| 6 | $t_{su(SIMO-SPCH)M}$ | Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{su(SIMO-SPCL)M}$ | Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | |
| 7 | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | |
| 10 | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | 26 | | 26 | | ns |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | 26 | | 26 | | |
| 11 | $t_{v(SPCH-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | $0.25t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | ns |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | $0.25t_{c(SPC)M} - 10$ | | $0.5t_{c(SPC)M} - 10$ | | |

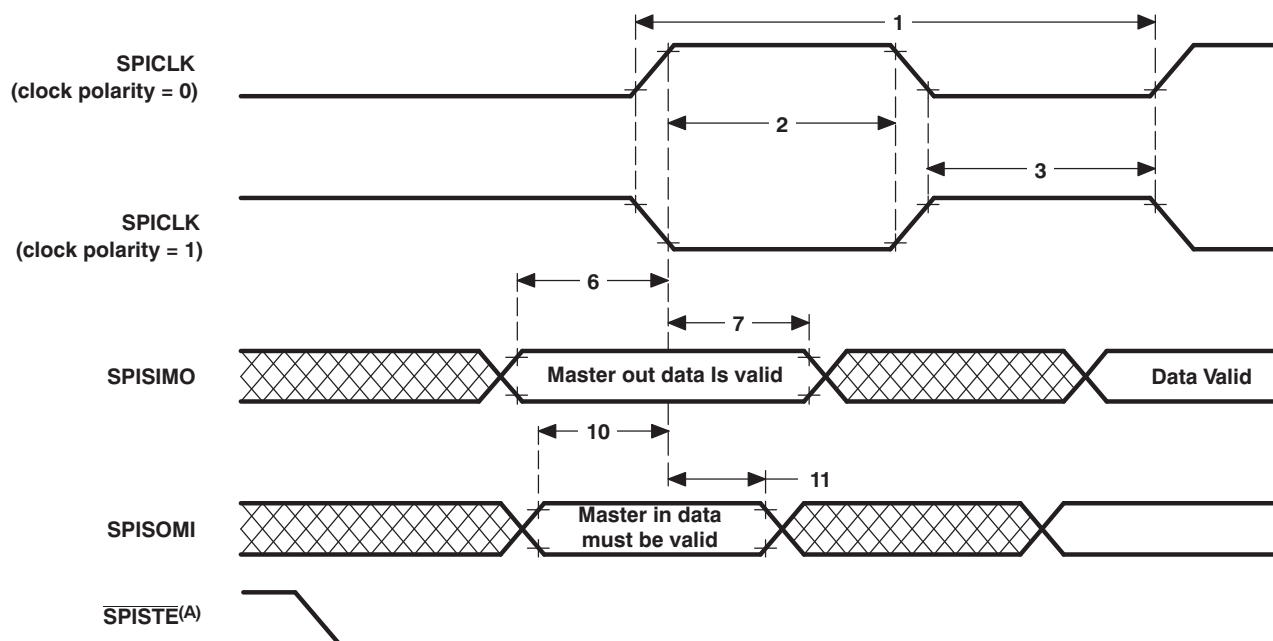
(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.

(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)

(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.

(4) $t_{c(LCO)}$ = LSPCLK cycle time

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



- A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{\text{C(SPC)}}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{\text{C(SPC)}}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 5-26. SPI Master Mode External Timing (Clock Phase = 1)

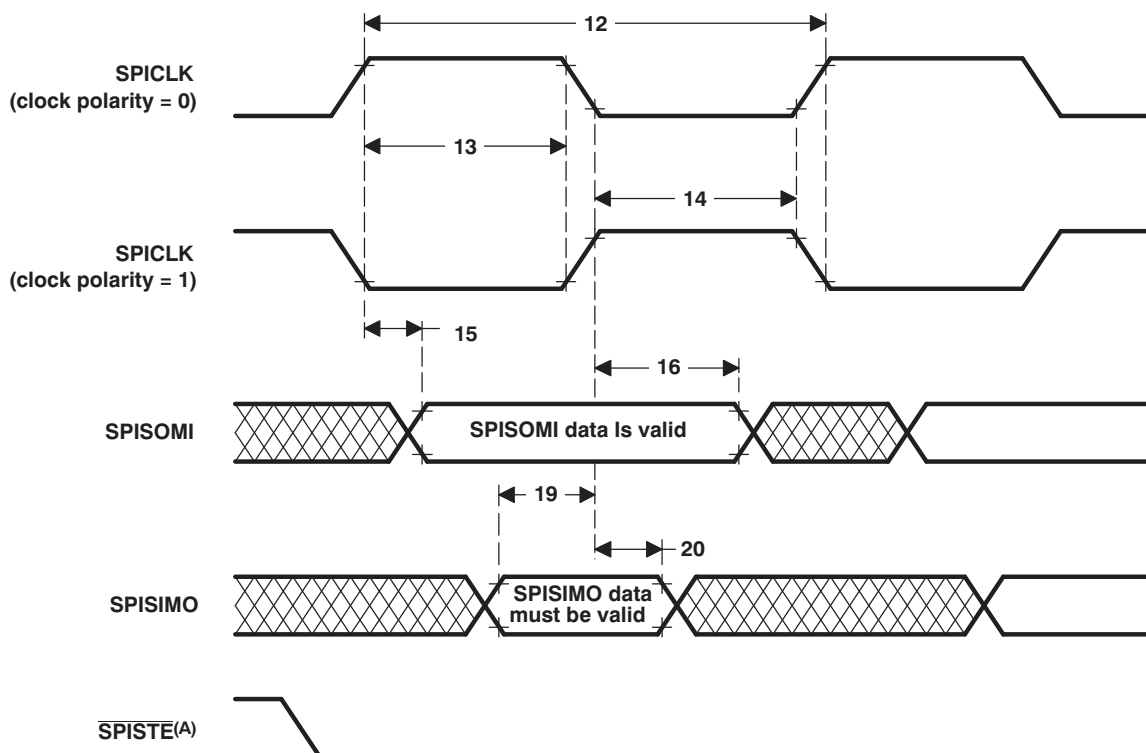
5.7.4.3.2 SPI Slave Mode Electrical Data/Timing

Table 5-28 lists the slave mode external timing (clock phase = 0) and Table 5-29 lists the slave mode external timing (clock phase = 1). Figure 5-27 and Figure 5-28 show the timing waveforms.

Table 5-28. SPI Slave Mode External Timing (Clock Phase = 0)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

| NO. | | | MIN | MAX | UNIT |
|-----|----------------------|---|-----------------------|------------------|------|
| 12 | $t_{c(SPC)}S$ | Cycle time, SPICLK | $4t_{c(LCO)}$ | | ns |
| 13 | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | |
| 14 | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | |
| 15 | $t_{d(SPCH-SOMI)}S$ | Delay time, SPICLK high to SPISOMI valid (clock polarity = 0) | | 21 | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPICLK low to SPISOMI valid (clock polarity = 1) | | 21 | |
| 16 | $t_{v(SPCL-SOMI)}S$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0) | $0.75t_{c(SPC)}S$ | | ns |
| | $t_{v(SPCH-SOMI)}S$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1) | $0.75t_{c(SPC)}S$ | | |
| 19 | $t_{su(SIMO-SPCL)}S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0) | 26 | | ns |
| | $t_{su(SIMO-SPCH)}S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1) | 26 | | |
| 20 | $t_{v(SPCL-SIMO)}S$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | | ns |
| | $t_{v(SPCH-SIMO)}S$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | | |

- (1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
- (2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
- (3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
- (4) $t_{c(LCO)}$ = LSPCLK cycle time
- (5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



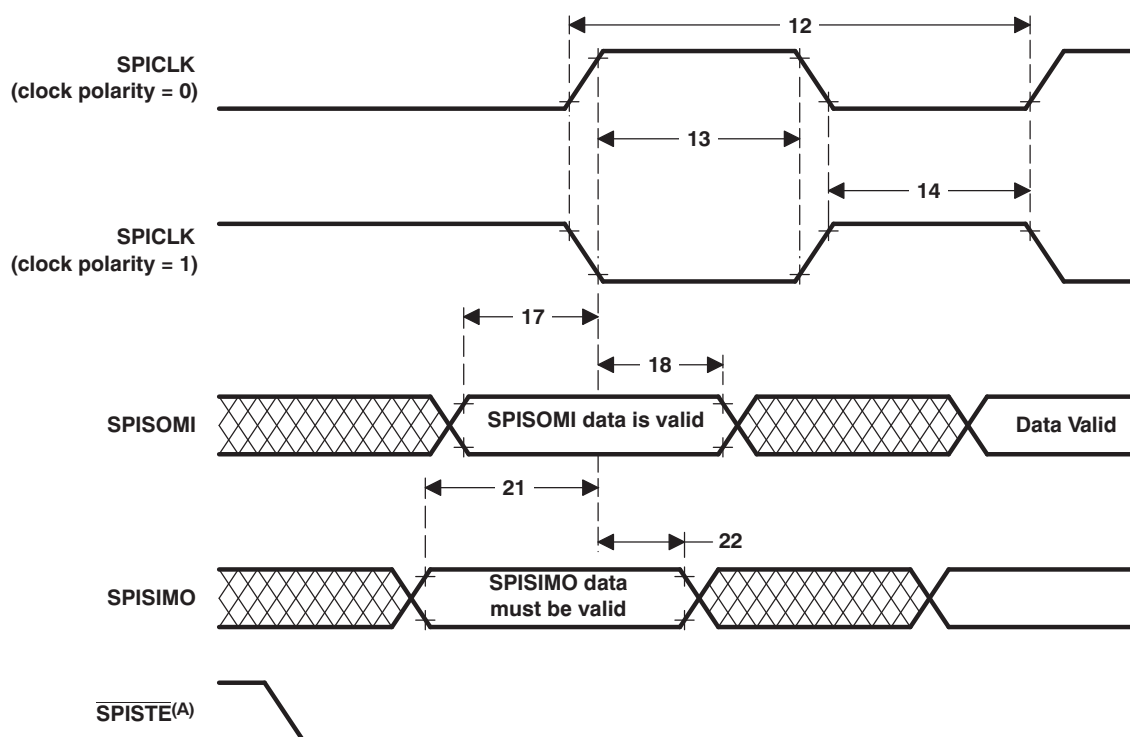
- A. In the slave mode, the SPISIMO signal should be asserted low at least $0.5t_{c(SPC)}$ (minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 5-27. SPI Slave Mode External Timing (Clock Phase = 0)

Table 5-29. SPI Slave Mode External Timing (Clock Phase = 1)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

| NO. | | | MIN | MAX | UNIT |
|-----|----------------------|---|-----------------------|------------------|------|
| 12 | $t_{c(SPC)}S$ | Cycle time, SPICLK | $8t_{c(LCO)}$ | | ns |
| 13 | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | |
| 14 | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | $0.5t_{c(SPC)}S$ | |
| 17 | $t_{su(SOMI-SPCH)}S$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | $0.125t_{c(SPC)}S$ | | ns |
| | $t_{su(SOMI-SPCL)}S$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | $0.125t_{c(SPC)}S$ | | |
| 18 | $t_{v(SPCL-SOMI)}S$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | $0.75t_{c(SPC)}S$ | | ns |
| | $t_{v(SPCH-SOMI)}S$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | $0.75t_{c(SPC)}S$ | | |
| 21 | $t_{su(SIMO-SPCH)}S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 0) | 26 | | ns |
| | $t_{su(SIMO-SPCL)}S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 1) | 26 | | |
| 22 | $t_{v(SPCH-SIMO)}S$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)}S - 10$ | | ns |
| | $t_{v(SPCL-SIMO)}S$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)}S - 10$ | | |

- (1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
- (2) $t_{c(SPC)} = \text{SPI clock cycle time} = \text{LSPCLK}/4 \text{ or } \text{LSPCLK}/(\text{SPIBRR} + 1)$
- (3) $t_{c(LCO)} = \text{LSPCLK cycle time}$
- (4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
 Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
 Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
- (5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



- A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{\text{C(SPC)}}$ before the valid SPI clock edge and remain low for at least $0.5t_{\text{C(SPC)}}$ after the receiving edge (SPICLK) of the last data bit.

Figure 5-28. SPI Slave Mode External Timing (Clock Phase = 1)

5.7.4.4 Serial Communications Interface

The F28PLC8x device includes two SCI modules (SCI-A, SCI-B). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
- NOTE:** Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
 - One start bit
 - Data-word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in [Table 5-30](#) and [Table 5-31](#).

Table 5-30. SCI-A Registers⁽¹⁾

| NAME | ADDRESS | SIZE (x16) | ALLOW PROTECTED | DESCRIPTION |
|-------------------------|---------|------------|-----------------|--|
| SCICCRA | 0x7050 | 1 | No | SCI-A Communications Control Register |
| SCICTL1A | 0x7051 | 1 | No | SCI-A Control Register 1 |
| SCIHBAUDA | 0x7052 | 1 | No | SCI-A Baud Register, High Bits |
| SCILBAUDA | 0x7053 | 1 | No | SCI-A Baud Register, Low Bits |
| SCICTL2A | 0x7054 | 1 | No | SCI-A Control Register 2 |
| SCIRXSTA | 0x7055 | 1 | No | SCI-A Receive Status Register |
| SCIRXEMUA | 0x7056 | 1 | No | SCI-A Receive Emulation Data Buffer Register |
| SCIRXBUFA | 0x7057 | 1 | No | SCI-A Receive Data Buffer Register |
| SCITXBUFA | 0x7059 | 1 | No | SCI-A Transmit Data Buffer Register |
| SCIFFTXA ⁽²⁾ | 0x705A | 1 | No | SCI-A FIFO Transmit Register |
| SCIFFRXA ⁽²⁾ | 0x705B | 1 | No | SCI-A FIFO Receive Register |
| SCIFFCTA ⁽²⁾ | 0x705C | 1 | No | SCI-A FIFO Control Register |
| SCIPRIA | 0x705F | 1 | No | SCI-A Priority Control Register |

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

(2) These registers are new registers for the FIFO mode.

Table 5-31. SCI-B Registers⁽¹⁾

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION |
|-------------------------|---------|------------|--|
| SCICCRB | 0x7750 | 1 | SCI-B Communications Control Register |
| SCICTL1B | 0x7751 | 1 | SCI-B Control Register 1 |
| SCIHBAUDB | 0x7752 | 1 | SCI-B Baud Register, High Bits |
| SCILBAUDB | 0x7753 | 1 | SCI-B Baud Register, Low Bits |
| SCICTL2B | 0x7754 | 1 | SCI-B Control Register 2 |
| SCIRXSTB | 0x7755 | 1 | SCI-B Receive Status Register |
| SCIRXEMUB | 0x7756 | 1 | SCI-B Receive Emulation Data Buffer Register |
| SCIRXBUFB | 0x7757 | 1 | SCI-B Receive Data Buffer Register |
| SCITXBUFB | 0x7759 | 1 | SCI-B Transmit Data Buffer Register |
| SCIFFTXB ⁽²⁾ | 0x775A | 1 | SCI-B FIFO Transmit Register |
| SCIFFRXB ⁽²⁾ | 0x775B | 1 | SCI-B FIFO Receive Register |
| SCIFFCTB ⁽²⁾ | 0x775C | 1 | SCI-B FIFO Control Register |
| SCIPRIB | 0x775F | 1 | SCI-B Priority Control Register |

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

(2) These registers are new registers for the FIFO mode.

Figure 5-29 shows the SCI module block diagram.

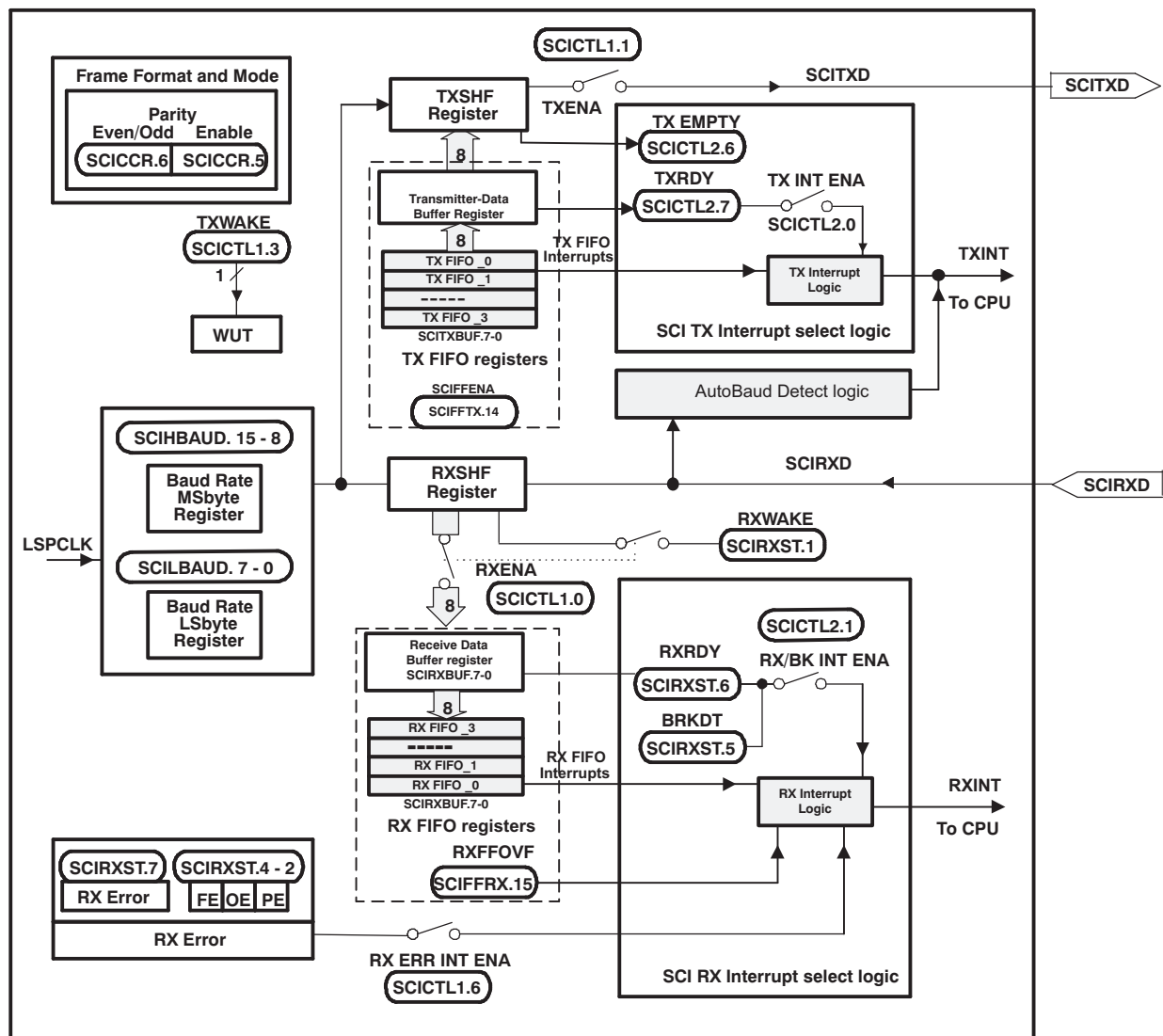


Figure 5-29. SCI Module Block Diagram

5.7.4.5 Multichannel Buffered Serial Port Module

The McBSP module has the following features:

- Compatible to McBSP in TMS320C28x/TMS320F28x devices
- Full-duplex communications
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8-, 12-, 16-, 20-, 24-, or 32-bits
- 8-bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- Works with SPI-compatible devices
- The following application interfaces can be supported on the McBSP:
 - T1/E1 framers
 - IOM-2 compliant devices
 - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
 - IIS-compliant devices
 - SPI
- McBSP clock rate,

$$\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDV})}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit.

NOTE

See [Table 5-57](#) for maximum I/O pin toggling speed.

NOTE

On the 80-pin packages, only the clock-stop mode (SPI) of the McBSP is supported.

Figure 5-30 shows the block diagram of the McBSP module.

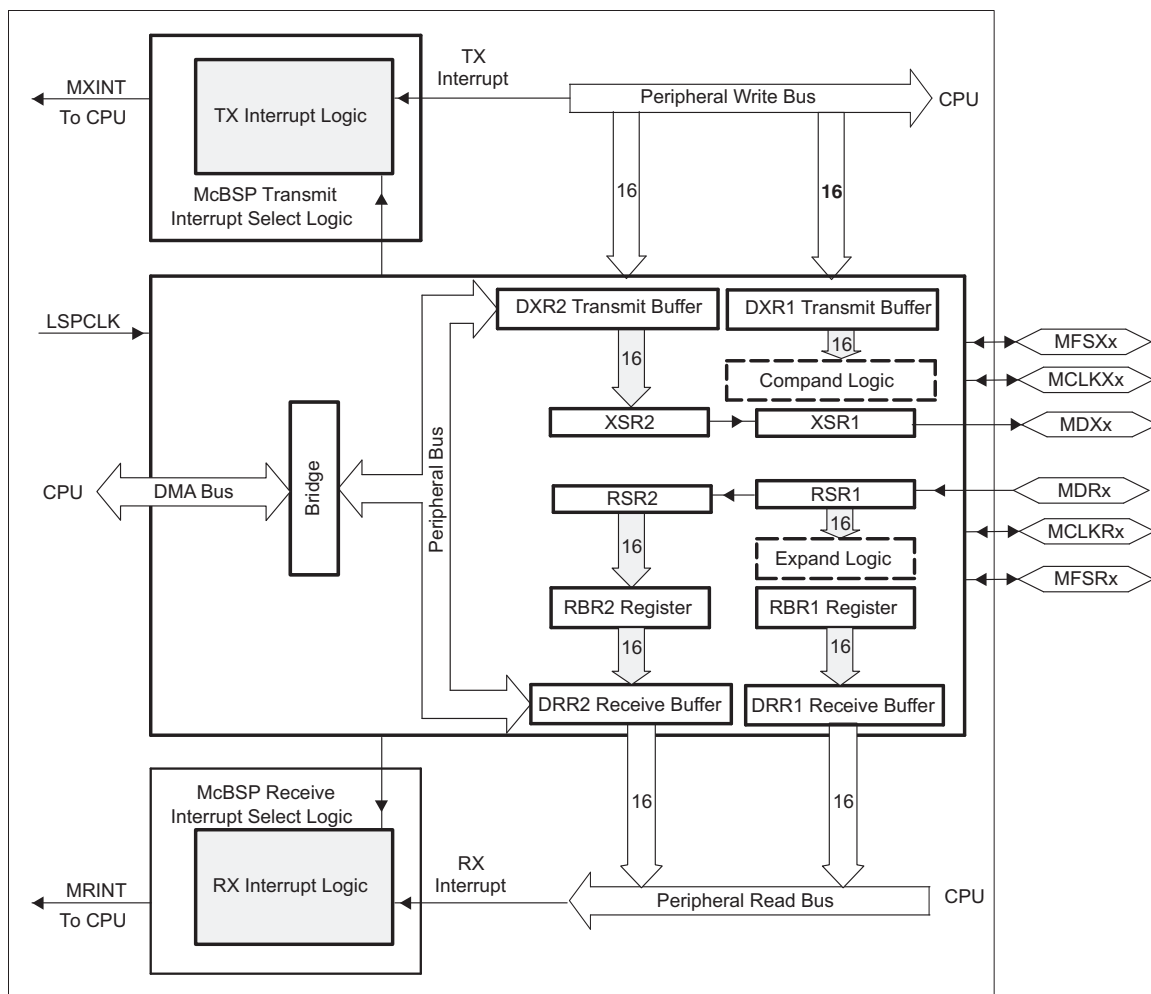


Figure 5-30. McBSP Module

Table 5-32 provides a summary of the McBSP registers.

Table 5-32. McBSP Register Summary

| NAME | McBSP-A ADDRESS | TYPE | RESET VALUE | DESCRIPTION |
|--|-----------------|------|-------------|--|
| Data Registers, Receive, Transmit | | | | |
| DDR2 | 0x5000 | R | 0x0000 | McBSP Data Receive Register 2 |
| DDR1 | 0x5001 | R | 0x0000 | McBSP Data Receive Register 1 |
| DXR2 | 0x5002 | W | 0x0000 | McBSP Data Transmit Register 2 |
| DXR1 | 0x5003 | W | 0x0000 | McBSP Data Transmit Register 1 |
| McBSP Control Registers | | | | |
| SPCR2 | 0x5004 | R/W | 0x0000 | McBSP Serial Port Control Register 2 |
| SPCR1 | 0x5005 | R/W | 0x0000 | McBSP Serial Port Control Register 1 |
| RCR2 | 0x5006 | R/W | 0x0000 | McBSP Receive Control Register 2 |
| RCR1 | 0x5007 | R/W | 0x0000 | McBSP Receive Control Register 1 |
| XCR2 | 0x5008 | R/W | 0x0000 | McBSP Transmit Control Register 2 |
| XCR1 | 0x5009 | R/W | 0x0000 | McBSP Transmit Control Register 1 |
| SRGR2 | 0x500A | R/W | 0x0000 | McBSP Sample Rate Generator Register 2 |
| SRGR1 | 0x500B | R/W | 0x0000 | McBSP Sample Rate Generator Register 1 |
| Multichannel Control Registers | | | | |
| MCR2 | 0x500C | R/W | 0x0000 | McBSP Multichannel Register 2 |
| MCR1 | 0x500D | R/W | 0x0000 | McBSP Multichannel Register 1 |
| RCERA | 0x500E | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition A |
| RCERB | 0x500F | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition B |
| XCERA | 0x5010 | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition A |
| XCERB | 0x5011 | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition B |
| PCR | 0x5012 | R/W | 0x0000 | McBSP Pin Control Register |
| RCERC | 0x5013 | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition C |
| RCERD | 0x5014 | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition D |
| XCERC | 0x5015 | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition C |
| XCERD | 0x5016 | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition D |
| RCERE | 0x5017 | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition E |
| RCERF | 0x5018 | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition F |
| XCERE | 0x5019 | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition E |
| XCERF | 0x501A | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition F |
| RCERG | 0x501B | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition G |
| RCERH | 0x501C | R/W | 0x0000 | McBSP Receive Channel Enable Register Partition H |
| XCERG | 0x501D | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition G |
| XCERH | 0x501E | R/W | 0x0000 | McBSP Transmit Channel Enable Register Partition H |
| MFFINT | 0x5023 | R/W | 0x0000 | McBSP Interrupt Enable Register |

5.7.4.5.1 McBSP Electrical Data/Timing

5.7.4.5.1.1 McBSP Transmit and Receive Timing

Table 5-33. McBSP Timing Requirements⁽¹⁾⁽²⁾

| NO. | | | | MIN | MAX | UNIT |
|-----|--|---|------------|-------------------|----------------------|------|
| | McBSP module clock (CLKG, CLKX, CLKR) range | | | 1 | | kHz |
| | | | | | 20 ⁽³⁾⁽⁴⁾ | MHz |
| | McBSP module cycle time (CLKG, CLKX, CLKR) range | | | 50 ⁽⁴⁾ | | ns |
| | | | | | 1 | ms |
| M11 | $t_{c(CKR\bar{X})}$ | Cycle time, CLKR/X | CLKR/X ext | 2P | | ns |
| M12 | $t_{w(CKR\bar{X})}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P – 7 | | ns |
| M13 | $t_{r(CKR\bar{X})}$ | Rise time, CLKR/X | CLKR/X ext | | 7 | ns |
| M14 | $t_{f(CKR\bar{X})}$ | Fall time, CLKR/X | CLKR/X ext | | 7 | ns |
| M15 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 18 | | ns |
| | | | CLKR ext | 2 | | |
| M16 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 0 | | ns |
| | | | CLKR ext | 6 | | |
| M17 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 18 | | ns |
| | | | CLKR ext | 2 | | |
| M18 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 0 | | ns |
| | | | CLKR ext | 6 | | |
| M19 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 18 | | ns |
| | | | CLKX ext | 2 | | |
| M20 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 0 | | ns |
| | | | CLKX ext | 6 | | |

- (1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- (2) $2P = 1/CLKG$ in ns. CLKG is the output of sample rate generator mux. $CLKG = CLKSRG/(1 + CLKGDV)$. CLKSRG can be LSPCLK, CLKX, CLKR as source. $CLKSRG \leq (SYSCLKOUT/2)$. McBSP performance is limited by I/O buffer switching speed.
- (3) Internal clock prescalers must be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (20 MHz).
- (4) Maximum McBSP module clock frequency decreases to 10 MHz for internal CLKR.

Table 5-34. McBSP Switching Characteristics⁽¹⁾⁽²⁾

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|-----|----------------------|--|------------|---------------|---------------|------|
| M1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P | | ns |
| M2 | $t_{w(CKRXH)}$ | Pulse duration, CLKR/X high | CLKR/X int | $D - 5^{(3)}$ | $D + 5^{(3)}$ | ns |
| M3 | $t_{w(CKRXL)}$ | Pulse duration, CLKR/X low | CLKR/X int | $C - 5^{(3)}$ | $C + 5^{(3)}$ | ns |
| M4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | 0 | 4 | ns |
| | | | CLKR ext | 3 | 27 | |
| M5 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | 0 | 4 | ns |
| | | | CLKX ext | 3 | 27 | |
| M6 | $t_{dis(CKXH-DXHZ)}$ | Disable time, CLKX high to DX high impedance following last data bit | CLKX int | | 8 | ns |
| | | | CLKX ext | | 14 | |
| M7 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid. | CLKX int | | 9 | ns |
| | | This applies to all bits except the first bit transmitted. | CLKX ext | | 28 | |
| | | Delay time, CLKX high to DX valid | CLKX int | | 8 | |
| | | | CLKX ext | | 14 | |
| | | Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | CLKX int | | P + 8 | |
| | | | CLKX ext | | P + 14 | |
| M8 | $t_{en(CKXH-DX)}$ | Enable time, CLKX high to DX driven | CLKX int | 0 | | ns |
| | | | CLKX ext | 6 | | |
| | | Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | CLKX int | P | | |
| | | | CLKX ext | P + 6 | | |
| M9 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid | FSX int | | 8 | ns |
| | | | FSX ext | | 14 | |
| | | Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode. | FSX int | | P + 8 | |
| | | | FSX ext | | P + 14 | |
| M10 | $t_{en(FXH-DX)}$ | Enable time, FSX high to DX driven | FSX int | 0 | | ns |
| | | | FSX ext | 6 | | |
| | | Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode | FSX int | P | | |
| | | | FSX ext | P + 6 | | |

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

(2) 2P = 1/CLKG in ns.

(3) C = CLKRX low pulse width = P

D = CLKRX high pulse width = P

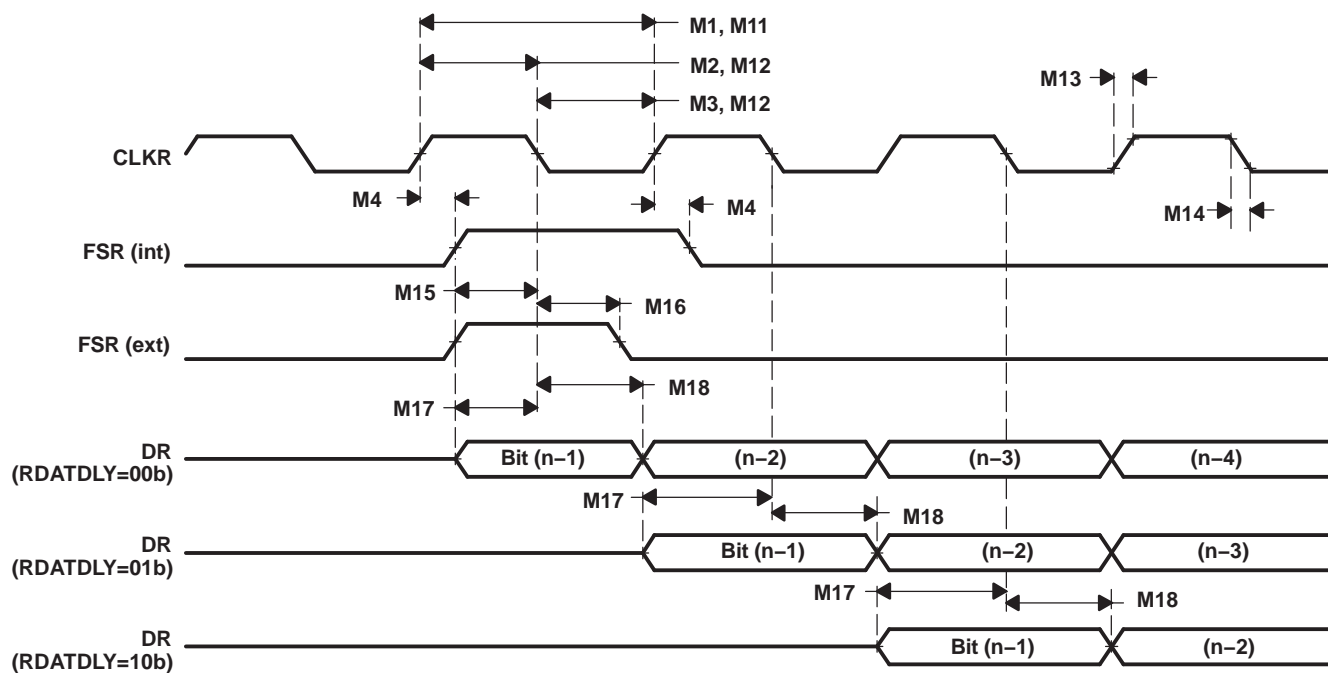


Figure 5-31. McBSP Receive Timing

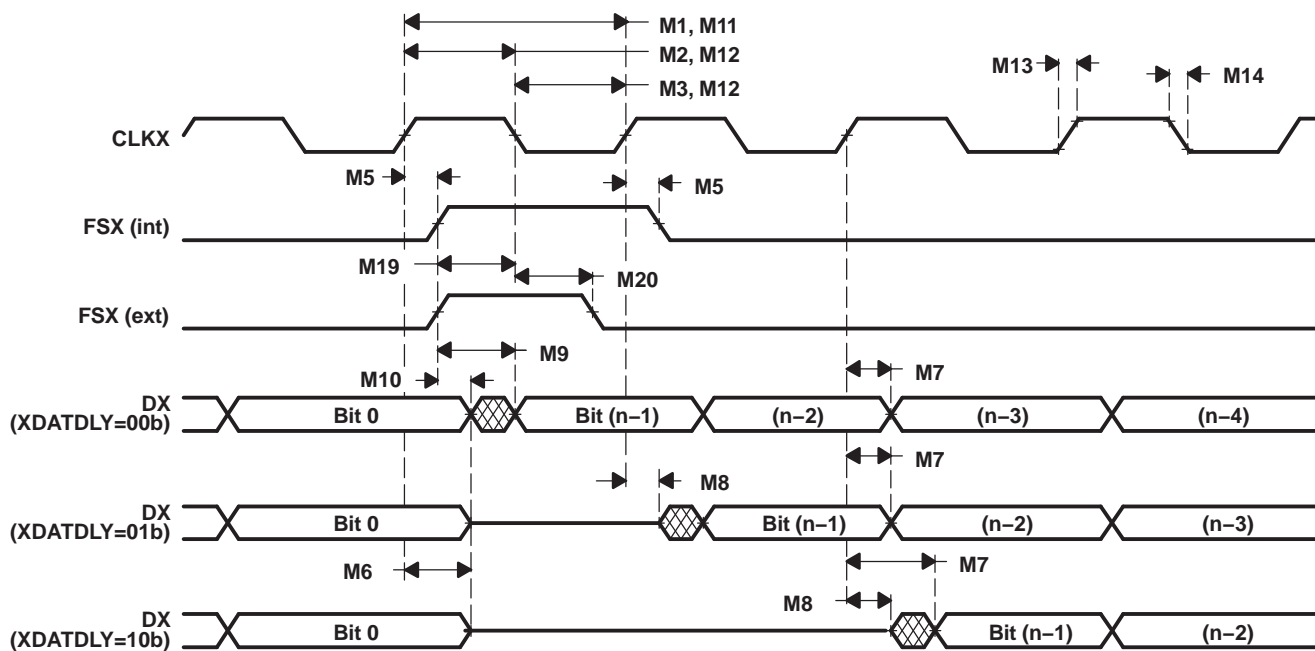


Figure 5-32. McBSP Transmit Timing

5.7.4.5.1.2 McBSP as SPI Master or Slave Timing

Table 5-35. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|---------------------|--------------------------------------|-------------------|-----|---------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M30 | $t_{su}(DRV-CKXL)$ | Setup time, DR valid before CLKX low | 30 | | 8P – 10 | | ns |
| M31 | $t_h(CKXL-DRV)$ | Hold time, DR valid after CLKX low | 1 | | 8P – 10 | | ns |
| M32 | $t_{su}(BFXL-CKXH)$ | Setup time, FSX low before CLKX high | | | 8P + 10 | | ns |
| M33 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽¹⁾ | | 16P | | ns |

(1) 2P = 1/CLKG

Table 5-36. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MASTER | | SLAVE | | UNIT |
|-----|---------------------|---|-------------------|-----|--------|---------|------|
| | | | MIN | MAX | MIN | MAX | |
| M24 | $t_h(CKXL-FXL)$ | Hold time, FSX low after CLKX low | 2P ⁽¹⁾ | | | | ns |
| M25 | $t_d(FXL-CKXH)$ | Delay time, FSX low to CLKX high | P | | | | ns |
| M26 | $t_d(CKXH-DXV)$ | Delay time, CLKX high to DX valid | –2 | 0 | 3P + 6 | 5P + 20 | ns |
| M28 | $t_{dis}(FXH-DXHZ)$ | Disable time, DX high impedance following last data bit from FSX high | 6 | | 6P + 6 | | ns |
| M29 | $t_d(FXL-DXV)$ | Delay time, FSX low to DX valid | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With a maximum LSPCLK speed of 90 MHz, CLKX maximum frequency is LSPCLK/16, that is 5.625 MHz and P = 11.11 ns.

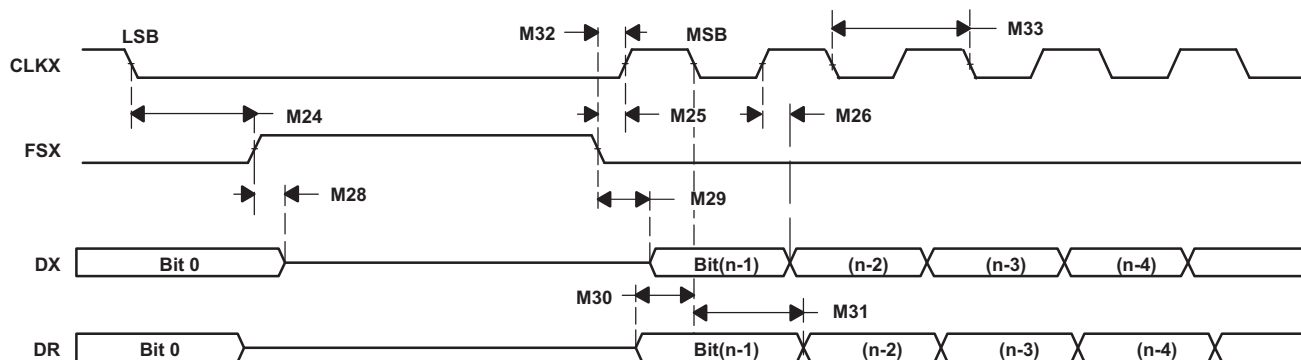


Figure 5-33. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5-37. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|---------------------------------------|-------------------|-----|----------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M39 | $t_{su}(DRV-CKXH)$ | Setup time, DR valid before CLKX high | 30 | | 8P – 10 | | ns |
| M40 | $t_h(CKXH-DRV)$ | Hold time, DR valid after CLKX high | 1 | | 8P – 10 | | ns |
| M41 | $t_{su}(FXL-CKXH)$ | Setup time, FSX low before CLKX high | | | 16P + 10 | | ns |
| M42 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽¹⁾ | | 16P | | ns |

(1) 2P = 1/CLKG

Table 5-38. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MASTER | | SLAVE | | UNIT |
|-----|----------------------|---|-------------------|-----|--------|---------|------|
| | | | MIN | MAX | MIN | MAX | |
| M34 | $t_h(CKXL-FXL)$ | Hold time, FSX low after CLKX low | P | | | | ns |
| M35 | $t_d(FXL-CKXH)$ | Delay time, FSX low to CLKX high | 2P ⁽¹⁾ | | | | ns |
| M36 | $t_d(CKXL-DXV)$ | Delay time, CLKX low to DX valid | –2 | 0 | 3P + 6 | 5P + 20 | ns |
| M37 | $t_{dis}(CKXL-DXHZ)$ | Disable time, DX high impedance following last data bit from CLKX low | P + 6 | | 7P + 6 | | ns |
| M38 | $t_d(FXL-DXV)$ | Delay time, FSX low to DX valid | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With a maximum LSPCLK speed of 90 MHz, CLKX maximum frequency is LSPCLK/16; that is, 5.625 MHz and P = 11.11 ns.

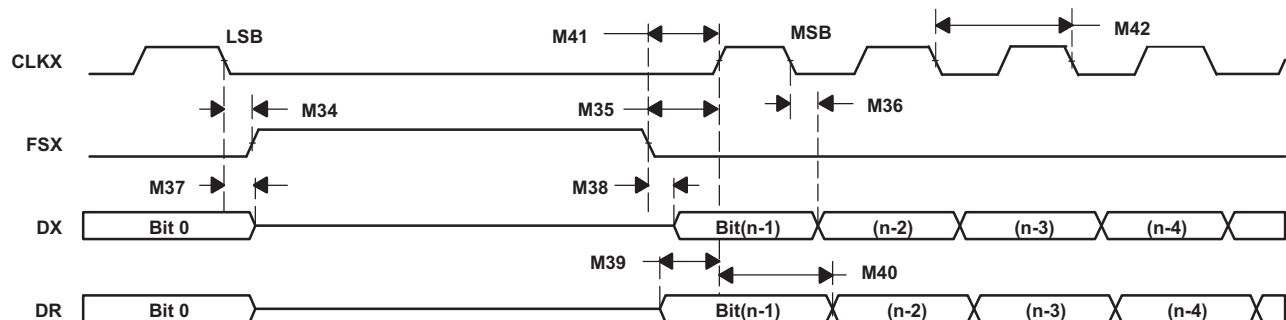


Figure 5-34. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5-39. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|---------------------------------------|------------|-----|---------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M49 | $t_{su}(DRV-CKXH)$ | Setup time, DR valid before CLKX high | 30 | | 8P – 10 | | ns |
| M50 | $t_h(CKXH-DRV)$ | Hold time, DR valid after CLKX high | 1 | | 8P – 10 | | ns |
| M51 | $t_{su}(FXL-CKXL)$ | Setup time, FSX low before CLKX low | | | 8P + 10 | | ns |
| M52 | $t_c(CKX)$ | Cycle time, CLKX | $2P^{(1)}$ | | 16P | | ns |

(1) $2P = 1/CLKG$ **Table 5-40. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)**

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MASTER | | SLAVE | | UNIT |
|-----|---------------------|---|------------|-----|--------|---------|------|
| | | | MIN | MAX | MIN | MAX | |
| M43 | $t_h(CKXH-FXL)$ | Hold time, FSX low after CLKX high | $2P^{(1)}$ | | | | ns |
| M44 | $t_d(FXL-CKXL)$ | Delay time, FSX low to CLKX low | P | | | | ns |
| M45 | $t_d(CKXL-DXV)$ | Delay time, CLKX low to DX valid | –2 | 0 | 3P + 6 | 5P + 20 | ns |
| M47 | $t_{dis}(FXH-DXHZ)$ | Disable time, DX high impedance following last data bit from FSX high | 6 | | 6P + 6 | | ns |
| M48 | $t_d(FXL-DXV)$ | Delay time, FSX low to DX valid | 6 | | 4P + 6 | | ns |

(1) $2P = 1/CLKG$

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With a maximum LSPCLK speed of 90 MHz, CLKX maximum frequency is LSPCLK/16; that is, 5.625 MHz and $P = 11.11$ ns.

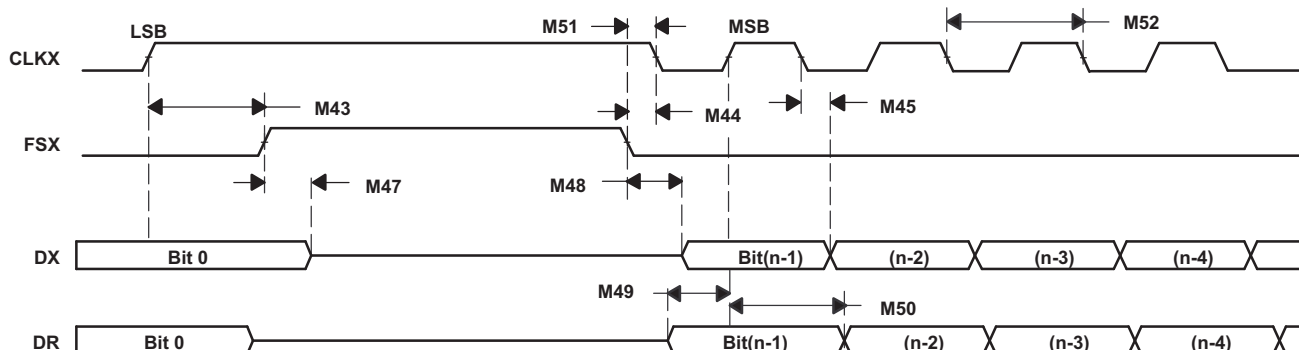
**Figure 5-35. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1**

Table 5-41. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)

| NO. | | | MASTER | | SLAVE | | UNIT |
|-----|--------------------|--------------------------------------|-------------------|-----|----------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| M58 | $t_{su(DRV-CKXL)}$ | Setup time, DR valid before CLKX low | 30 | | 8P – 10 | | ns |
| M59 | $t_h(CKXL-DRV)$ | Hold time, DR valid after CLKX low | 1 | | 8P – 10 | | ns |
| M60 | $t_{su(FXL-CKXL)}$ | Setup time, FSX low before CLKX low | | | 16P + 10 | | ns |
| M61 | $t_c(CKX)$ | Cycle time, CLKX | 2P ⁽¹⁾ | | 16P | | ns |

(1) 2P = 1/CLKG

Table 5-42. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MASTER | | SLAVE | | UNIT |
|-----|----------------------|--|-------------------|-----|--------|---------|------|
| | | | MIN | MAX | MIN | MAX | |
| M53 | $t_h(CKXH-FXL)$ | Hold time, FSX low after CLKX high | P | | | | ns |
| M54 | $t_d(FXL-CKXL)$ | Delay time, FSX low to CLKX low | 2P ⁽¹⁾ | | | | ns |
| M55 | $t_d(CKXH-DXV)$ | Delay time, CLKX high to DX valid | –2 | 0 | 3P + 6 | 5P + 20 | ns |
| M56 | $t_{dis}(CKXH-DXHZ)$ | Disable time, DX high impedance following last data bit from CLKX high | P + 6 | | 7P + 6 | | ns |
| M57 | $t_d(FXL-DXV)$ | Delay time, FSX low to DX valid | 6 | | 4P + 6 | | ns |

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With a maximum LSPCLK speed of 90 MHz, CLKX maximum frequency is LSPCLK/16, that is 5.625 MHz and P = 11.11 ns.

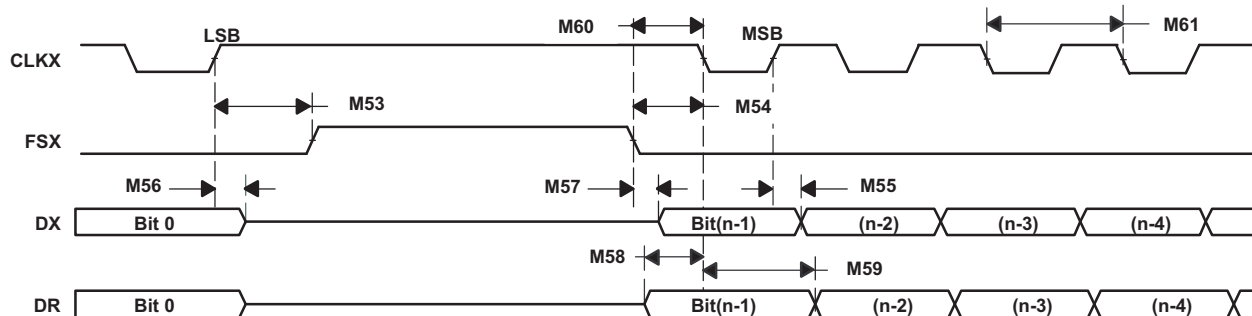


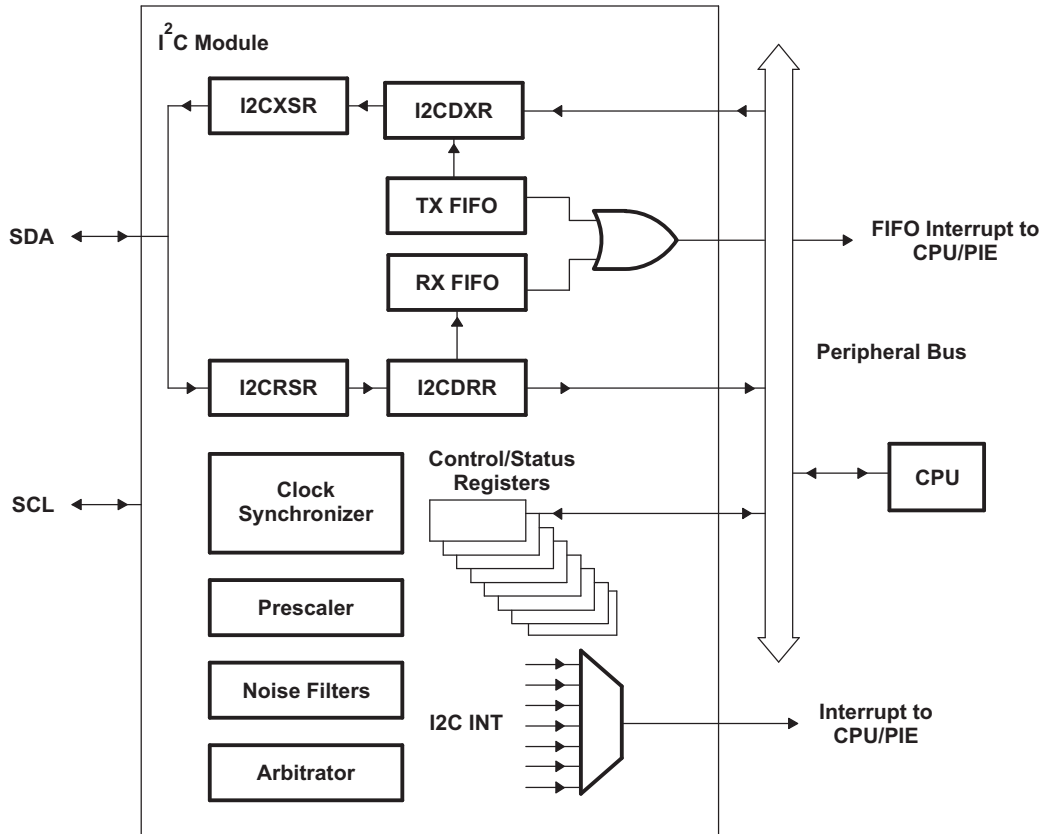
Figure 5-36. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.7.4.6 Inter-Integrated Circuit

The device contains one I²C serial port. [Figure 5-37](#) shows how the I²C peripheral module interfaces within the device.

The I²C module has the following features:

- Compliance with the Philips Semiconductors I²C-bus specification (version 2.1):
 - Support for 1-bit to 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate of from 10 kbps up to 400 kbps (I²C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
 - Transmit-data ready
 - Receive-data ready
 - Register-access ready
 - No-acknowledgment received
 - Arbitration lost
 - Stop condition detected
 - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



- The I²C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I²C port are also at the SYSCLKOUT rate.
- The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I²C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 5-37. I²C Peripheral Module Interfaces

The registers in [Table 5-43](#) configure and control the I²C port operation.

Table 5-43. I2C-A Registers

| NAME | ADDRESS | EALLOW PROTECTED | DESCRIPTION |
|---------|---------|---------------------|--|
| I2COAR | 0x7900 | No | I ² C own address register |
| I2CIER | 0x7901 | No | I ² C interrupt enable register |
| I2CSTR | 0x7902 | No | I ² C status register |
| I2CCLKL | 0x7903 | No | I ² C clock low-time divider register |
| I2CCLKH | 0x7904 | No | I ² C clock high-time divider register |
| I2CCNT | 0x7905 | No | I ² C data count register |
| I2CDRR | 0x7906 | No | I ² C data receive register |
| I2CSAR | 0x7907 | No | I ² C slave address register |
| I2CDXR | 0x7908 | No | I ² C data transmit register |
| I2CMDR | 0x7909 | No | I ² C mode register |
| I2CISRC | 0x790A | No | I ² C interrupt source register |
| I2CPSC | 0x790C | No | I ² C prescaler register |
| I2CFFTX | 0x7920 | No | I ² C FIFO transmit register |
| I2CFFRX | 0x7921 | No | I ² C FIFO receive register |
| I2CRSR | – | No | I ² C receive shift register (not accessible to the CPU) |
| I2CXSR | – | No | I ² C transmit shift register (not accessible to the CPU) |

5.7.4.6.1 I²C Electrical Data/Timing

Table 5-44. I²C Timing

| | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|---|---|------------------------|-----------------------|------|
| f _{SCL} | SCL clock frequency | I ² C clock module frequency is between 7 MHz and 12 MHz and I ² C prescaler and clock divider registers are configured appropriately | | 400 | kHz |
| v _{il} | Low level input voltage | | | 0.3 V _{DDIO} | V |
| V _{ih} | High level input voltage | | 0.7 V _{DDIO} | | V |
| V _{hys} | Input hysteresis | | 0.05 V _{DDIO} | | V |
| V _{ol} | Low level output voltage | 3 mA sink current | 0 | 0.4 | V |
| t _{LOW} | Low period of SCL clock | I ² C clock module frequency is between 7 MHz and 12 MHz and I ² C prescaler and clock divider registers are configured appropriately | 1.3 | | μs |
| t _{HIGH} | High period of SCL clock | I ² C clock module frequency is between 7 MHz and 12 MHz and I ² C prescaler and clock divider registers are configured appropriately | 0.6 | | μs |
| I _I | Input current with an input voltage between 0.1 V _{DDIO} and 0.9 V _{DDIO} MAX | | –10 | 10 | μA |

5.7.4.7 Enhanced Pulse Width Modulator Module

The F28PLC8x device contains two ePWM modules (ePWM1, ePWM2). Figure 5-38 shows a block diagram of the ePWM modules. Figure 5-39 shows the signal interconnections with the ePWM.

Table 5-45 shows the complete ePWM register set per module.

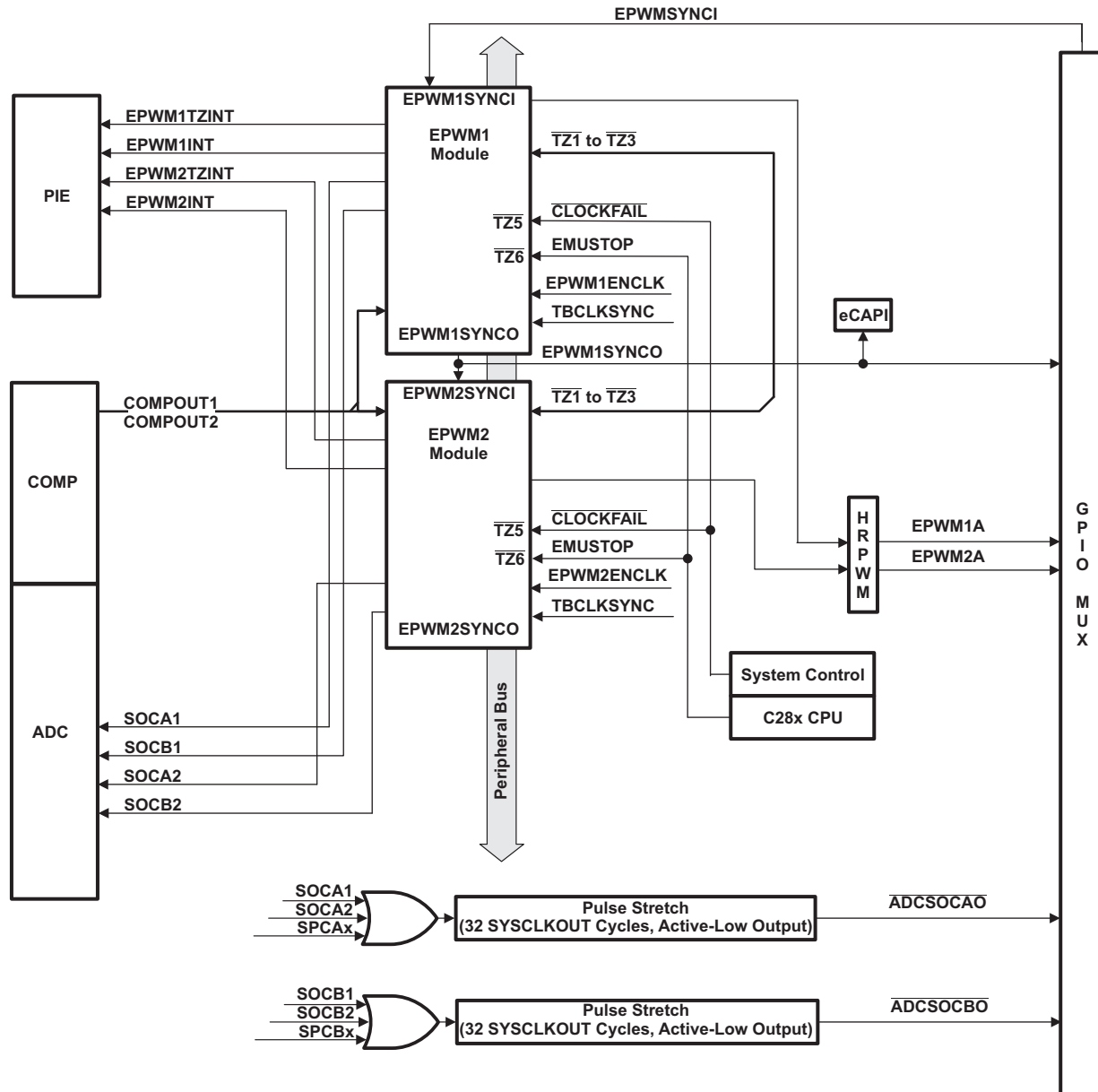


Figure 5-38. ePWM

Table 5-45. ePWM1–ePWM2 Control and Status Registers

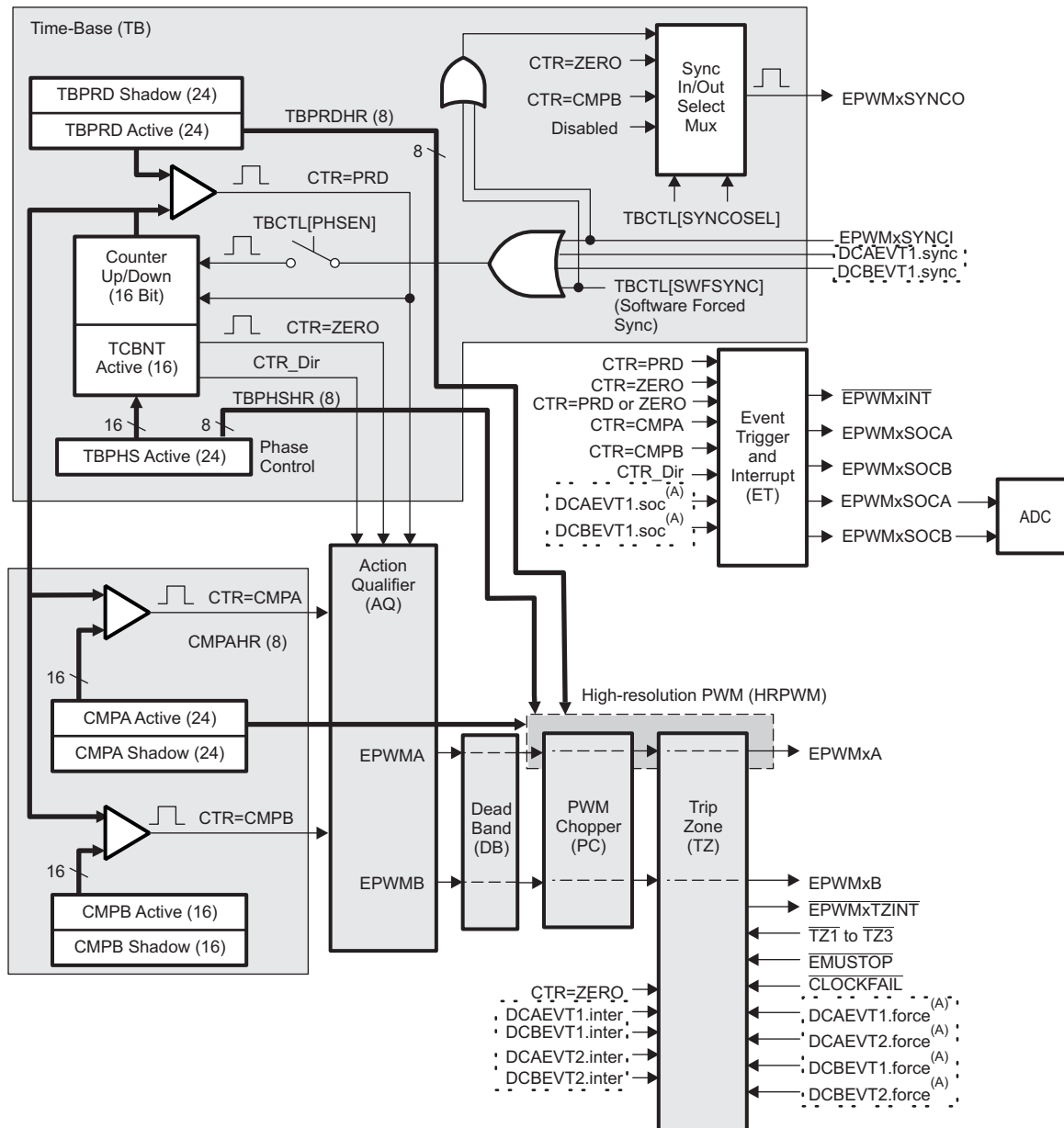
| NAME | ePWM1 | ePWM2 | SIZE (x16) / #SHADOW | DESCRIPTION |
|-------------|--------|--------|----------------------|--|
| TBCTL | 0x6800 | 0x6840 | 1 / 0 | Time Base Control Register |
| TBSTS | 0x6801 | 0x6841 | 1 / 0 | Time Base Status Register |
| TBPHSHR | 0x6802 | 0x6842 | 1 / 0 | Time Base Phase HRPWM Register |
| TBPHS | 0x6803 | 0x6843 | 1 / 0 | Time Base Phase Register |
| TBCTR | 0x6804 | 0x6844 | 1 / 0 | Time Base Counter Register |
| TBPRD | 0x6805 | 0x6845 | 1 / 1 | Time Base Period Register Set |
| TBPRDHR | 0x6806 | 0x6846 | 1 / 1 | Time Base Period High Resolution Register ⁽¹⁾ |
| CMPCTL | 0x6807 | 0x6847 | 1 / 0 | Counter Compare Control Register |
| CMPAHR | 0x6808 | 0x6848 | 1 / 1 | Time Base Compare A HRPWM Register |
| CMPA | 0x6809 | 0x6849 | 1 / 1 | Counter Compare A Register Set |
| CMPB | 0x680A | 0x684A | 1 / 1 | Counter Compare B Register Set |
| AQCTLA | 0x680B | 0x684B | 1 / 0 | Action Qualifier Control Register For Output A |
| AQCTLB | 0x680C | 0x684C | 1 / 0 | Action Qualifier Control Register For Output B |
| AQSFR | 0x680D | 0x684D | 1 / 0 | Action Qualifier Software Force Register |
| AQCSFR | 0x680E | 0x684E | 1 / 1 | Action Qualifier Continuous S/W Force Register Set |
| DBCTL | 0x680F | 0x684F | 1 / 1 | Dead-Band Generator Control Register |
| DBRED | 0x6810 | 0x6850 | 1 / 0 | Dead-Band Generator Rising Edge Delay Count Register |
| DBFED | 0x6811 | 0x6851 | 1 / 0 | Dead-Band Generator Falling Edge Delay Count Register |
| TZSEL | 0x6812 | 0x6852 | 1 / 0 | Trip Zone Select Register ⁽¹⁾ |
| TZDCSEL | 0x6813 | 0x6853 | 1 / 0 | Trip Zone Digital Compare Register |
| TZCTL | 0x6814 | 0x6854 | 1 / 0 | Trip Zone Control Register ⁽¹⁾ |
| TZEINT | 0x6815 | 0x6855 | 1 / 0 | Trip Zone Enable Interrupt Register ⁽¹⁾ |
| TZFLG | 0x6816 | 0x6856 | 1 / 0 | Trip Zone Flag Register ⁽¹⁾ |
| TZCLR | 0x6817 | 0x6857 | 1 / 0 | Trip Zone Clear Register ⁽¹⁾ |
| TZFRC | 0x6818 | 0x6858 | 1 / 0 | Trip Zone Force Register ⁽¹⁾ |
| ETSEL | 0x6819 | 0x6859 | 1 / 0 | Event Trigger Selection Register |
| ETPS | 0x681A | 0x685A | 1 / 0 | Event Trigger Prescale Register |
| ETFLG | 0x681B | 0x685B | 1 / 0 | Event Trigger Flag Register |
| ETCLR | 0x681C | 0x685C | 1 / 0 | Event Trigger Clear Register |
| ETFRC | 0x681D | 0x685D | 1 / 0 | Event Trigger Force Register |
| PCCTL | 0x681E | 0x685E | 1 / 0 | PWM Chopper Control Register |
| HRCNFG | 0x6820 | 0x6860 | 1 / 0 | HRPWM Configuration Register ⁽¹⁾ |
| HRMSTEP | 0x6826 | - | 1 / 0 | HRPWM MEP Step Register |
| HRPCTL | 0x6828 | 0x6868 | 1 / 0 | High resolution Period Control Register ⁽¹⁾ |
| TBPRDHRM | 0x682A | 0x686A | 1 / W ⁽²⁾ | Time Base Period HRPWM Register Mirror |
| TBPRDM | 0x682B | 0x686B | 1 / W ⁽²⁾ | Time Base Period Register Mirror |
| CMPAHRM | 0x682C | 0x686C | 1 / W ⁽²⁾ | Compare A HRPWM Register Mirror |
| CMPAM | 0x682D | 0x686D | 1 / W ⁽²⁾ | Compare A Register Mirror |
| DCTRIPSEL | 0x6830 | 0x6870 | 1 / 0 | Digital Compare Trip Select Register ⁽¹⁾ |
| DCACTL | 0x6831 | 0x6871 | 1 / 0 | Digital Compare A Control Register ⁽¹⁾ |
| DCBCTL | 0x6832 | 0x6872 | 1 / 0 | Digital Compare B Control Register ⁽¹⁾ |
| DCFCTL | 0x6833 | 0x6873 | 1 / 0 | Digital Compare Filter Control Register ⁽¹⁾ |
| DCCAPCT | 0x6834 | 0x6874 | 1 / 0 | Digital Compare Capture Control Register ⁽¹⁾ |
| DCOFFSET | 0x6835 | 0x6875 | 1 / 1 | Digital Compare Filter Offset Register |
| DCOFFSETCNT | 0x6836 | 0x6876 | 1 / 0 | Digital Compare Filter Offset Counter Register |

(1) Registers that are EALLOW protected.

(2) W = Write to shadow register

Table 5-45. ePWM1–ePWM2 Control and Status Registers (continued)

| NAME | ePWM1 | ePWM2 | SIZE (x16) / #SHADOW | DESCRIPTION |
|--------------|--------|--------|----------------------|--|
| DCFWINDOW | 0x6837 | 0x6877 | 1 / 0 | Digital Compare Filter Window Register |
| DCFWINDOWCNT | 0x6838 | 0x6878 | 1 / 0 | Digital Compare Filter Window Counter Register |
| DCCAP | 0x6839 | 0x6879 | 1 / 1 | Digital Compare Counter Capture Register |



- A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and TZ signals.

Figure 5-39. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

5.7.4.7.1 ePWM Electrical Data/Timing

PWM refers to PWM outputs on ePWM1–2. Table 5-46 shows the PWM timing requirements and Table 5-47, switching characteristics.

Table 5-46. ePWM Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------|------------------------|-----------------------------|-----|--------|
| $t_{w(SYCIN)}$ | Sync input pulse width | | | |
| | Asynchronous | $2t_{c(SCO)}$ | | cycles |
| | Synchronous | $2t_{c(SCO)}$ | | cycles |
| | With input qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-58.

Table 5-47. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|---|---------------|-----|--------|
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | 33.33 | | ns |
| $t_{w(SYNCOUT)}$ | Sync output pulse width | $8t_{c(SCO)}$ | | cycles |
| $t_{d(PWM)tza}$ | Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low | | 25 | ns |
| $t_{d(TZ-PWM)HZ}$ | Delay time, trip input active to PWM Hi-Z | | 20 | ns |

5.7.4.7.2 Trip-Zone Input Timing

Table 5-48. Trip-Zone Input Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------|--|-------------------------------|-----|--------|
| $t_{w(TZ)}$ | Pulse duration, \overline{TZx} input low | | | |
| | Asynchronous | $2t_{c(TBCLK)}$ | | cycles |
| | Synchronous | $2t_{c(TBCLK)}$ | | cycles |
| | With input qualifier | $2t_{c(TBCLK)} + t_{w(IQSW)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see Table 5-58.

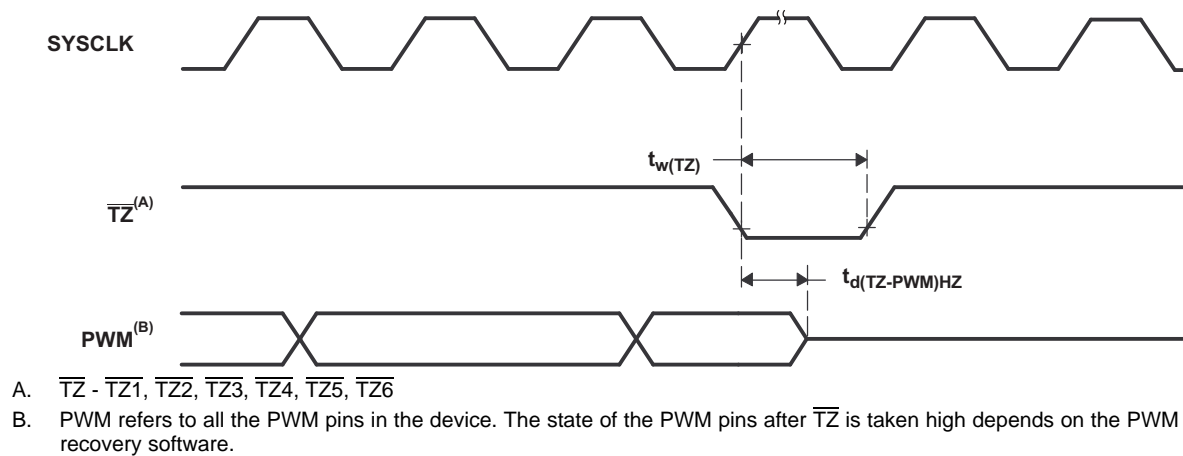


Figure 5-40. PWM Hi-Z Characteristics

5.7.4.8 High-Resolution PWM

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

NOTE

The minimum SYSCLKOUT frequency allowed for HRPWM is 60 MHz.

NOTE

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB channel will have ± 1 – 2 TBCLK cycles of jitter on the output.

5.7.4.8.1 HRPWM Electrical Data/Timing

Table 5-49 shows the high-resolution PWM switching characteristics.

Table 5-49. High-Resolution PWM Characteristics⁽¹⁾

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size ⁽²⁾ | | 150 | 310 | ps |

(1) The HRPWM operates at a minimum SYSCLKOUT frequency of 60 MHz.

(2) Maximum MEP step size is based on worst-case process, maximum temperature and minimum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

5.7.4.9 Enhanced Capture Module

The device contains an enhanced capture module (eCAP1). Figure 5-41 shows a functional block diagram of a module.

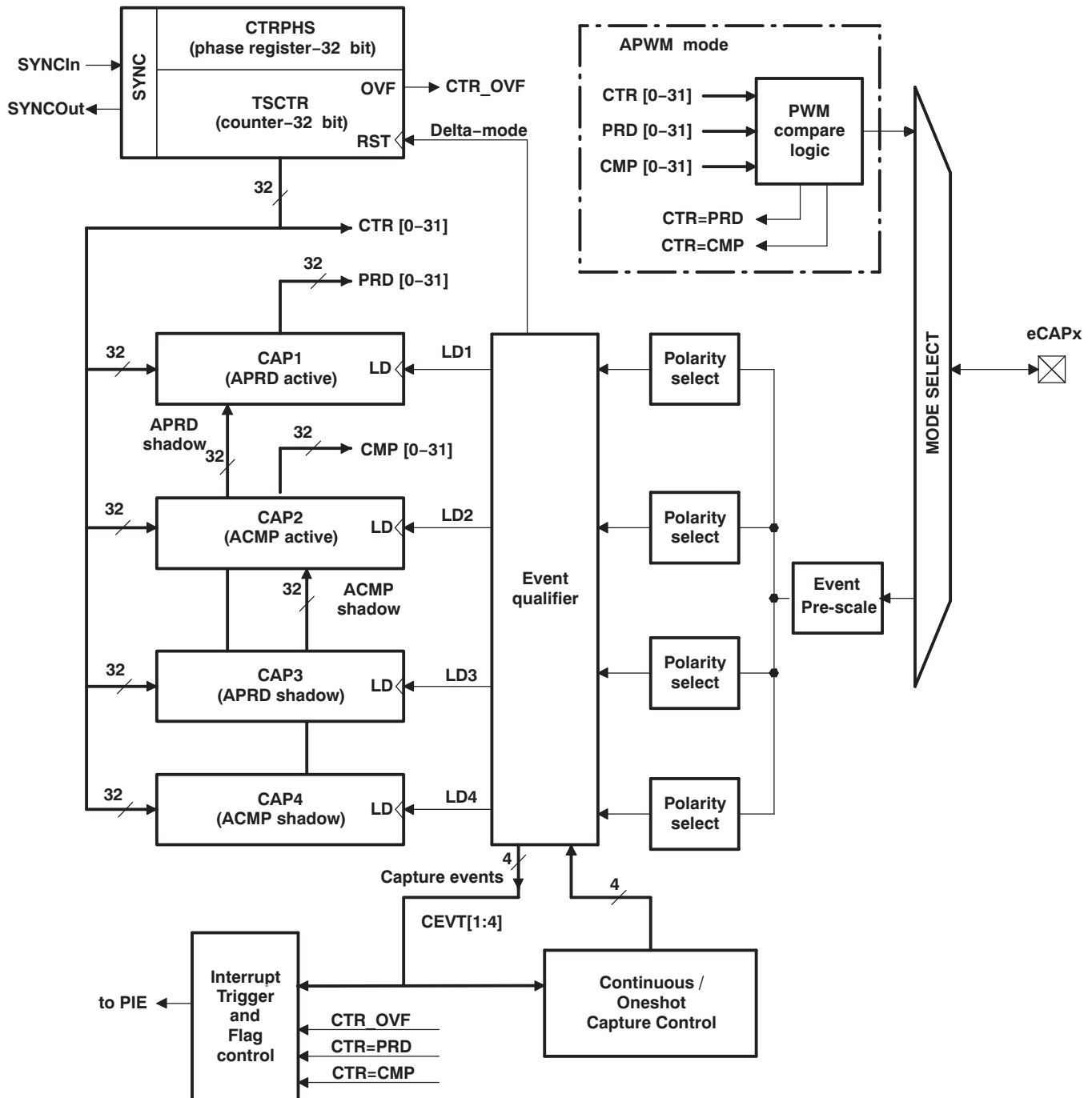


Figure 5-41. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

[Table 5-50](#) lists the eCAP Control and Status Registers.

Table 5-50. eCAP Control and Status Registers

| NAME | eCAP1 | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION |
|----------|-----------------|------------|---------------------|-------------------------------------|
| TSCTR | 0x6A00 | 2 | No | Time-Stamp Counter |
| CTPHS | 0x6A02 | 2 | No | Counter Phase Offset Value Register |
| CAP1 | 0x6A04 | 2 | No | Capture 1 Register |
| CAP2 | 0x6A06 | 2 | No | Capture 2 Register |
| CAP3 | 0x6A08 | 2 | No | Capture 3 Register |
| CAP4 | 0x6A0A | 2 | No | Capture 4 Register |
| Reserved | 0x6A0C – 0x6A12 | 8 | No | Reserved |
| ECCTL1 | 0x6A14 | 1 | No | Capture Control Register 1 |
| ECCTL2 | 0x6A15 | 1 | No | Capture Control Register 2 |
| ECEINT | 0x6A16 | 1 | No | Capture Interrupt Enable Register |
| ECFLG | 0x6A17 | 1 | No | Capture Interrupt Flag Register |
| ECCLR | 0x6A18 | 1 | No | Capture Interrupt Clear Register |
| ECFRC | 0x6A19 | 1 | No | Capture Interrupt Force Register |
| Reserved | 0x6A1A – 0x6A1F | 6 | No | Reserved |

5.7.4.9.1 eCAP Electrical Data/Timing

[Table 5-51](#) shows the eCAP timing requirement and [Table 5-52](#) shows the eCAP switching characteristics.

Table 5-51. eCAP Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------|---------------------------|----------------------|-----------------------------|--------|
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SCO)}$ | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | cycles |
| | | With input qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ | cycles |

(1) For an explanation of the input qualifier parameters, see [Table 5-58](#).

Table 5-52. eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_{w(APWM)}$ Pulse duration, APWMx output high/low | 20 | | ns |

5.7.4.10 JTAG Port

On the F28PLC8x device, the JTAG port is reduced to 5 pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 5-42. During emulation/debug, the GPIO function of these pins are not available. If the GPIO38/TCK/XCLKIN pin is used to provide an external clock, an alternate clock source should be used to clock the device during emulation/debug since this pin will be needed for the TCK function.

NOTE

In the F28PLC8x device, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the emulation capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the emulator from driving (or being driven by) the JTAG pins for successful debug.

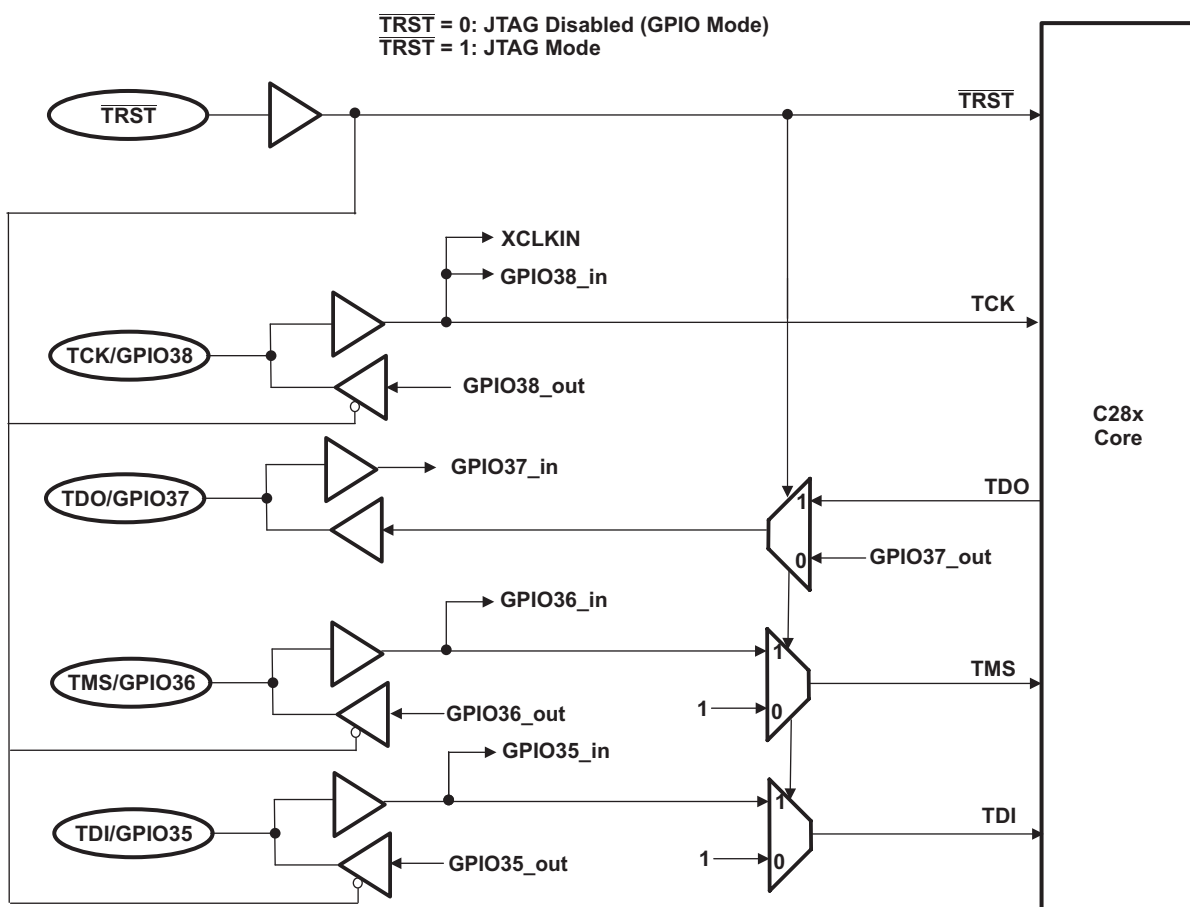


Figure 5-42. JTAG/GPIO Multiplexing

5.7.4.11 General-Purpose Input/Output MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 45 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). [Table 5-53](#) shows the GPIO register mapping.

Table 5-53. GPIO Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION |
|---|---------|------------|---|
| GPIO CONTROL REGISTERS (EALLOW PROTECTED) | | | |
| GPACTRL | 0x6F80 | 2 | GPIO A Control Register (GPIO0 to 31) |
| GPAQSEL1 | 0x6F82 | 2 | GPIO A Qualifier Select 1 Register (GPIO0 to 15) |
| GPAQSEL2 | 0x6F84 | 2 | GPIO A Qualifier Select 2 Register (GPIO16 to 31) |
| GPAMUX1 | 0x6F86 | 2 | GPIO A MUX 1 Register (GPIO0 to 15) |
| GPAMUX2 | 0x6F88 | 2 | GPIO A MUX 2 Register (GPIO16 to 31) |
| GPADIR | 0x6F8A | 2 | GPIO A Direction Register (GPIO0 to 31) |
| GPAPUD | 0x6F8C | 2 | GPIO A Pullup Disable Register (GPIO0 to 31) |
| GPBCTRL | 0x6F90 | 2 | GPIO B Control Register (GPIO32 to 44) |
| GPBQSEL1 | 0x6F92 | 2 | GPIO B Qualifier Select 1 Register (GPIO32 to 44) |
| GPBMUX1 | 0x6F96 | 2 | GPIO B MUX 1 Register (GPIO32 to 44) |
| GPBDIR | 0x6F9A | 2 | GPIO B Direction Register (GPIO32 to 44) |
| GPBPUD | 0x6F9C | 2 | GPIO B Pullup Disable Register (GPIO32 to 44) |
| AIOMUX1 | 0x6FB6 | 2 | Analog, I/O mux 1 register (AIO0 to AIO15) |
| AIODIR | 0x6FBA | 2 | Analog, I/O Direction Register (AIO0 to AIO15) |
| GPIO DATA REGISTERS (NOT EALLOW PROTECTED) | | | |
| GPADAT | 0x6FC0 | 2 | GPIO A Data Register (GPIO0 to 31) |
| GPASET | 0x6FC2 | 2 | GPIO A Data Set Register (GPIO0 to 31) |
| GPACLEAR | 0x6FC4 | 2 | GPIO A Data Clear Register (GPIO0 to 31) |
| GPATOGGLE | 0x6FC6 | 2 | GPIO A Data Toggle Register (GPIO0 to 31) |
| GPBDAT | 0x6FC8 | 2 | GPIO B Data Register (GPIO32 to 44) |
| GPBSET | 0x6FCA | 2 | GPIO B Data Set Register (GPIO32 to 44) |
| GPBCLEAR | 0x6FCC | 2 | GPIO B Data Clear Register (GPIO32 to 44) |
| GPBTOGGLE | 0x6FCE | 2 | GPIO B Data Toggle Register (GPIO32 to 44) |
| AIODAT | 0x6FD8 | 2 | Analog I/O Data Register (AIO0 to AIO15) |
| AIOSET | 0x6FDA | 2 | Analog I/O Data Set Register (AIO0 to AIO15) |
| AIOCLEAR | 0x6FDC | 2 | Analog I/O Data Clear Register (AIO0 to AIO15) |
| AIOGGLE | 0x6FDE | 2 | Analog I/O Data Toggle Register (AIO0 to AIO15) |
| GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED) | | | |
| GPIOXINT1SEL | 0x6FE0 | 1 | XINT1 GPIO Input Select Register (GPIO0 to 31) |
| GPIOXINT2SEL | 0x6FE1 | 1 | XINT2 GPIO Input Select Register (GPIO0 to 31) |
| GPIOXINT3SEL | 0x6FE2 | 1 | XINT3 GPIO Input Select Register (GPIO0 to 31) |
| GPIOLPMSSEL | 0x6FE8 | 2 | LPM GPIO Select Register (GPIO0 to 31) |

NOTE

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

Table 5-54. GPIOA MUX⁽¹⁾ (2)

| | DEFAULT AT RESET PRIMARY I/O FUNCTION | PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 | PERIPHERAL SELECTION 3 |
|--------------------------|---|---------------------------|---------------------------|---------------------------|
| GPAMUX1 REGISTER BITS | (GPAMUX1 BITS = 00) | (GPAMUX1 BITS = 01) | (GPAMUX1 BITS = 10) | (GPAMUX1 BITS = 11) |
| 1-0 | GPIO0 | EPWM1A (O) | Reserved | Reserved |
| 3-2 | GPIO1 | Reserved | Reserved | COMP1OUT (O) |
| 5-4 | GPIO2 | EPWM2A (O) | Reserved | Reserved |
| 7-6 | GPIO3 | Reserved | SPISOMIA (I/O) | COMP2OUT (O) |
| 9-8 | GPIO4 | Reserved | Reserved | Reserved |
| 11-10 | GPIO5 | Reserved | SPISIMOA (I/O) | ECAP1 (I/O) |
| 13-12 | GPIO6 | Reserved | EPWMSYNCl (I) | EPWMSYNCO (O) |
| 15-14 | GPIO7 | Reserved | SCIRXDA (I) | Reserved |
| 17-16 | GPIO8 | Reserved | Reserved | ADCSOAO (O) |
| 19-18 | GPIO9 | Reserved | SCITXDB (O) | Reserved |
| 21-20 | GPIO10 | Reserved | Reserved | ADCSOCBO (O) |
| 23-22 | GPIO11 | Reserved | SCIRXDB (I) | ECAP1 (I/O) |
| 25-24 | GPIO12 | TZ1 (I) | SCITXDA (O) | SPISIMOB (I/O) |
| 27-26 | GPIO13 | TZ2 (I) | Reserved | SPISOMIB (I/O) |
| 29-28 | GPIO14 | TZ3 (I) | SCITXDB (O) | SPICLKB (I/O) |
| 31-30 | GPIO15 | Reserved | SCIRXDB (I) | SPISTEB (I/O) |
| GPAMUX2 REGISTER BITS | (GPAMUX2 BITS = 00) | (GPAMUX2 BITS = 01) | (GPAMUX2 BITS = 10) | (GPAMUX2 BITS = 11) |
| 1-0 | GPIO16 | SPISIMOA (I/O) | Reserved | TZ2 (I) |
| 3-2 | GPIO17 | SPISOMIA (I/O) | Reserved | TZ3 (I) |
| 5-4 | GPIO18 | SPICLKA (I/O) | SCITXDB (O) | XCLKOUT (O) |
| 7-6 | GPIO19/XCLKIN | SPISTEA (I/O) | SCIRXDB (I) | ECAP1 (I/O) |
| 9-8 | GPIO20 | Reserved | MDXA (O) | COMP1OUT (O) |
| 11-10 | GPIO21 | Reserved | MDRA (I) | COMP2OUT (O) |
| 13-12 | GPIO22 | Reserved | MCLKXA (I/O) | SCITXDB (O) |
| 15-14 | GPIO23 | Reserved | MFSXA (I/O) | SCIRXDB (I) |
| 17-16 | GPIO24 | ECAP1 (I/O) | Reserved | SPISIMOB (I/O) |
| 19-18 | GPIO25 | Reserved | Reserved | SPISOMIB (I/O) |
| 21-20 | GPIO26 | Reserved | Reserved | SPICLKB (I/O) |
| 23-22 | GPIO27 | Reserved | Reserved | SPISTEB (I/O) |
| 25-24 | GPIO28 | SCIRXDA (I) | SDAA (I/OD) | TZ2 (I) |
| 27-26 | GPIO29 | SCITXDA (O) | SCLA (I/OD) | TZ3 (I) |
| 29-28 | GPIO30 | Reserved | Reserved | Reserved |
| 31-30 | GPIO31 | Reserved | Reserved | Reserved |

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should the Reserved GPxMUX1/2 register setting be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

(2) I = Input, O = Output, OD = Open Drain

Table 5-55. GPIOB MUX⁽¹⁾⁽²⁾

| | DEFAULT AT RESET PRIMARY I/O FUNCTION | PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 | PERIPHERAL SELECTION 3 |
|--------------------------|--|---------------------------|---------------------------|---------------------------|
| GPBMUX1 REGISTER BITS | (GPBMUX1 BITS = 00) | (GPBMUX1 BITS = 01) | (GPBMUX1 BITS = 10) | (GPBMUX1 BITS = 11) |
| 1-0 | GPIO32 | SDAA (I/OD) | EPWMSYNCl (I) | ADCSOCAO (O) |
| 3-2 | GPIO33 | SCLA (I/OD) | EPWMSYNCO (O) | ADCSOCBO (O) |
| 5-4 | GPIO34 | COMP2OUT (O) | Reserved | COMP3OUT (O) |
| 7-6 | GPIO35 (TDI) | Reserved | Reserved | Reserved |
| 9-8 | GPIO36 (TMS) | Reserved | Reserved | Reserved |
| 11-10 | GPIO37 (TDO) | Reserved | Reserved | Reserved |
| 13-12 | GPIO38/XCLKIN (TCK) | Reserved | Reserved | Reserved |
| 15-14 | GPIO39 | Reserved | Reserved | Reserved |
| 17-16 | Reserved | Reserved | Reserved | Reserved |
| 19-18 | Reserved | Reserved | Reserved | Reserved |
| 21-20 | Reserved | Reserved | Reserved | Reserved |
| 23-22 | Reserved | Reserved | Reserved | Reserved |
| 25-24 | Reserved | Reserved | Reserved | Reserved |
| 27-26 | Reserved | Reserved | Reserved | Reserved |
| 29-28 | Reserved | Reserved | Reserved | Reserved |
| 31-30 | Reserved | Reserved | Reserved | Reserved |

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should the Reserved GPxMUX1/2 register setting be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

(2) I = Input, O = Output, OD = Open Drain

Table 5-56. Analog MUX⁽¹⁾

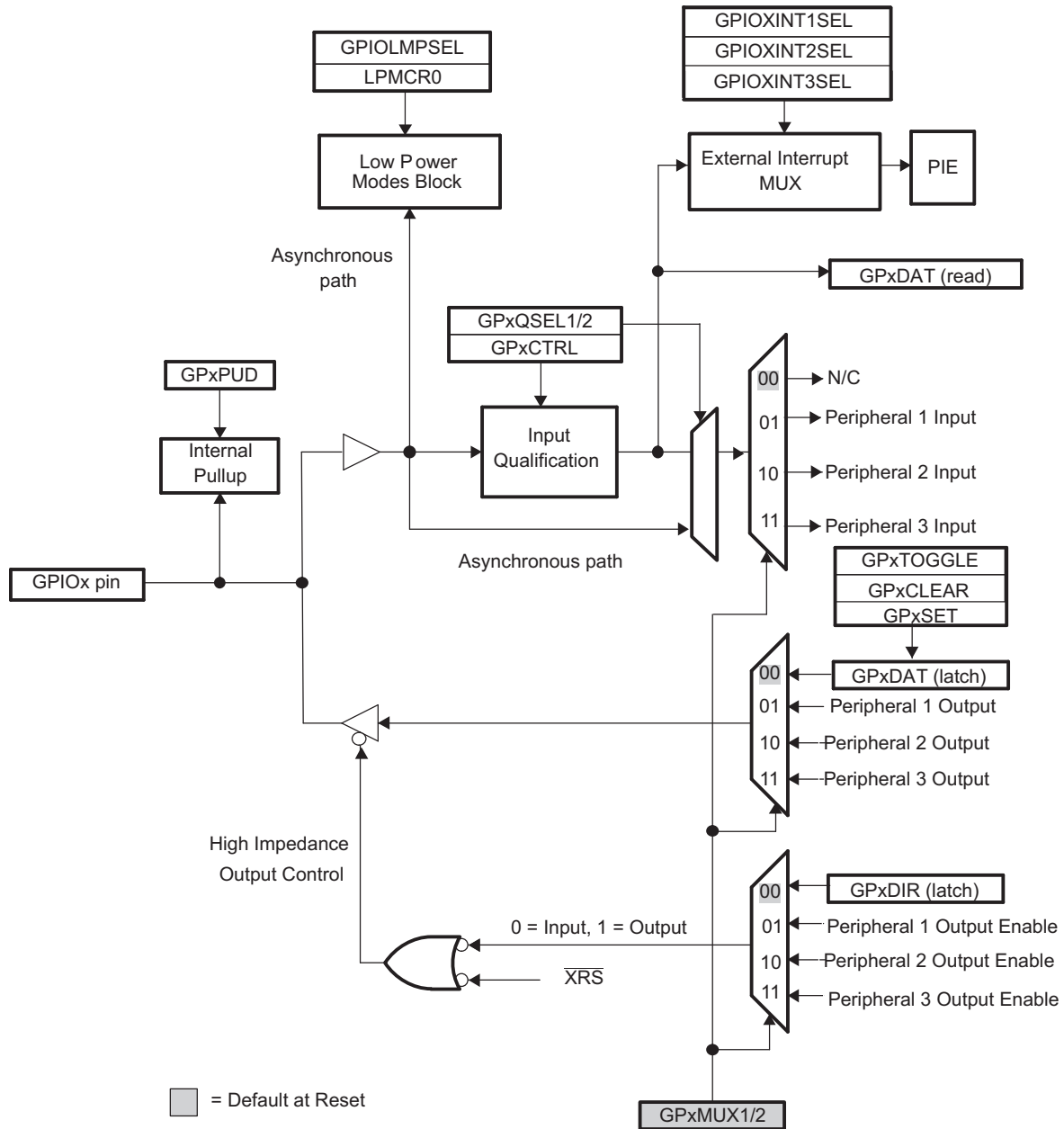
| | | DEFAULT AT RESET |
|-----------------------|---------------------------------|--|
| | AIOx AND PERIPHERAL SELECTION 1 | PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3 |
| AIOMUX1 REGISTER BITS | AIOMUX1 BITS = 0,x | AIOMUX1 BITS = 1,x |
| 1-0 | ADCINA0 (I) | ADCINA0 (I) |
| 3-2 | ADCINA1 (I) | ADCINA1 (I) |
| 5-4 | AIO2 (I/O) | Reserved |
| 7-6 | Reserved | Reserved |
| 9-8 | AIO4 (I/O) | Reserved |
| 11-10 | Reserved | Reserved |
| 13-12 | AIO6 (I/O) | Reserved |
| 15-14 | Reserved | Reserved |
| 17-16 | ADCINB0 (I) | ADCINB0 (I) |
| 19-18 | ADCINB1 (I) | ADCINB1 (I) |
| 21-20 | AIO10 (I/O) | Reserved |
| 23-22 | Reserved | Reserved |
| 25-24 | AIO12 (I/O) | Reserved |
| 27-26 | Reserved | Reserved |
| 29-28 | AIO14 (I/O) | Reserved |
| 31-30 | Reserved | Reserved |

(1) I = Input, O = Output

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2 = 0, 0): This mode is the default mode of all GPIO pins at reset and this mode simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. The sampling period specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in [Figure 5-45](#) (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more than one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.



- A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.
- B. GPxDAT latch/read are accessed at the same memory location.
- C. This diagram is a generic GPIO MUX block diagram. Not all options may be applicable for all GPIO pins.

Figure 5-43. GPIO Multiplexing

5.7.4.11.1 GPIO Electrical Data/Timing

5.7.4.11.1.1 GPIO Output Timing

Table 5-57. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------|---------------------------------------|-----|-------------------|------|
| $t_{r(GPO)}$ | Rise time, GPIO switching low to high | | 13 ⁽¹⁾ | ns |
| $t_{f(GPO)}$ | Fall time, GPIO switching high to low | | 13 ⁽¹⁾ | ns |
| f_{GPO} | Toggling frequency | | 22.5 | MHz |

(1) Rise time and fall time vary with electrical loading on I/O pins. Values given in [Table 5-57](#) are applicable for a 40-pF load on I/O pins.

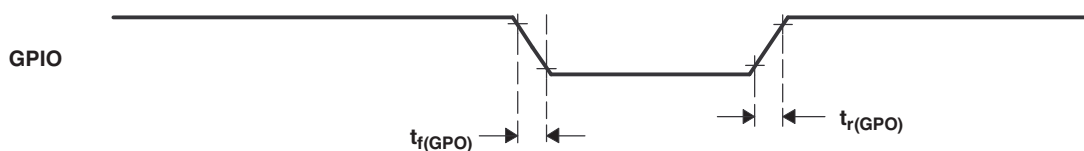


Figure 5-44. General-Purpose Output Timing

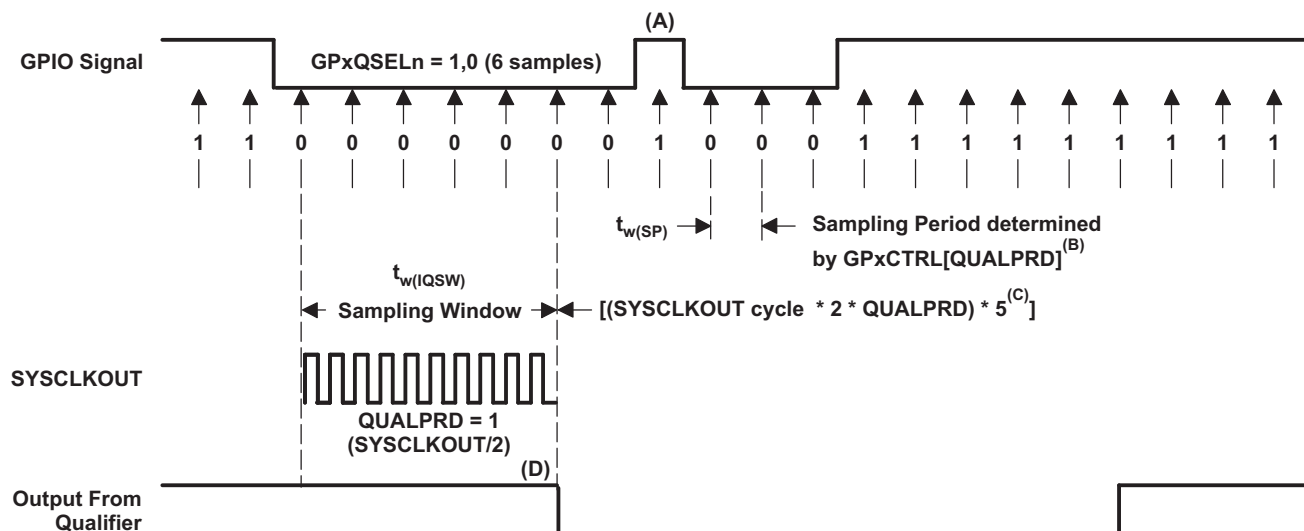
5.7.4.11.1.2 GPIO Input Timing

Table 5-58. General-Purpose Input Timing Requirements

| | | MIN | MAX | UNIT |
|--|----------------------|---|-----|--------|
| $t_{w(SP)}$ Sampling period | QUALPRD = 0 | $1t_{c(SCO)}$ | | cycles |
| | QUALPRD \neq 0 | $2t_{c(SCO)} * QUALPRD$ | | cycles |
| $t_{w(IQSW)}$ Input qualifier sampling window | | $t_{w(SP)} * (n^{(1)} - 1)$ | | cycles |
| $t_{w(GPI)}^{(2)}$ Pulse duration, GPIO low/high | Synchronous mode | $2t_{c(SCO)}$ | | cycles |
| | With input qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$ | | cycles |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.

(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active-low signal and V_{IH} to V_{IH} for an active-high signal.



- This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. The QUALPRD bit field value can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period is 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).
- The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.
- The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for $(5 \times QUALPRD \times 2)$ SYSCLKOUT cycles. This condition would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 5-45. Sampling Mode

5.7.4.11.1.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = $\text{SYSCLKOUT} / (2 * \text{QUALPRD})$, if $\text{QUALPRD} \neq 0$

Sampling frequency = SYSCLKOUT , if $\text{QUALPRD} = 0$

Sampling period = $\text{SYSCLKOUT cycle} \times 2 \times \text{QUALPRD}$, if $\text{QUALPRD} \neq 0$

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle , if $\text{QUALPRD} = 0$

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. The number of samples is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = $(\text{SYSCLKOUT cycle} \times 2 \times \text{QUALPRD}) \times 2$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLKOUT cycle}) \times 2$, if $\text{QUALPRD} = 0$

Case 2:

Qualification using 6 samples

Sampling window width = $(\text{SYSCLKOUT cycle} \times 2 \times \text{QUALPRD}) \times 5$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLKOUT cycle}) \times 5$, if $\text{QUALPRD} = 0$

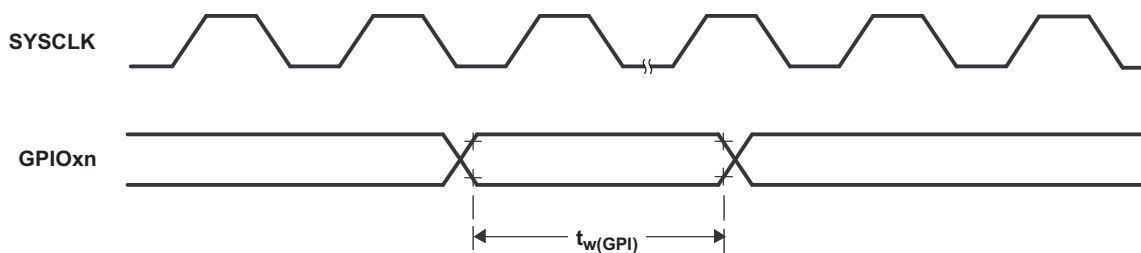


Figure 5-46. General-Purpose Input Timing

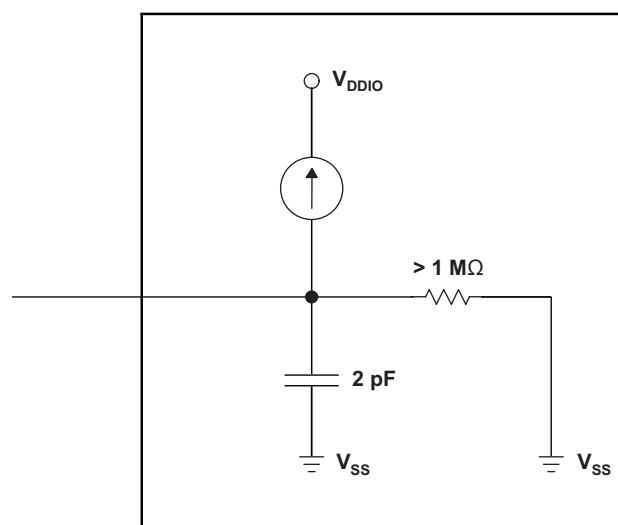


Figure 5-47. Input Resistance Model for a GPIO Pin With an Internal Pullup

5.7.4.11.1.4 Low-Power Mode Wakeup Timing

Table 5-59 shows the timing requirements, Table 5-60 shows the switching characteristics, and Figure 5-48 shows the timing diagram for IDLE mode.

Table 5-59. IDLE Mode Timing Requirements⁽¹⁾

| | | | MIN | MAX | UNIT |
|-------------------|---|-------------------------|-----------------------------|-----|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SCO)}$ | | cycles |
| | | With input qualifier | $5t_{c(SCO)} + t_{w(IQSW)}$ | | |

(1) For an explanation of the input qualifier parameters, see Table 5-58.

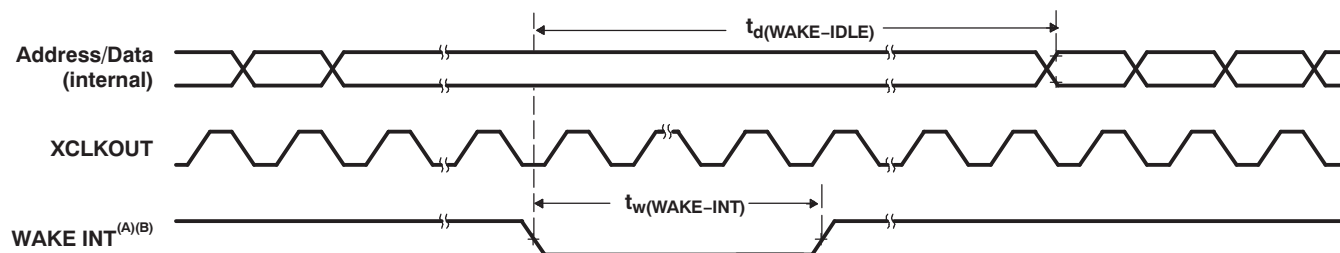
Table 5-60. IDLE Mode Switching Characteristics⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|-------------------------|-----|--------------------------------|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽²⁾ | | | | cycles |
| | • Wake-up from Flash – Flash module in active state | Without input qualifier | | $20t_{c(SCO)}$ | cycles |
| | | With input qualifier | | $20t_{c(SCO)} + t_{w(IQSW)}$ | |
| | • Wake-up from Flash – Flash module in sleep state | Without input qualifier | | $1050t_{c(SCO)}$ | cycles |
| | | With input qualifier | | $1050t_{c(SCO)} + t_{w(IQSW)}$ | |
| | • Wake-up from SARAM | Without input qualifier | | $20t_{c(SCO)}$ | cycles |
| | | With input qualifier | | $20t_{c(SCO)} + t_{w(IQSW)}$ | |

(1) For an explanation of the input qualifier parameters, see Table 5-58.

(2) This delay time is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake-up) signal involves additional latency.



- WAKE INT can be any enabled interrupt, \overline{WDINT} or \overline{XRS} . After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- From the time the IDLE instruction is executed to place the device into low-power mode, wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-48. IDLE Entry and Exit Timing

Table 5-61. STANDBY Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------------|---|---|--|-----|--------|
| t _{w(WAKE-INT)} | Pulse duration, external wake-up signal | Without input qualification | 3t _{c(OSCCLK)} | | cycles |
| | | With input qualification ⁽¹⁾ | (2 + QUALSTDBY) * t _{c(OSCCLK)} | | |

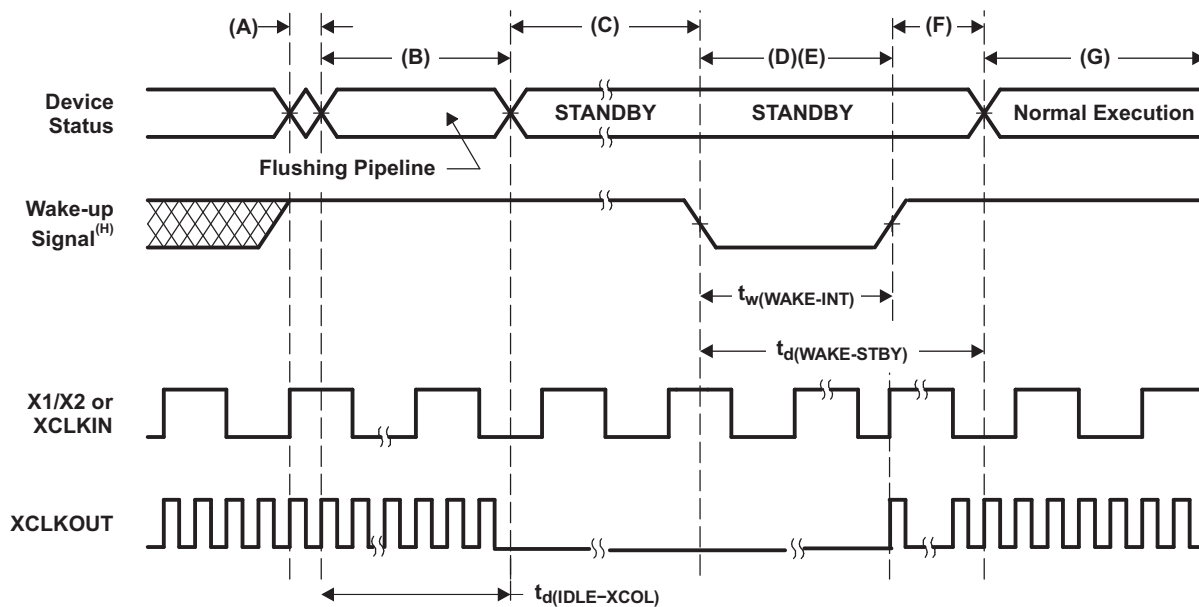
(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 5-62. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------------------|---|-------------------------|--|------------------------|--------|
| t _d (IDLE-XCOL) | Delay time, IDLE instruction executed to XCLKOUT low | | 32t _c (SCO) | 45t _c (SCO) | cycles |
| t _d (WAKE-STBY) | Delay time, external wake signal to program execution resume ⁽¹⁾ | | | | cycles |
| | • Wake up from flash – Flash module in active state | Without input qualifier | 100t _c (SCO) | | cycles |
| | | With input qualifier | 100t _c (SCO) + t _w (WAKE-INT) | | |
| | • Wake up from flash – Flash module in sleep state | Without input qualifier | 1125t _c (SCO) | | cycles |
| | | With input qualifier | 1125t _c (SCO) + t _w (WAKE-INT) | | |
| | • Wake up from SARAM | Without input qualifier | 100t _c (SCO) | | cycles |
| | | With input qualifier | 100t _c (SCO) + t _w (WAKE-INT) | | |

(1) This delay time is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.



- A. IDLE instruction is executed to put the device into STANDBY mode.
- B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for the number of cycles indicated below before being turned off:
 - 16 cycles, when DIVSEL = 00 or 01
 - 32 cycles, when DIVSEL = 10
 - 64 cycles, when DIVSEL = 11
 This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. The external wake-up signal is driven active.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. After a latency period, the STANDBY mode is exited.
- G. Normal execution resumes. The device will respond to the interrupt (if enabled).
- H. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-49. STANDBY Entry and Exit Timing Diagram

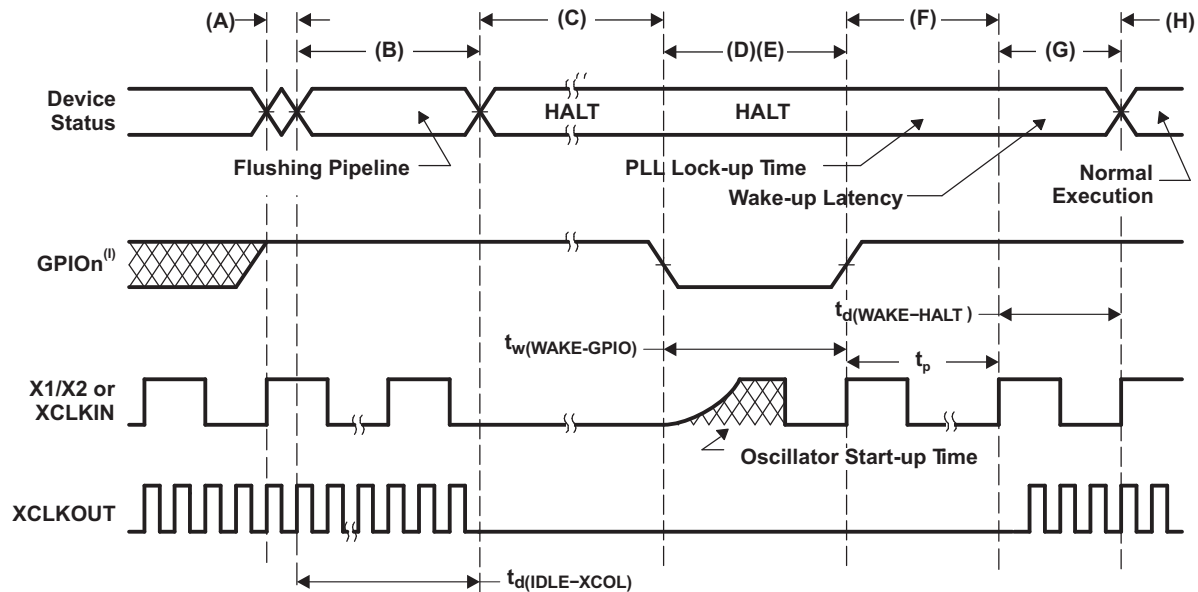
Table 5-63. HALT Mode Timing Requirements

| | | MIN | MAX | UNIT |
|--------------------|--|------------------------------|-----|--------|
| $t_{w(WAKE-GPIO)}$ | Pulse duration, GPIO wake-up signal | $t_{oscst} + 2t_{c(OSCCLK)}$ | | cycles |
| $t_{w(WAKE-XRS)}$ | Pulse duration, \overline{XRS} wakeup signal | $t_{oscst} + 8t_{c(OSCCLK)}$ | | cycles |

Table 5-64. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|---|----------------|------------------|--------|
| $t_{d(IDLE-XCOL)}$ | Delay time, IDLE instruction executed to XCLKOUT low | $32t_{c(SCO)}$ | $45t_{c(SCO)}$ | cycles |
| t_p | PLL lock-up time | | 1 | ms |
| $t_{d(WAKE-HALT)}$ | Delay time, PLL lock to program execution resume | | | |
| | <ul style="list-style-type: none"> • Wake up from flash <ul style="list-style-type: none"> – Flash module in sleep state • Wake up from SARAM | | $1125t_{c(SCO)}$ | cycles |
| | | | $35t_{c(SCO)}$ | cycles |



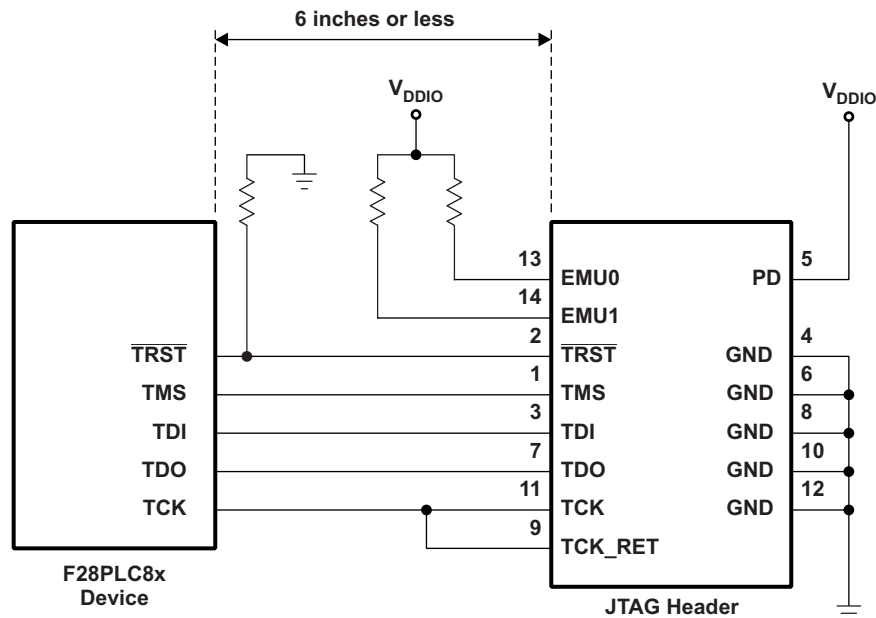
- A. IDLE instruction is executed to put the device into HALT mode.
- B. The PLL block responds to the HALT signal. SYSCLKOUT is held for the number of cycles indicated below before oscillator is turned off and the CLKIN to the core is stopped:
 - 16 cycles, when DIVSEL = 00 or 01
 - 32 cycles, when DIVSEL = 10
 - 64 cycles, when DIVSEL = 11
 This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT mode. Keeping INTOSC1, INTOSC2, and the watchdog alive in HALT mode is done by writing to the appropriate bits in the CLKCTL register. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. When the GPIO pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized, which enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. Once the oscillator has stabilized, the PLL lock sequence is initiated, which takes 1 ms.
- G. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.
- H. Normal operation resumes.
- I. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-50. HALT Wake-Up Using GPIO

5.7.5 Emulation and Debug

5.7.5.1 Emulator Connection Without Signal Buffering for the F28PLC8x Device

Figure 5-51 shows the connection between the F28PLC8x device and JTAG header for a single-processor configuration. If the distance between the JTAG header and the F28PLC8x device is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 5-51 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see Section 4.1, Terminal Functions.



- A. See [Figure 5-42](#) for JTAG/GPIO multiplexing.

Figure 5-51. Emulator Connection Without Signal Buffering for the F28PLC8x Device

NOTE

The F28PLC8x device does not have EMU0/EMU1 pins. For designs that have a JTAG Header on-board, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7-k Ω (typical) resistor.

5.8 Current Consumption

Table 5-65. TMS320F28PLC84, TMS320F28PLC83 Current Consumption at 90-MHz SYSCLKOUT

| MODE | TEST CONDITIONS | VREG ENABLED | | | | | | VREG DISABLED | | | | | | | |
|------------------------|--|----------------------------------|-------|---------------------------------|-------|---------------------|-------|----------------------|-------|----------------------------------|--------|---------------------------------|-------|---------------------|-------|
| | | I _{DDIO} ⁽¹⁾ | | I _{DDA} ⁽²⁾ | | I _{DD3VFL} | | I _{DD} | | I _{DDIO} ⁽¹⁾ | | I _{DDA} ⁽²⁾ | | I _{DD3VFL} | |
| | | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX | TYP ⁽³⁾ | MAX |
| Operational (Flash) | The following peripheral clocks are enabled: <ul style="list-style-type: none">ePWM1, ePWM2eCAP1HRPWMSCI-A, SCI-BSPI-A, SPI-BADCI²CCOMP1, COMP2, COMP3CPU-TIMER0, CPU-TIMER1, CPU-TIMER2McBSP All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected. ⁽⁴⁾ Code is running out of flash with 2 wait-states. XCLKOUT is turned off. | 230 mA | | 16 mA | 22 mA | 25 mA | | 220 mA | | 20 mA | | 16 mA | 22 mA | 25 mA | |
| IDLE | Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off. | 22 mA | 27 mA | 15 μA | 25 μA | 5 μA | 10 μA | 21 mA | 26 mA | 120 μA | 400 μA | 15 μA | 25 μA | 5 μA | 10 μA |
| STANDBY | Flash is powered down. Peripheral clocks are off. | 9 mA | 11 mA | 15 μA | 25 μA | 5 μA | 10 μA | 8 mA | 10 mA | 120 μA | 400 μA | 15 μA | 25 μA | 5 μA | 10 μA |
| HALT | Flash is powered down. Peripheral clocks are off. Input clock is disabled. ⁽⁵⁾ | 75 μA | | 15 μA | 25 μA | 5 μA | 10 μA | 25 μA ⁽⁶⁾ | | 40 μA | | 15 μA | 25 μA | 5 μA | 10 μA |

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.

(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.

(3) The TYP numbers are applicable over room temperature and nominal voltage.

(4) The following is done in a loop:

- Data is continuously transmitted out of SPI-A, SPI-B, SCI-A, McBSP-A, and I²C ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing continuous conversion.
- COMP1 and COMP2 are continuously switching voltages.
- GPIO17 is toggled.

(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

(6) To realize the I_{DD} number shown for HALT mode, the following must be done:

- PLL2 must be shut down by clearing bit 2 of the PLLCTL register.
- A value of 0x00FF must be written to address 0x6822.

NOTE

The peripheral-I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If the clocks to all the peripherals are turned on at the same time, the current drawn by the device will be more than the numbers specified in the current consumption tables.

5.8.1 Reducing Current Consumption

The F28PLC8x device incorporates a method to reduce the device current consumption. Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. [Table 5-66](#) indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 5-66. Typical Current Consumption by Various Peripherals (at 90 MHz)⁽¹⁾

| PERIPHERAL MODULE ⁽²⁾ | I _{DD} CURRENT REDUCTION (mA) |
|-------------------------------------|---|
| ADC | 2 ⁽³⁾ |
| I ² C | 3 |
| ePWM | 2 |
| eCAP | 2 |
| SCI | 2 |
| SPI | 2 |
| COMP/DAC | 1 |
| HRPWM | 3 |
| CPU-TIMER | 1 |
| Internal zero-pin oscillator | 0.5 |
| McBSP | 6 |

- (1) All peripheral clocks (except CPU Timer clock) are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
- (2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.
- (3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 40 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This method results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.

5.8.2 Current Consumption Graphs (VREG Enabled)

Operational Current (Flash) vs Frequency (Internal VREG)

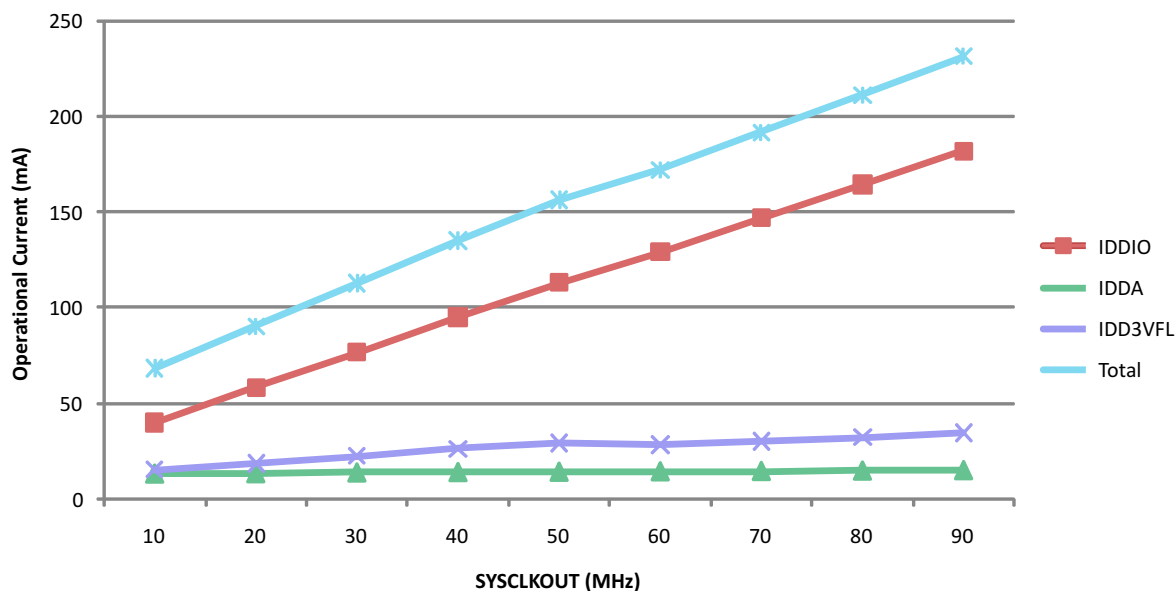


Figure 5-52. Typical Operational Current Versus Frequency

Operational Power vs Frequency (Internal VREG)

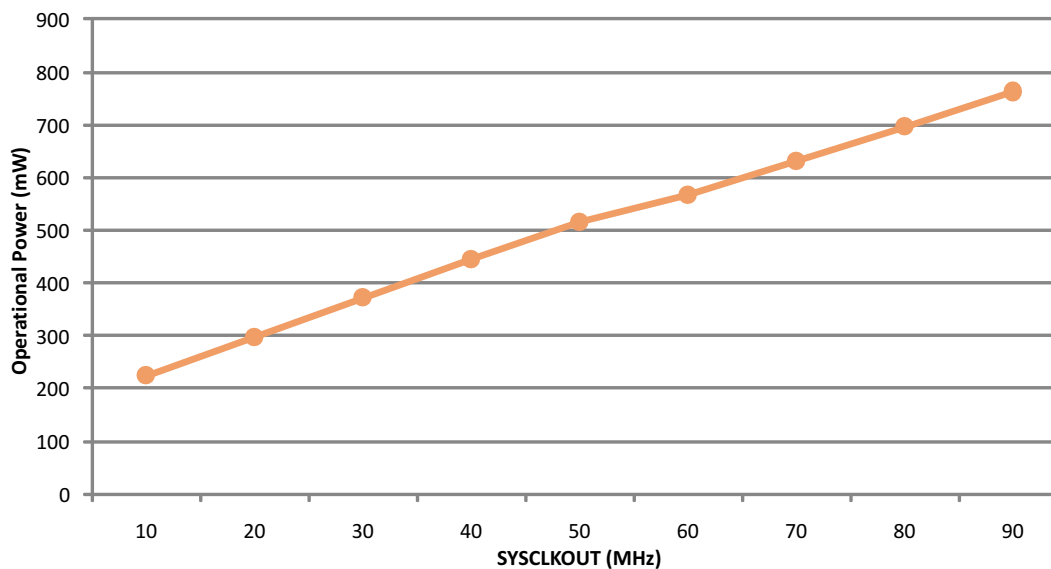


Figure 5-53. Typical Operational Power Versus Frequency

5.9 Parameter Information

5.9.1 Timing Parameter Symbolology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| Lowercase subscripts and their meanings: | | Letters and symbols and their meanings: | |
|--|------------------------|---|--|
| a | access time | H | High |
| c | cycle time (period) | L | Low |
| d | delay time | V | Valid |
| f | fall time | X | Unknown, changing, or don't care level |
| h | hold time | Z | High impedance |
| r | rise time | | |
| su | setup time | | |
| t | transition time | | |
| v | valid time | | |
| w | pulse duration (width) | | |

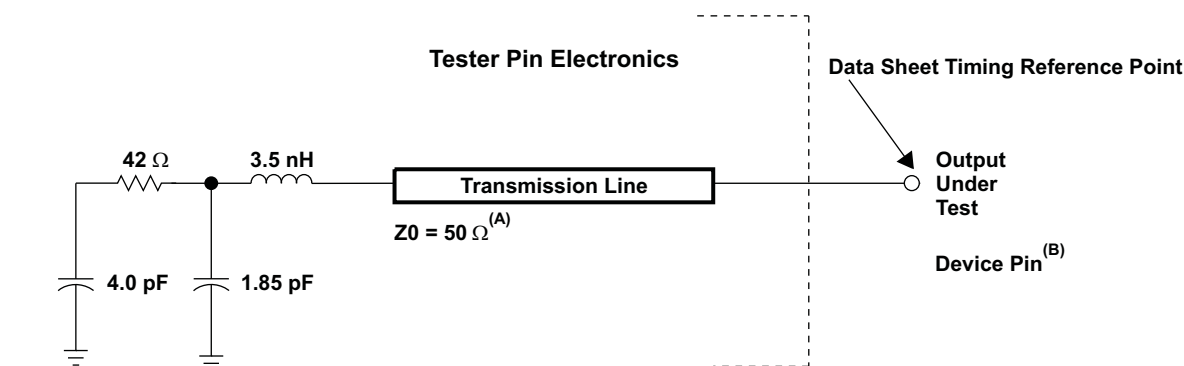
5.9.2 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

5.10 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



- Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.
- The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 5-54. 3.3-V Test Load Circuit

5.11 Flash Timing

Table 5-67. Flash/OTP Endurance for T Temperature Material⁽¹⁾

| | | ERASE/PROGRAM TEMPERATURE | MIN | TYP | MAX | UNIT |
|-----------|--|---------------------------|-------|-------|-----|--------|
| N_f | Flash endurance for the array (write/erase cycles) | 0°C to 105°C (ambient) | 20000 | 50000 | | cycles |
| N_{OTP} | OTP endurance for the array (write cycles) | 0°C to 30°C (ambient) | | | 1 | write |

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

Table 5-68. Flash Parameters at 90-MHz SYSCLKOUT

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------|-----|-----|-----|------|
| Program Time | 16-Bit Word | | | 50 | | μs |
| | 16K Sector | | | 500 | | ms |
| | 8K Sector | | | 250 | | ms |
| | 4K Sector | | | 125 | | ms |
| Erase Time ⁽¹⁾ | 16K Sector | | | 2 | | s |
| | 8K Sector | | | 2 | | s |
| | 4K Sector | | | 2 | | s |
| I_{DDP} ⁽²⁾ | V_{DD} current consumption during Erase/Program cycle | VREG disabled | | 80 | | mA |
| I_{DDIOP} ⁽²⁾ | V_{DDIO} current consumption during Erase/Program cycle | | | 60 | | |
| I_{DDIOP} ⁽²⁾ | V_{DDIO} current consumption during Erase/Program cycle | VREG enabled | | 120 | | mA |

(1) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(2) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the Recommended Operating Conditions of the data sheet. Any brown-out or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently.

Table 5-69. Flash/OTP Access Timing⁽¹⁾

| PARAMETER | | MIN | MAX | UNIT |
|--------------|--------------------------|-----|-----|------|
| $t_{a(fp)}$ | Paged Flash access time | 36 | | ns |
| $t_{a(fr)}$ | Random Flash access time | 36 | | ns |
| $t_{a(OTP)}$ | OTP access time | 60 | | ns |

(1) Access time numbers shown in this table are prior to device characterization. Final numbers will be published in the TMS datasheet.

Table 5-70. Flash Data Retention Duration

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|-------------------------|--------------------------|-----|-----|-------|
| $t_{retention}$ | Data retention duration | $T_J = 55^\circ\text{C}$ | 15 | | years |

Table 5-71. Minimum Required Flash/OTP Wait-States at Different Frequencies

| SYCLKOUT (MHz) | SYCLKOUT (ns) | PAGE WAIT-STATE⁽¹⁾ | RANDOM WAIT-STATE⁽¹⁾ | OTP WAIT-STATE |
|---------------------------|--------------------------|--|--|---------------------------|
| 90 | 11.11 | 3 | 3 | 5 |
| 80 | 12.5 | 2 | 2 | 4 |
| 70 | 14.29 | 2 | 2 | 4 |
| 60 | 16.67 | 2 | 2 | 3 |
| 55 | 18.18 | 1 | 1 | 3 |
| 50 | 20 | 1 | 1 | 2 |
| 45 | 22.22 | 1 | 1 | 2 |
| 40 | 25 | 1 | 1 | 2 |
| 35 | 28.57 | 1 | 1 | 2 |
| 30 | 33.33 | 1 | 1 | 1 |

(1) Page and random wait-state must be ≥ 1 .

The equations to compute the Flash page wait-state and random wait-state in [Table 5-71](#) are as follows:

$$\text{Flash Page Wait State} = \left\lceil \left(\frac{t_{a(f.p)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer, or 1, whichever is larger}$$

$$\text{Flash Random Wait State} = \left\lceil \left(\frac{t_{a(f.r)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer, or 1, whichever is larger}$$

The equation to compute the OTP wait-state in [Table 5-71](#) is as follows:

$$\text{OTP Wait State} = \left\lceil \left(\frac{t_{a(OTP)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer, or 1, whichever is larger}$$

6 Detailed Description

6.1 Overview

6.1.1 CPU

The TMS320F28PLCx (C28x) family is a member of the TMS320C2000™ MCU platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. Each C28x-based controller, including the TMS320F28PLC8x device, is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is equally efficient at MCU math tasks and at system control tasks. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit multiply-and-accumulate (MAC) 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this feature the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the device to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

6.1.2 Viterbi, Complex Math, CRC Unit

The C28x VCU enhances the processing power of C2000™ devices by adding additional assembly instructions to target complex math, Viterbi decode, and Cyclic Redundancy Check (CRC) calculations. The VCU instructions accelerate many applications, including the following:

- OFDM used in the PRIME and G3 standards for power line communications
- Short-range radar complex math calculations
- Power calculations
- Memory and data communication packet checks (CRC)

The VCU features include:

- Instructions to support Cyclic Redundancy Checks, which is a polynomial code checksum.
 - CRC8
 - CRC16
 - CRC32
- Instructions to support a flexible software implementation of a Viterbi decoder
 - Branch metric calculations for a code rate of 1/2 or 1/3
 - Add-Compare Select or Viterbi Butterfly in 5 cycles per butterfly
 - Traceback in 3 cycles per stage
 - Easily supports a constraint length of K = 7 used in PRIME and G3 standards
- Complex math arithmetic unit
 - Single-cycle Add or Subtract
 - 2-cycle multiply
 - 2-cycle MAC
 - Single-cycle repeat MAC
- Independent register space

6.1.3 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

| | | |
|----------|----------------|--|
| Highest: | Data Writes | (Simultaneous data and program writes cannot occur on the memory bus.) |
| | Program Writes | (Simultaneous data and program writes cannot occur on the memory bus.) |
| | Data Reads | |
| | Program Reads | (Simultaneous program reads and fetches cannot occur on the memory bus.) |
| Lowest: | Fetches | (Simultaneous program reads and fetches cannot occur on the memory bus.) |

6.1.4 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the device adopts a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1).

6.1.5 Real-Time JTAG and Analysis

The device implements the standard IEEE 1149.1 JTAG ⁽¹⁾ interface for in-circuit based debug. Additionally, the device supports real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This feature is unique to the 28x family of devices, and requires no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs. This device does not support boundary scan; however, IDCODE and BYPASS features are available if the following considerations are taken into account. The IDCODE does not come by default. The user needs to go through a sequence of SHIFT IR and SHIFT DR state of JTAG to get the IDCODE. For BYPASS instruction, the first shifted DR value would be 1.

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

6.1.6 Flash

The F28PLC8x device contains 128K x 16 of embedded flash memory, segregated into eight 16K x 16 sectors. The device also contains a single 1K x 16 of OTP memory at address range 0x3D 7800 – 0x3D 7BF9. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, the flash/OTP can be used to execute code or store data information. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data variables and should not contain program code.

NOTE

The Flash and OTP wait-states can be configured by the application. This feature allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

6.1.7 M0, M1 SARAMs

The device contains these two blocks of single-access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer, which makes for easier programming in high-level languages.

6.1.8 L4 SARAM, and L0, L1, L2, L3, L5, L6, L7, and L8 DPSARAMs

The device contains 48K x 16 of single-access RAM. This block is mapped to both program and data space. L0 is 2K in size. L1 and L2 are each 1K in size. L3 is 4K in size. L4, L5, L6, L7, and L8 are each 8K in size. L5, L6, L7, and L8 are shared with the DMA, which can utilize these blocks for its data space. See [Figure 6-5](#). DPSARAM refers to the dual-port configuration of these blocks.

6.1.9 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 6-1. Boot Mode Selection

| MODE | GPIO37/TDO | GPIO34/COMP2OUT/ COMP3OUT | TRST | MODE |
|------|------------|------------------------------|------|---|
| 3 | 1 | 1 | 0 | GetMode |
| 2 | 1 | 0 | 0 | Wait (see Section 6.1.10 for description) |
| 1 | 0 | 1 | 0 | SCI |
| 0 | 0 | 0 | 0 | Parallel IO |
| EMU | x | x | 1 | Emulation Boot |

6.1.9.1 Emulation Boot

When the emulator is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that an emulator is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in emulation boot.

6.1.9.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I²C, or OTP.

6.1.9.3 Peripheral Pins Used by the Bootloader

Table 6-2 shows which GPIO pins are used by each peripheral bootloader. Refer to the GPIO mux table to see if these conflict with any of the peripherals you would like to use in your application.

Table 6-2. Peripheral Bootload Pins

| BOOTLOADER | PERIPHERAL LOADER PINS |
|------------------|--|
| SCI | SCIRXDA (GPIO28) SCITXDA (GPIO29) |
| Parallel Boot | Data (GPIO31,30,5:0) 28x Control (AIO6) Host Control (AIO12) |
| SPI | SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) SPISTEA (GPIO19) |
| I ² C | SDAA (GPIO32) SCLA (GPIO33) |

6.1.10 Security

The F28PLC8x device supports high levels of security to protect the user firmware from being reverse-engineered. The security features a 128-bit password (hardcoded for 16 wait-states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to CSM secure memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the flash. Note that dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in flash programmed (that is, secured), the CPU will start running and may execute an instruction that performs an access to a protected ECSL area. If this event occurs, the ECSL will trip and cause the emulator connection to be cut.

The solution is to use the *Wait* boot option. The *Wait* boot option will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. The F28PLC8x device does not support a hardware wait-in-reset mode.

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F 7F80 and 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 through 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data and should not contain program code.

The 128-bit password (at 0x3F 7FF8 – 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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6.1.11 Peripheral Interrupt Expansion Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F28PLCx, 72 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. Eight CPU clock cycles are needed to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled or disabled within the PIE block.

6.1.12 External Interrupts (XINT1–XINT3)

The F28PLC8x device supports three masked external interrupts (XINT1–XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled or disabled. These interrupts also contain a 16-bit free-running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time-stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0–GPIO31 pins.

6.1.13 Internal Zero Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 16 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to [Section 5](#), Electrical Specifications, for timing details. The PLL block can be set in bypass mode.

6.1.14 Watchdog

The device contains two watchdogs: CPU-Watchdog that monitors the core and NMI-Watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-Watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

6.1.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled or disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I²C) can be scaled relative to the CPU clock.

6.1.16 Low-power Modes

The F28PLC8x device is a full static CMOS device. Three low-power modes are provided:

- IDLE:** Places CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
- STANDBY:** Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
- HALT:** This mode basically shuts down the device and places the device in the lowest possible power-consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, this oscillator is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU-watchdog can wake the device from this mode.

The CPU clock (OSCCLK) and WDCLK should be from the same clock source before attempting to put the device into HALT or STANDBY.

6.1.17 Peripheral Frames 0, 1, 2, 3 (PFn)

The device segregates peripherals into four sections. The mapping of peripherals is as follows:

- PF0:
 - PIE: PIE Interrupt Enable and Control Registers Plus PIE Vector Table
 - Flash: Flash Waitstate Registers
 - Timers: CPU-Timers 0, 1, 2 Registers
 - CSM: Code Security Module KEY Registers
 - ADC: ADC Result Registers
- PF1: GPIO: GPIO MUX Configuration and Control Registers
- PF2:
 - SYS: System Control Registers
 - SCI: Serial Communications Interface Control and RX/TX Registers
 - SPI: Serial Port Interface Control and RX/TX Registers
 - ADC: ADC Status, Control, and Configuration Registers
 - I²C: Inter-Integrated Circuit Module and Registers
 - XINT: External Interrupt Registers
- PF3:
 - McBSP: Multichannel Buffered Serial Port Registers
 - ePWM: Enhanced Pulse Width Modulator Module and Registers
 - eCAP: Enhanced Capture Module and Registers
 - Comparators: Comparator Modules

6.1.18 General-Purpose Input/Output Multiplexer

Most of the peripheral signals are multiplexed with GPIO signals. This muxing enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This selection is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

6.1.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, the counter is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and can be connected to INT13 of the CPU. CPU-Timer 2 is reserved for DSP/BIOS™. CPU-Timer 2 is connected to INT14 of the CPU. If DSP/BIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTSOC2)
- External clock source

6.1.20 Control Peripherals

The F28PLC8x device supports the following peripherals that are used for embedded control and communication:

| | |
|-------------|--|
| ePWM: | The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high resolution duty and period features. The type 1 module found on the F28PLC8x device also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs. |
| eCAP: | The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal. |
| ADC: | The ADC block is a 12-bit converter. The ADC has 13 single-ended channels pinned out. The ADC also contains two sample-and-hold units for simultaneous sampling. |
| Comparator: | Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator. |

6.1.21 Serial Port Peripherals

The F28PLC8x device supports the following serial communication peripherals:

- SPI:** The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the device and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
- SCI:** The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.
- I²C:** The inter-integrated circuit module provides an interface between a device and other devices compliant with Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1 and connected by way of an I²C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit data to and from the device through the I²C module. The I²C contains a 4-level receive-and-transmit FIFO for reducing interrupt servicing overhead.
- McBSP:** The multichannel buffered serial port connects to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo audio DAC devices. The McBSP receive and transmit registers are supported by the DMA to significantly reduce the overhead for servicing this peripheral. Each McBSP module can be configured as an SPI as required.

6.1.22 VREG, BOR, POR

Although the core and I/O circuitry operate on two different voltages, the F28PLC8x device has an on-chip voltage regulator (VREG) to generate the V_{DD} voltage from the V_{DDIO} supply. This feature eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode.

6.1.22.1 On-chip Voltage Regulator

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

6.1.22.1.1 Using the On-chip VREG

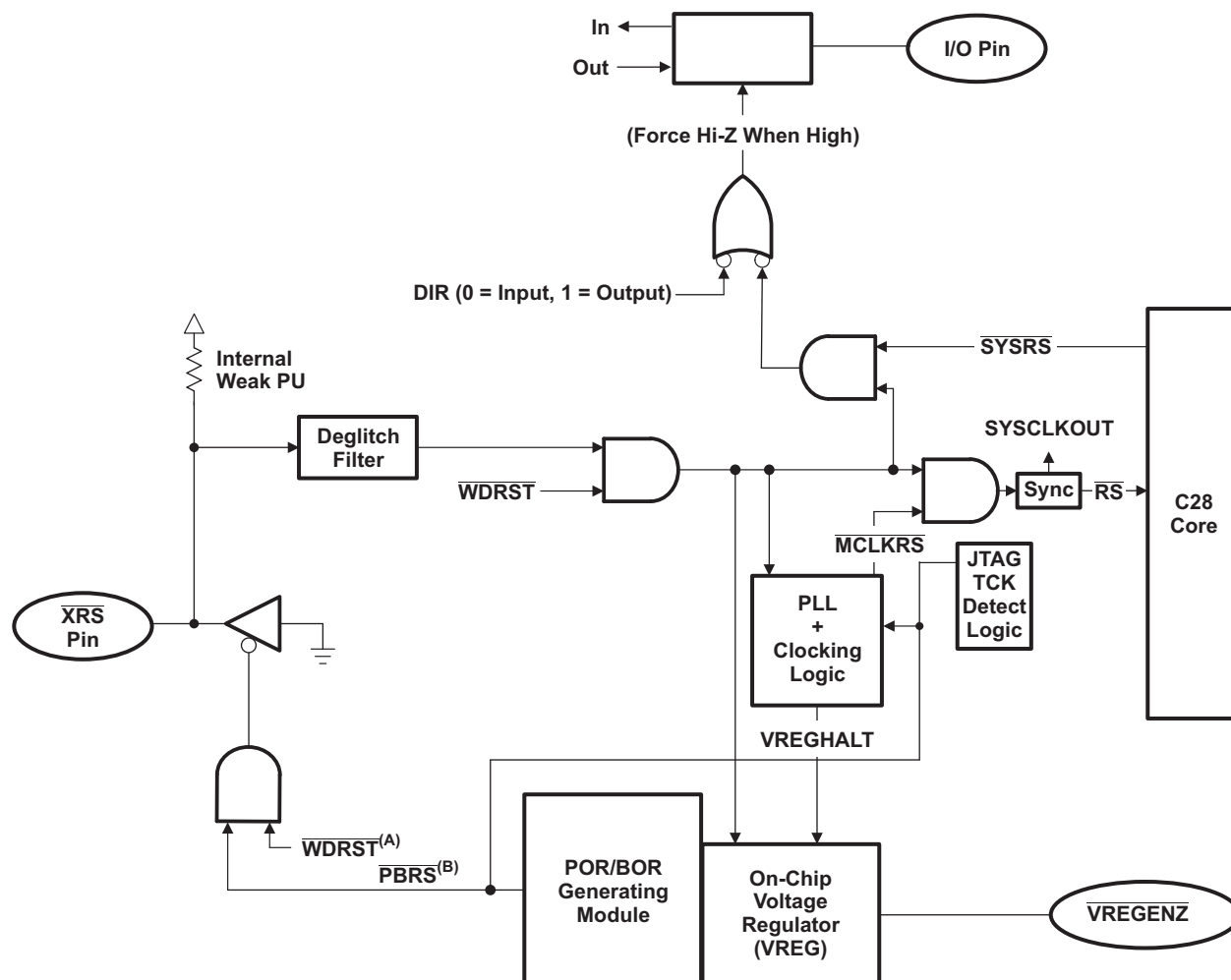
To utilize the on-chip VREG, the $\overline{\text{VREGENZ}}$ pin should be tied low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 μF (minimum) capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins.

6.1.22.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{\text{VREGENZ}}$ pin must be tied high.

6.1.22.2 On-chip Power-On Reset and Brown-Out Reset Circuit

Two on-chip supervisory circuits, the POR and the BOR remove the burden of monitoring the V_{DD} and V_{DDIO} supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{\text{VREGENZ}}$ pin is tied low). Both functions tie the $\overline{\text{XRS}}$ pin low when one of the voltages is below their respective trip point. Additionally, when the internal voltage regulator is enabled, an over-voltage protection circuit will tie $\overline{\text{XRS}}$ low if the V_{DD} rail rises above its trip point. See [Section 5](#) for the various trip points as well as the delay time for the device to release the $\overline{\text{XRS}}$ pin after the under/over-voltage condition is removed. [Figure 6-1](#) shows the VREG, POR, and BOR. To disable both the V_{DD} and V_{DDIO} BOR functions, a bit is provided in the BORCFG register.



- A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.
 B. $\overline{\text{PBRST}}$ is the reset signal from the POR/BOR module.

Figure 6-1. VREG + POR + BOR + Reset Signal Connectivity

6.1.23 Interrupts

Figure 6-2 shows how the various interrupt sources are multiplexed.

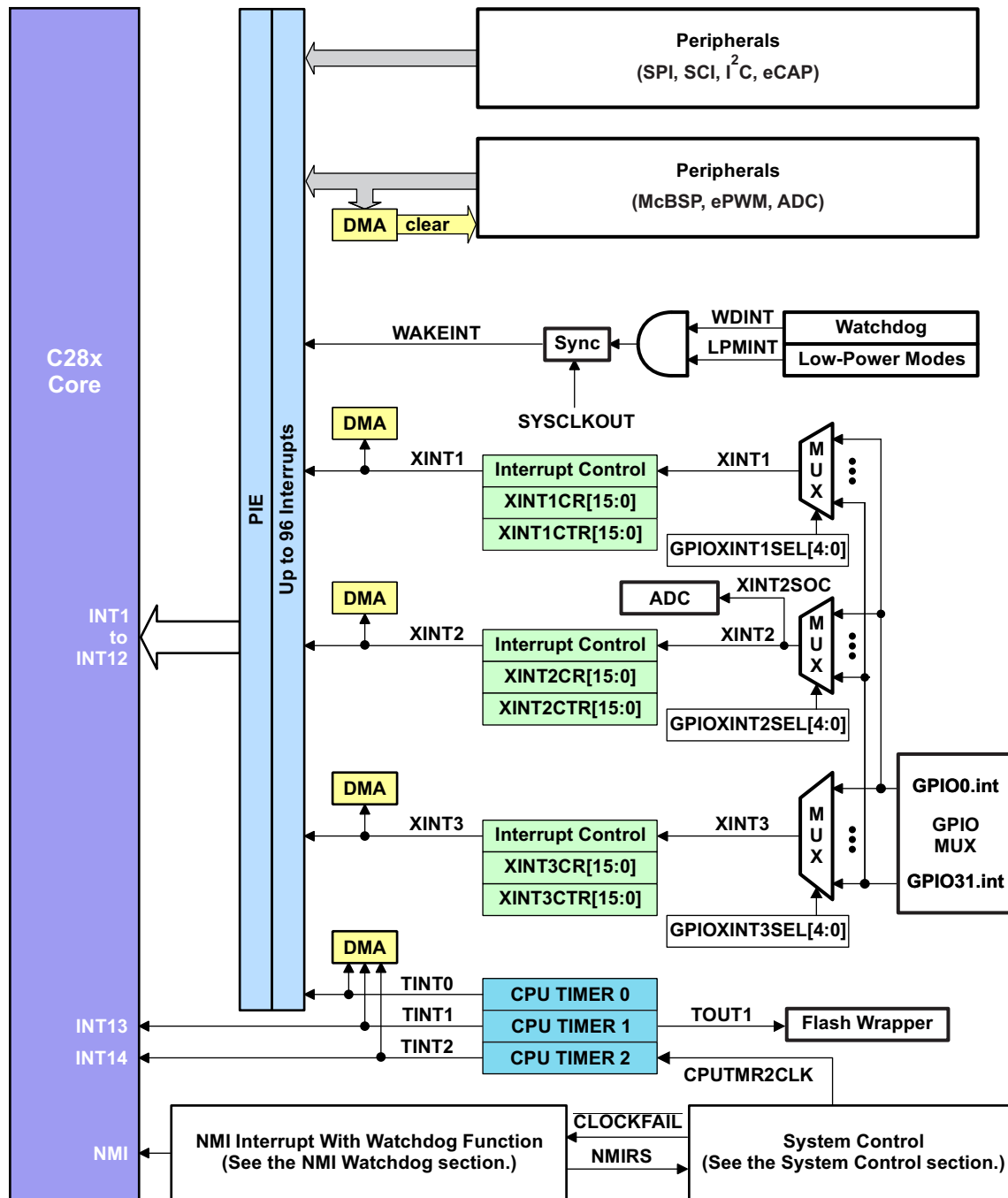


Figure 6-2. External and PIE Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 6-3 shows the interrupts used by the F28PLC8x device.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1, and so forth.

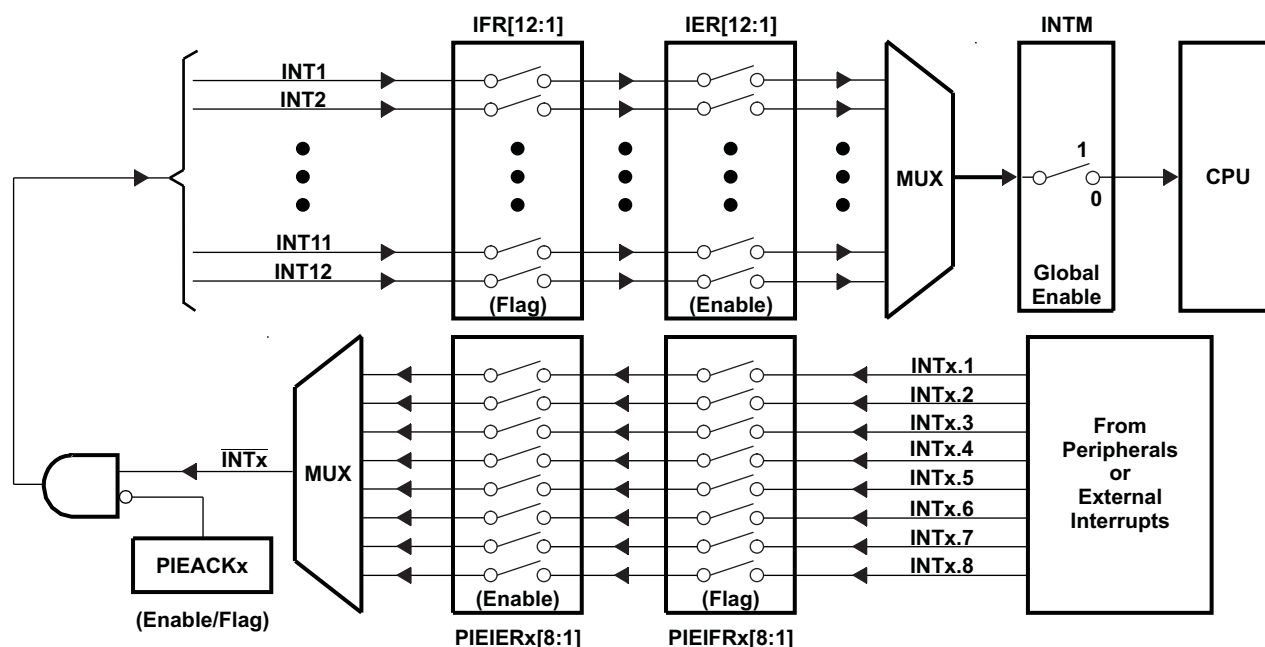


Figure 6-3. Multiplexing of Interrupts Using the PIE Block

Table 6-3. PIE MUXed Peripheral Interrupt Vector Table⁽¹⁾

| | INTx.8 | INTx.7 | INTx.6 | INTx.5 | INTx.4 | INTx.3 | INTx.2 | INTx.1 |
|---------|------------------------------|-----------------------------|------------------------------|-------------------------------|-------------------------------|-------------------------------|---------------------------------|---------------------------------|
| INT1.y | WAKEINT (LPM/WD) 0xD4E | TINT0 (TIMER 0) 0xD4C | ADCINT9 (ADC) 0xD4A | XINT2 Ext. int. 2 0xD48 | XINT1 Ext. int. 1 0xD46 | Reserved – 0xD44 | ADCINT2 (ADC) 0xD42 | ADCINT1 (ADC) 0xD40 |
| INT2.y | Reserved – 0xD5E | Reserved – 0xD5C | Reserved – 0xD5A | Reserved – 0xD58 | Reserved – 0xD56 | Reserved – 0xD54 | EPWM2_TZINT (ePWM2) 0xD52 | EPWM1_TZINT (ePWM1) 0xD50 |
| INT3.y | Reserved – 0xD6E | Reserved – 0xD6C | Reserved – 0xD6A | Reserved – 0xD68 | Reserved – 0xD66 | Reserved – 0xD64 | EPWM2_INT (ePWM2) 0xD62 | EPWM1_INT (ePWM1) 0xD60 |
| INT4.y | Reserved – 0xD7E | Reserved – 0xD7C | Reserved – 0xD7A | Reserved – 0xD78 | Reserved – 0xD76 | Reserved – 0xD74 | Reserved – 0xD72 | ECAP1_INT (eCAP1) 0xD70 |
| INT5.y | Reserved – 0xD8E | Reserved – 0xD8C | Reserved – 0xD8A | Reserved – 0xD88 | Reserved – 0xD86 | Reserved – 0xD84 | Reserved – 0xD82 | Reserved – 0xD80 |
| INT6.y | Reserved – 0xD9E | Reserved – 0xD9C | MXINTA (McBSP-A) 0xD9A | MRINTA (McBSP-A) 0xD98 | SPITXINTB (SPI-B) 0xD96 | SPIRXINTB (SPI-B) 0xD94 | SPITXINTA (SPI-A) 0xD92 | SPIRXINTA (SPI-A) 0xD90 |
| INT7.y | Reserved – 0xDAE | Reserved – 0xDAC | DINTCH6 (DMA) 0xDAA | DINTCH5 (DMA) 0xDA8 | DINTCH4 (DMA) 0xDA6 | DINTCH3 (DMA) 0xDA4 | DINTCH2 (DMA) 0xDA2 | DINTCH1 (DMA) 0xDA0 |
| INT8.y | Reserved – 0xDBE | Reserved – 0xDBC | Reserved – 0xDBA | Reserved – 0xDB8 | Reserved – 0xDB6 | Reserved – 0xDB4 | I2CINT2A (I2C-A) 0xDB2 | I2CINT1A (I2C-A) 0xDB0 |
| INT9.y | Reserved – 0xDCE | Reserved – 0xDCC | Reserved – 0xDCA | Reserved – 0xDC8 | SCITXINTB (SCI-B) 0xDC6 | SCIRXINTB (SCI-B) 0xDC4 | SCITXINTA (SCI-A) 0xDC2 | SCIRXINTA (SCI-A) 0xDC0 |
| INT10.y | ADCINT8 (ADC) 0xDDE | ADCINT7 (ADC) 0xDDC | ADCINT6 (ADC) 0xDDA | ADCINT5 (ADC) 0xDD8 | ADCINT4 (ADC) 0xDD6 | ADCINT3 (ADC) 0xDD4 | ADCINT2 (ADC) 0xDD2 | ADCINT1 (ADC) 0xDD0 |
| INT11.y | Reserved – 0xDEE | Reserved – 0xDEC | Reserved – 0xDEA | Reserved – 0xDE8 | Reserved – 0xDE6 | Reserved – 0xDE4 | Reserved – 0xDE2 | Reserved – 0xDE0 |
| INT12.y | Reserved – 0xDFE | Reserved – 0xDFC | Reserved – 0xDFA | Reserved – 0xDF8 | Reserved – 0xDF6 | Reserved – 0xDF4 | Reserved – 0xDF2 | XINT3 Ext. Int. 3 0xDF0 |

(1) Out of 96 possible interrupts, some interrupts are not used. These interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:

- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (for example, PIE group 7).

Table 6-4. PIE Configuration and Control Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION ⁽¹⁾ |
|----------|--------------------|------------|----------------------------------|
| PIECTRL | 0x0CE0 | 1 | PIE, Control Register |
| PIEACK | 0x0CE1 | 1 | PIE, Acknowledge Register |
| PIEIER1 | 0x0CE2 | 1 | PIE, INT1 Group Enable Register |
| PIEIFR1 | 0x0CE3 | 1 | PIE, INT1 Group Flag Register |
| PIEIER2 | 0x0CE4 | 1 | PIE, INT2 Group Enable Register |
| PIEIFR2 | 0x0CE5 | 1 | PIE, INT2 Group Flag Register |
| PIEIER3 | 0x0CE6 | 1 | PIE, INT3 Group Enable Register |
| PIEIFR3 | 0x0CE7 | 1 | PIE, INT3 Group Flag Register |
| PIEIER4 | 0x0CE8 | 1 | PIE, INT4 Group Enable Register |
| PIEIFR4 | 0x0CE9 | 1 | PIE, INT4 Group Flag Register |
| PIEIER5 | 0x0CEA | 1 | PIE, INT5 Group Enable Register |
| PIEIFR5 | 0x0CEB | 1 | PIE, INT5 Group Flag Register |
| PIEIER6 | 0x0CEC | 1 | PIE, INT6 Group Enable Register |
| PIEIFR6 | 0x0CED | 1 | PIE, INT6 Group Flag Register |
| PIEIER7 | 0x0CEE | 1 | PIE, INT7 Group Enable Register |
| PIEIFR7 | 0x0CEF | 1 | PIE, INT7 Group Flag Register |
| PIEIER8 | 0x0CF0 | 1 | PIE, INT8 Group Enable Register |
| PIEIFR8 | 0x0CF1 | 1 | PIE, INT8 Group Flag Register |
| PIEIER9 | 0x0CF2 | 1 | PIE, INT9 Group Enable Register |
| PIEIFR9 | 0x0CF3 | 1 | PIE, INT9 Group Flag Register |
| PIEIER10 | 0x0CF4 | 1 | PIE, INT10 Group Enable Register |
| PIEIFR10 | 0x0CF5 | 1 | PIE, INT10 Group Flag Register |
| PIEIER11 | 0x0CF6 | 1 | PIE, INT11 Group Enable Register |
| PIEIFR11 | 0x0CF7 | 1 | PIE, INT11 Group Flag Register |
| PIEIER12 | 0x0CF8 | 1 | PIE, INT12 Group Enable Register |
| PIEIFR12 | 0x0CF9 | 1 | PIE, INT12 Group Flag Register |
| Reserved | 0x0CFA – 0x0CFF | 6 | Reserved |

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

6.1.23.1 External Interrupts

Table 6-5. External Interrupt Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION |
|----------|-----------|------------|------------------------------|
| XINT1CR | 0x00 7070 | 1 | XINT1 configuration register |
| XINT2CR | 0x00 7071 | 1 | XINT2 configuration register |
| XINT3CR | 0x00 7072 | 1 | XINT3 configuration register |
| XINT1CTR | 0x00 7078 | 1 | XINT1 counter register |
| XINT2CTR | 0x00 7079 | 1 | XINT2 counter register |
| XINT3CTR | 0x00 707A | 1 | XINT3 counter register |

Each external interrupt can be enabled, disabled, or qualified using positive, negative, or both positive and negative edge.

6.1.23.1.1 External Interrupt Electrical Data/Timing

Table 6-6. External Interrupt Timing Requirements⁽¹⁾

| | | MIN | MAX | UNIT |
|--|----------------|-----------------------------|-----|--------|
| $t_{w(INT)}$ ⁽²⁾ Pulse duration, INT input low/high | Synchronous | $1t_{c(SCO)}$ | | cycles |
| | With qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see [Table 5-58](#).

(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 6-7. External Interrupt Switching Characteristics⁽¹⁾

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|---|------------------------------|-----|--------|
| $t_{d(INT)}$ Delay time, INT low/high to interrupt-vector fetch | $t_{w(IQSW)} + 12t_{c(SCO)}$ | | cycles |

(1) For an explanation of the input qualifier parameters, see [Table 5-58](#).

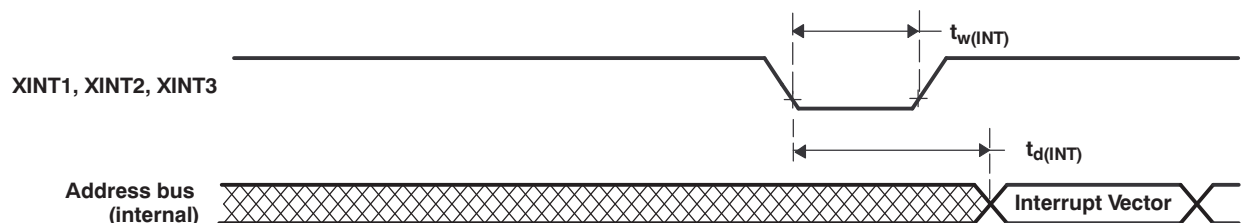


Figure 6-4. External Interrupt Timing

6.2 Memory

6.2.1 Memory Map

In [Figure 6-5](#), the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.
- Locations 0x3D 7C80–0x3D 7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.

| | Data Space | Prog Space |
|-----------|---|------------|
| 0x00 0000 | <i>M0 Vector RAM (Enabled if VMAP = 0)</i> | |
| 0x00 0040 | M0 SARAM (1K x 16, 0-Wait) | |
| 0x00 0400 | M1 SARAM (1K x 16, 0-Wait) | |
| 0x00 0800 | Peripheral Frame 0 | Reserved |
| 0x00 0D00 | <div>PIE Vector - RAM (256 x 16) (Enabled if VMAP = 1, ENPIE = 1)</div> | |
| 0x00 0E00 | Peripheral Frame 0 | |
| 0x00 1400 | Reserved | |
| 0x00 5000 | Peripheral Frame 3 (4K x 16, Protected) DMA-Accessible | Reserved |
| 0x00 6000 | Peripheral Frame 1 (4K x 16, Protected) | |
| 0x00 7000 | Peripheral Frame 2 (4K x 16, Protected) | |
| 0x00 8000 | L0 DPSARAM (2K x 16) (0-Wait, Secure Zone + ECSL) | |
| 0x00 8800 | L1 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL) | |
| 0x00 8C00 | L2 DPSARAM (1K x 16) (0-Wait, Secure Zone + ECSL) | |
| 0x00 9000 | L3 DPSARAM (4K x 16) (0-Wait, Secure Zone + ECSL) | |
| 0x00 A000 | L4 SARAM (8K x 16) (0-Wait, Secure Zone + ECSL) | |
| 0x00 C000 | L5 DPSARAM (8K x 16) (0-Wait, DMA RAM 0) | |
| 0x00 E000 | L6 DPSARAM (8K x 16) (0-Wait, DMA RAM 1) | |
| 0x01 0000 | L7 DPSARAM (8K x 16) (0-Wait, DMA RAM 2) | |
| 0x01 2000 | L8 DPSARAM (8K x 16) (0-Wait, DMA RAM 3) | |
| 0x01 4000 | Reserved | |
| 0x3D 7800 | User OTP (1K x 16, Secure Zone + ECSL) | |
| 0x3D 7BFA | Reserved | |
| 0x3D 7C80 | Calibration Data | |
| 0x3D 7CC0 | Get_mode function | |
| 0x3D 7CD0 | Reserved | |
| 0x3D 7E80 | PARTID | |
| | Calibration Data | |
| 0x3D 7EB0 | Reserved | |
| 0x3D 8000 | FLASH (128K x 16, 8 Sectors, Secure Zone + ECSL) | |
| 0x3F 7FF8 | 128-Bit Password | |
| 0x3F 8000 | Boot ROM (32K x 16, 0-Wait) | |
| 0x3F FFC0 | <i>Vector (32 Vectors, Enabled if VMAP = 1)</i> | |

Figure 6-5. F28PLC8x Memory Map

Table 6-8. Addresses of Flash Sectors in F28PLC8x

| ADDRESS RANGE | PROGRAM AND DATA SPACE |
|-----------------------|--|
| 0x3D 8000 – 0x3D BFFF | Sector H (16K x 16) |
| 0x3D C000 – 0x3D FFFF | Sector G (16K x 16) |
| 0x3E 0000 – 0x3E 3FFF | Sector F (16K x 16) |
| 0x3E 4000 – 0x3E 7FFF | Sector E (16K x 16) |
| 0x3E 8000 – 0x3E BFFF | Sector D (16K x 16) |
| 0x3E C000 – 0x3E FFFF | Sector C (16K x 16) |
| 0x3F 0000 – 0x3F 3FFF | Sector B (16K x 16) |
| 0x3F 4000 – 0x3F 7FF5 | Sector A (16K x 16) |
| 0x3F 7FF6 – 0x3F 7FF7 | Boot-to-Flash Entry Point (program branch instruction here) |
| 0x3F 7FF8 – 0x3F 7FFF | Security Password (128-Bit) (Do not program to all zeros) |

NOTE

Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data and should not contain program code.

Peripheral Frame 1 and Peripheral Frame 2 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations will appear in reverse order on the memory bus of the CPU. This action can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable, and by default, this mode protects the selected zones.

The wait-states for the various spaces in the memory map area are listed in [Table 6-9](#).

Table 6-9. Wait-States

| AREA | WAIT-STATES (CPU) | COMMENTS |
|--------------------|---|--|
| M0 and M1 SARAMs | 0-wait | Fixed |
| Peripheral Frame 0 | 0-wait | |
| Peripheral Frame 1 | 0-wait (writes) 2-wait (reads) | Cycles can be extended by peripheral-generated ready. Back-to-back write operations to Peripheral Frame 1 registers will incur a 1-cycle stall (1-cycle delay). |
| Peripheral Frame 2 | 0-wait (writes) 2-wait (reads) | Fixed. Cycles cannot be extended by the peripheral. |
| Peripheral Frame 3 | 0-wait (writes) 2-wait (reads) | Assumes no conflict between CPU and DMA cycles. The wait states can be extended by peripheral-generated ready. |
| L0–L8 SARAM | 0-wait data and program | Assumes no CPU conflicts |
| OTP | Programmable 1-wait minimum | Programmed via the Flash registers. 1-wait is minimum number of wait states allowed. |
| FLASH | Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged | Programmed via the Flash registers. |
| FLASH Password | 16-wait fixed | Wait states of password locations are fixed. |
| Boot-ROM | 0-wait | |

6.2.2 Register Map

The F28PLC8x device contains four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See [Table 6-10](#).

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See [Table 6-11](#).

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See [Table 6-12](#).

Peripheral Frame 3: McBSP registers are mapped to this. See [Table 6-13](#).

Table 6-10. Peripheral Frame 0 Registers⁽¹⁾

| NAME | ADDRESS RANGE | SIZE (x16) | EALLOW PROTECTED ⁽²⁾ |
|--|-----------------------|------------|---------------------------------|
| Device Emulation Registers | 0x00 0880 – 0x00 0984 | 261 | Yes |
| System Power Control Registers | 0x00 0985 – 0x00 0987 | 3 | Yes |
| FLASH Registers ⁽³⁾ | 0x00 0A80 – 0x00 0ADF | 96 | Yes |
| Code Security Module Registers | 0x00 0AE0 – 0x00 0AEF | 16 | Yes |
| ADC registers (0 wait read only) | 0x00 0B00 – 0x00 0B0F | 16 | No |
| CPU-TIMER0, CPU-TIMER1, CPU-TIMER2 Registers | 0x00 0C00 – 0x00 0C3F | 64 | No |
| PIE Registers | 0x00 0CE0 – 0x00 0CFF | 32 | No |
| PIE Vector Table | 0x00 0D00 – 0x00 0DFF | 256 | Yes |
| DMA Registers | 0x00 1000 – 0x00 11FF | 512 | Yes |

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.

(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.

(3) The Flash Registers are also protected by the Code Security Module.

Table 6-11. Peripheral Frame 1 Registers

| NAME | ADDRESS RANGE | SIZE (x16) | EALLOW PROTECTED |
|----------------|-----------------------|------------|------------------|
| GPIO registers | 0x00 6F80 – 0x00 6FFF | 128 | (1) |

(1) Some registers are EALLOW protected.

Table 6-12. Peripheral Frame 2 Registers

| NAME | ADDRESS RANGE | SIZE (x16) | EALLOW PROTECTED |
|----------------------------------|-----------------------|------------|------------------|
| System Control Registers | 0x00 7010 – 0x00 702F | 32 | Yes |
| SPI-A Registers | 0x00 7040 – 0x00 704F | 16 | No |
| SCI-A Registers | 0x00 7050 – 0x00 705F | 16 | No |
| NMI Watchdog Interrupt Registers | 0x00 7060 – 0x00 706F | 16 | Yes |
| External Interrupt Registers | 0x00 7070 – 0x00 707F | 16 | Yes |
| ADC Registers | 0x00 7100 – 0x00 717F | 128 | (1) |
| SPI-B Registers | 0x00 7740 – 0x00 774F | 16 | No |
| SCI-B Registers | 0x00 7750 – 0x00 775F | 16 | No |
| I2C-A Registers | 0x00 7900 – 0x00 793F | 64 | (1) |

(1) Some registers are EALLOW protected.

Table 6-13. Peripheral Frame 3 Registers

| NAME | ADDRESS RANGE | SIZE (x16) | EALLOW PROTECTED |
|--------------------------|-----------------------|------------|------------------|
| McBSP-A Registers | 0x00 5000 – 0x00 503F | 64 | No |
| Comparator 1 registers | 0x00 6400 – 0x00 641F | 32 | (1) |
| Comparator 2 registers | 0x00 6420 – 0x00 643F | 32 | (1) |
| Comparator 3 registers | 0x00 6440 – 0x00 645F | 32 | (1) |
| ePWM1 + HRPWM1 registers | 0x00 6800 – 0x00 683F | 64 | (1) |
| ePWM2 + HRPWM2 registers | 0x00 6840 – 0x00 687F | 64 | (1) |
| eCAP1 registers | 0x00 6A00 – 0x00 6A1F | 32 | No |

(1) Some registers are EALLOW protected.

6.3 Identification

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in [Table 6-14](#).

Table 6-14. Device Emulation Registers

| NAME | ADDRESS RANGE | SIZE (x16) | DESCRIPTION | EALLOW PROTECTED |
|-----------|-------------------|------------|--|------------------|
| DEVICECNF | 0x0880– 0x0881 | 2 | Device Configuration Register | Yes |
| PARTID | 0x3D 7E80 | 1 | Part ID Register TMS320F28PLC83PN TMS320F28PLC84PN | No |
| CLASSID | 0x0882 | 1 | Class ID Register TMS320F28PLC83 TMS320F28PLC84 | No |
| REVID | 0x0883 | 1 | Revision ID Register 0x0001 - Silicon Rev. A - TMS | No |

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x generation of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of F28PLCx-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
 - C/C++ Compiler
 - Code generation tools
 - Assembler/Linker
 - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ class, XDS560™ emulator, XDS100
- Flash programming tools
- Power supply
- Documentation and cables

7.1.1.1 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- *Getting Started With TMS320C28x Digital Signal Controllers* ([SPRAAM0](#)).
- [C2000 Getting Started Website \(http://www.ti.com/c2000getstarted\)](http://www.ti.com/c2000getstarted)
- TMS320F28x MCU Development and Experimenter's Kits (<http://www.ti.com/f28xkits>)

7.1.1.2 Reference Designs, Starter Kits, and Tools

Several PLC-related TI Designs reference designs are available for download on www.ti.com. Some of these reference designs are:

- System on Module for PRIME Power Line Communication (CENELEC Frequency Band) ([TIDM-SOMPLC-F28PLC83](#))
- Power Line Communications (PLC) System-on-Module for ARIB Frequency Band ([TIDM-SOMPLC-F28M35](#))
- PLC Motherboard with AC Mains Line Coupling ([TIDA-00192](#))
- Data Concentrator Reference Design ([TIDEP0006](#))

Several PLC evaluation kits are available for purchase on www.ti.com. Some of these evaluation kits are:

- Power Line Communications Kit for CENELEC Frequency Band ([TMDSPLCKITV4-CEN](#))
- Power Line Communications Kit for ARIB Frequency Band ([TMDSPLCKITV4-ARIB](#))
- Data Concentrator Evaluation Module ([TMDSDC3359](#))

7.1.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28PLC83**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, T). [Figure 7-1](#) provides a legend for reading the complete device name for any family member.

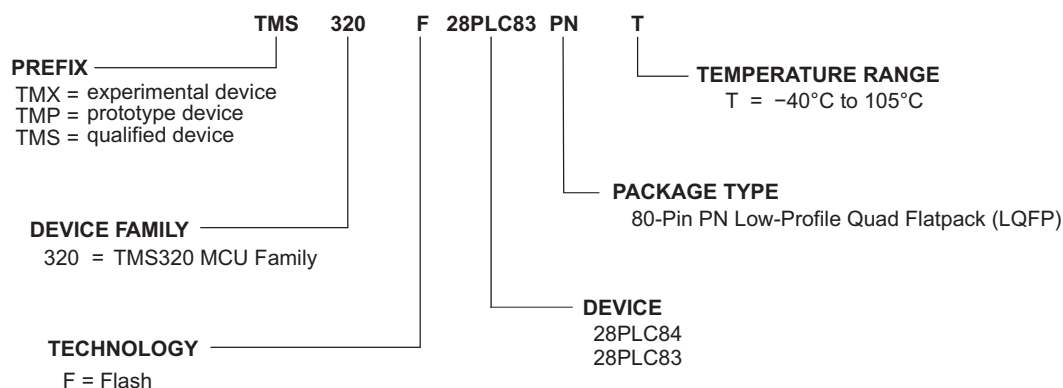


Figure 7-1. Device Nomenclature

7.2 Documentation Support

Extensive documentation supports all of the TMS320 MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* ([SPRU566](#)) for more information on types of peripherals.

The following documents can be downloaded from the TI website ([www.ti.com](#)):

Data Manual and Errata

[SPRS802](#) **TMS320F28PLC84, TMS320F28PLC83 Power Line Communications (PLC) Processors Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications for the F28PLC8x device.

[SPRZ379](#) **TMS320F28PLC84, TMS320F28PLC83 Power Line Communications (PLC) Processors Silicon Errata** describes known advisories on silicon and provides workarounds.

CPU User's Guides

[SPRU430](#) **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

Peripheral Guides and Technical Reference Manuals

[SPRU566](#) **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x digital signal processors (DSPs).

Tools Guides

[SPRU513](#) **TMS320C28x Assembly Language Tools v6.2.4 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[SPRU514](#) **TMS320C28x Optimizing C/C++ Compiler v6.2.4 User's Guide** describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

[SPRU608](#) **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

Application Reports

[SZZA021](#) **Semiconductor Packing Methodology** describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TMS320F28PLC84 | Click here | Click here | Click here | Click here | Click here |
| TMS320F28PLC83 | Click here | Click here | Click here | Click here | Click here |

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

TMS320C2000, C2000, DSP/BIOS, Code Composer Studio, XDS510, XDS560, TMS320, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TMS320F28PLC83PNT | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | F28PLC83PNT TMS320 | Samples |
| TMS320F28PLC83PNTR | ACTIVE | LQFP | PN | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | F28PLC83PNT TMS320 | Samples |
| TMS320F28PLC84PNT | ACTIVE | LQFP | PN | 80 | 119 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 105 | F28PLC84PNT TMS320 | Samples |
| TMS320F28PLC84PNTR | ACTIVE | LQFP | PN | 80 | 1000 | TBD | Call TI | Call TI | -40 to 105 | F28PLC84PNT TMS320 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

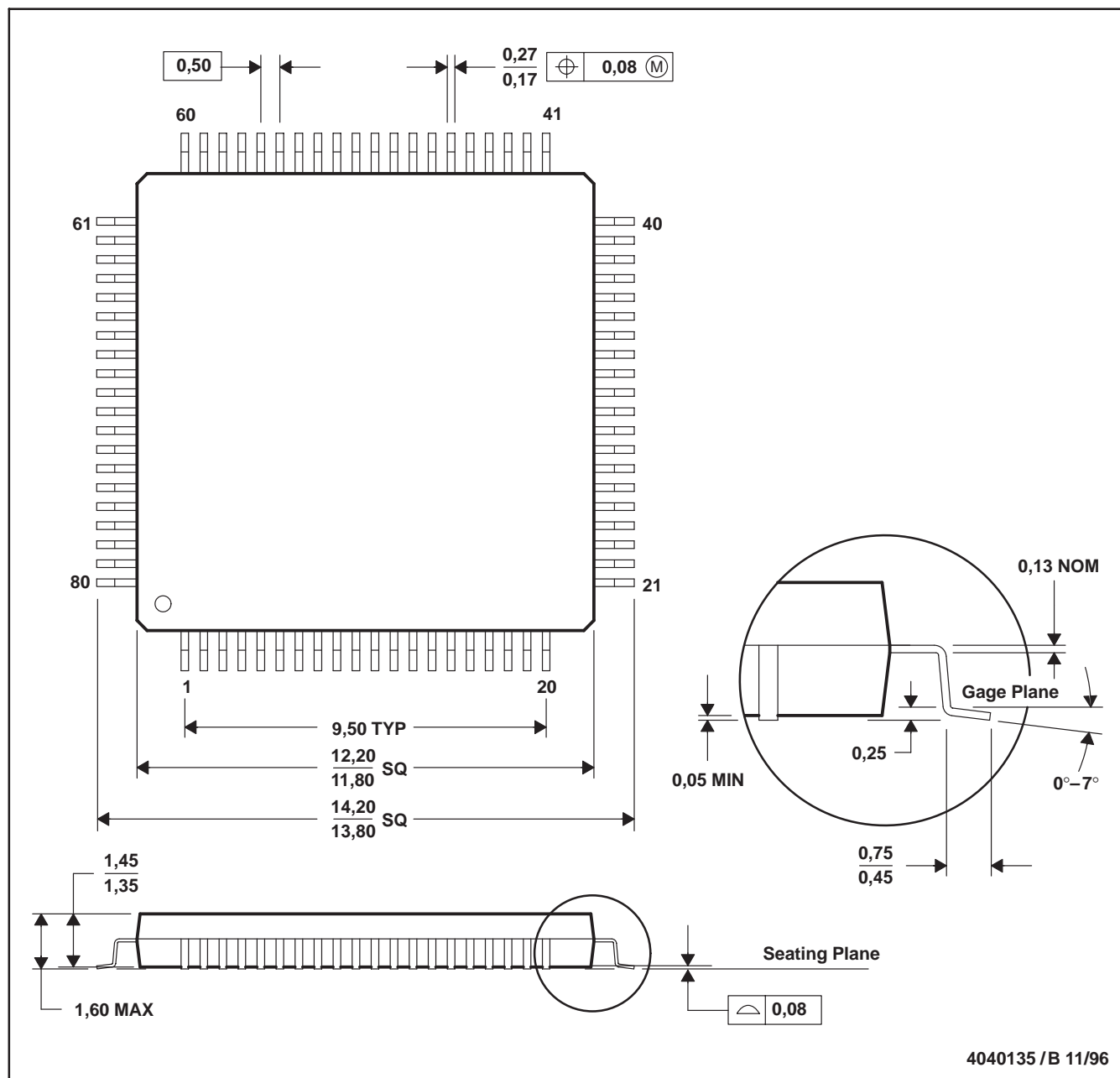
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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