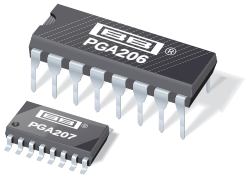
BURR - BROWN®



PGA206
PGA207

High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAINS:**
  PGA206: G=1, 2, 4, 8V/V
  PGA207: G=1, 2, 5, 10V/V
- **TRUE INSTRUMENTATION AMP INPUT**
- **FAST SETTLING: 3.5μs to 0.01%**
- **FET INPUT: I_B = 100pA max**
- **INPUT PROTECTION: ±40V**
- **LOW OFFSET VOLTAGE: 1.5mV max**
- **16-PIN DIP, SOL-16 SOIC PACKAGES**

APPLICATIONS

- **MULTIPLE-CHANNEL DATA ACQUISITION**
- **MEDICAL, PHYSIOLOGICAL AMPLIFIER**
- **PC-CONTROLLED ANALOG INPUT BOARDS**

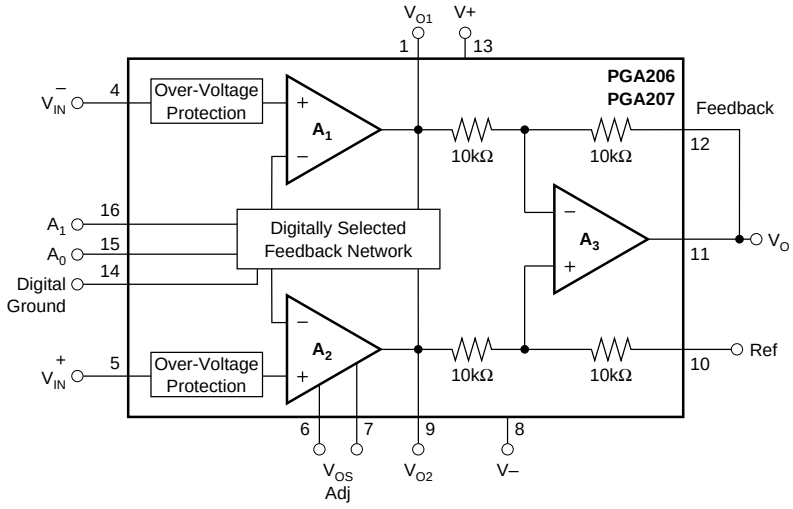
DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206 and PGA207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_B errors due to analog multiplexer series resistance.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to ±40V, even with the power supplies off. The PGA206 and PGA207 are laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for –40°C to +85°C operation.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1241B
Printed in U.S.A. May, 1995

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise noted.

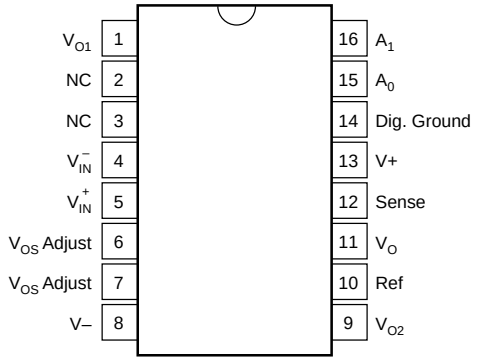
PARAMETER	CONDITIONS	PGA206P, U PGA207P, U MIN	PGA206P, U PGA207P, U TYP	PGA206P, U PGA207P, U MAX	PGA206PA, UA PGA207PA, UA MIN	PGA206PA, UA PGA207PA, UA TYP	PGA206PA, UA PGA207PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI	All Gains							
Initial	T_A = +25°C		±0.5	±1.5		±1	±2.5	mV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}, G = 8, 10		±2			*		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V		±5	±20		±10	±40	µV/V
Long-Term Stability			4.5			*		µV/mo
Impedance, Differential			10^{13} || 1			*		Ω || pF
Common-Mode			10^{12} || 4			*		Ω || pF
Common-Mode Voltage Range[1]	V_O = 0V	±(|V_S|–4)	±(|V_S| –2.5)		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±11V, ΔR_S = 1kΩ							
	G = 1	80	92		75	86		dB
	G = 2	85	96		80	90		dB
	G = 4 or 5	90	100		84	94		dB
	G = 8 or 10	95	100		84	94		dB
INPUT BIAS CURRENT	V_{IN} = 0		2	100		*	*	pA
vs Temperature			See Typical Curve			*		
Offset Current			1	100		*	*	pA
vs Temperature			See Typical Curve			*		
NOISE VOLTAGE, RTI	G = 8,10; R_S = 0Ω							
f = 10Hz			30			*		nV/√Hz
f = 100Hz			20			*		nV/√Hz
f = 1kHz			18			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Noise Current								
f = 1kHz			1.5			*		fA/√Hz
GAIN	All Gains, V_O = ±11V							
Gain Error			±0.01	±0.05		*	±0.1	%
Gain vs Temperature[2]			±1	±10		*	*	ppm/°C
Nonlinearity			±0.0003	±0.002		*	±0.005	% of FSR
OUTPUT								
Voltage, Positive		(V+) –4	(V+) –2.3		*	*		V
Negative		(V–) +4	(V–) +1.5		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			±17			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		5			*		MHz
	G = 2		4			*		MHz
	G = 4, 5		1.3			*		MHz
	G = 8, 10		600			*		kHz
Slew Rate	V_O = ±10V, G = 1 to 10		25			*		V/µs
Settling Time, 0.1%	20V Step, All Gains		2			*		µs
0.01%	20V Step, All Gains		3.5			*		µs
Output Overload Recovery	50% Overdrive		1.5			*		µs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V–		(V+) –4	*		*	V
Digital Low Voltage		V–		V_{DG} + 0.8V	*		*	V
Digital Input Current			1			*		pA
Digital High Voltage		V_{DG}+2		V+	*		*	V
Gain Switching Time			500			*		ns
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*	*	*	V
Current	V_{IN} = 0V		+12.4/–11.2	±13.5		*		mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
Thermal Resistance, θ_{JA}			80			*		°C/W

* Specification same as PGA206P or PGA207P.

NOTES: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test.

PIN CONFIGURATION

Top View **DIP SOL-16**



NC: No Internal Connection

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
PGA206PA	16-Pin Plastic DIP	180
PGA206P	16-Pin Plastic DIP	180
PGA206UA	SOL-16 Surface Mount	211
PGA206U	SOL-16 Surface Mount	211
PGA207PA	16-Pin Plastic DIP	180
PGA207P	16-Pin Plastic DIP	180
PGA207UA	SOL-16 Surface Mount	211
PGA207U	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ORDERING INFORMATION

PRODUCT	GAINS	PACKAGE	TEMPERATURE RANGE
PGA206PA	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206P	1, 2, 4, 8V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA206UA	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA206U	1, 2, 4, 8V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207PA	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207P	1, 2, 5, 10V/V	16-Pin Plastic DIP	–40°C to +85°C
PGA207UA	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C
PGA207U	1, 2, 5, 10V/V	SOL-16 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

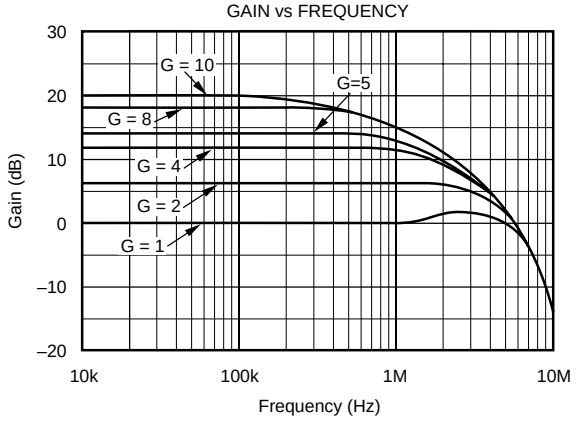
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

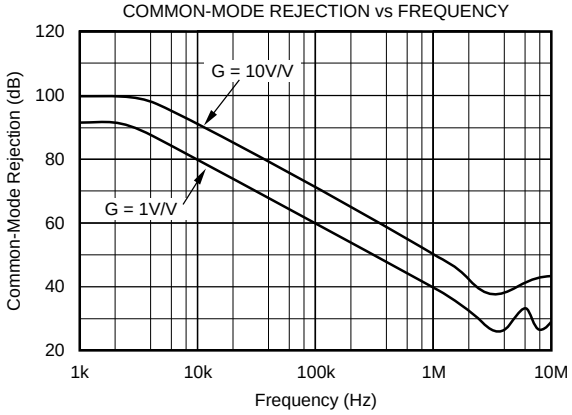
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

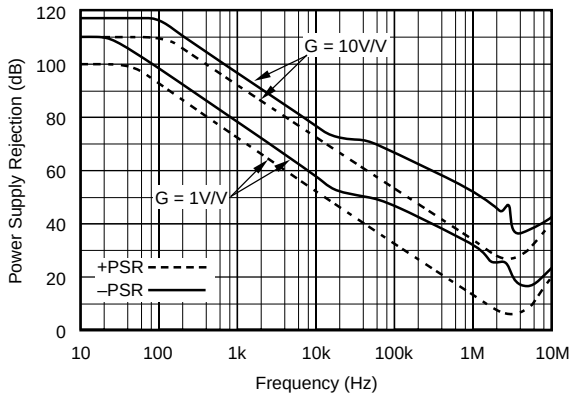
GAIN vs FREQUENCY



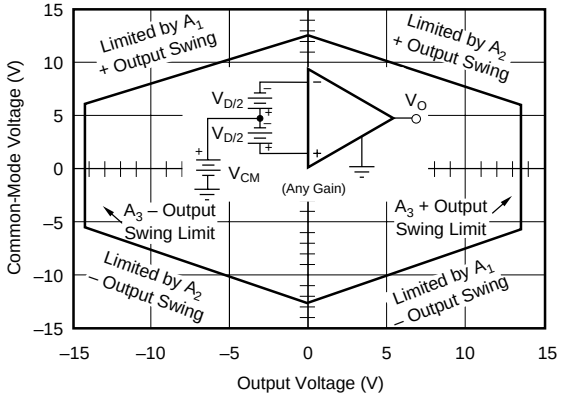
COMMON-MODE REJECTION vs FREQUENCY



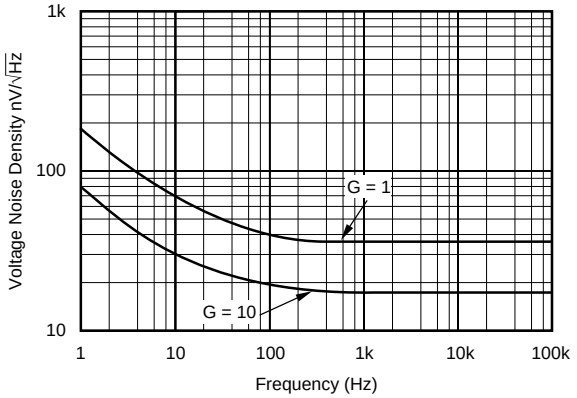
POWER SUPPLY REJECTION vs FREQUENCY



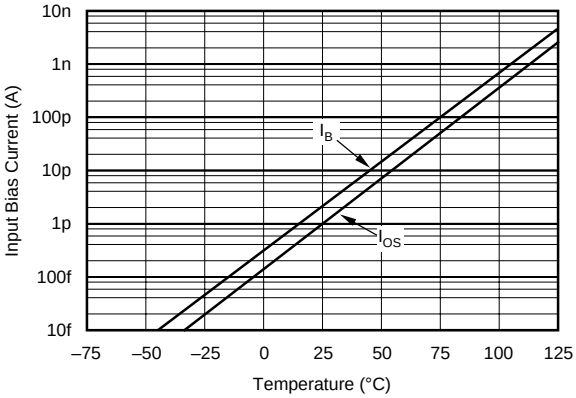
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



INPUT VOLTAGE NOISE vs FREQUENCY



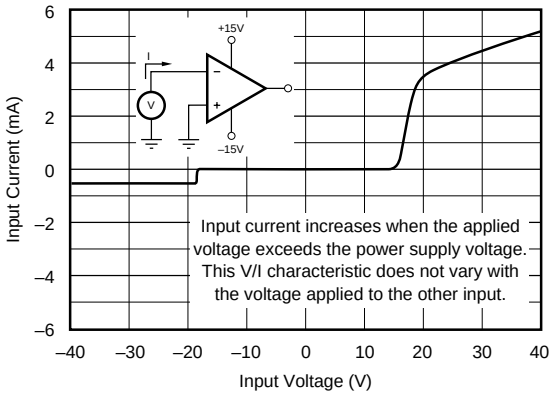
INPUT BIAS CURRENT vs TEMPERATURE



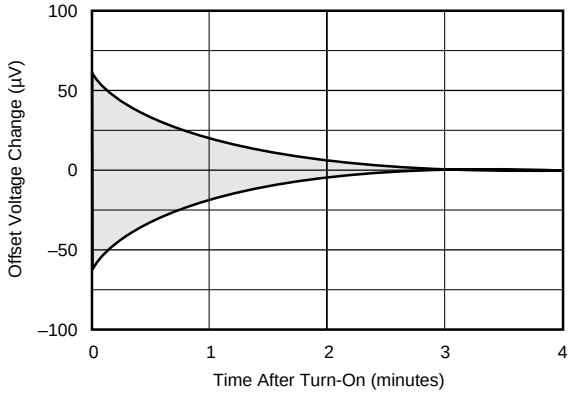
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

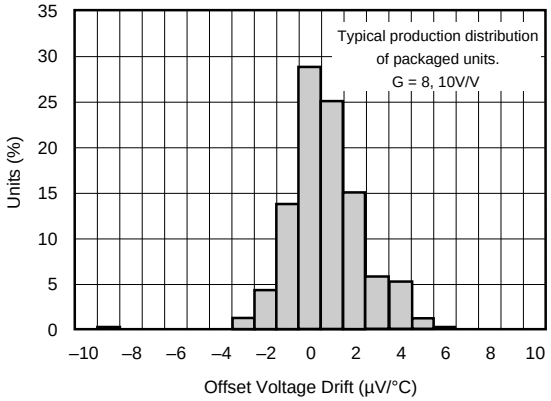
INPUT OVER-VOLTAGE V/I CHARACTERISTIC



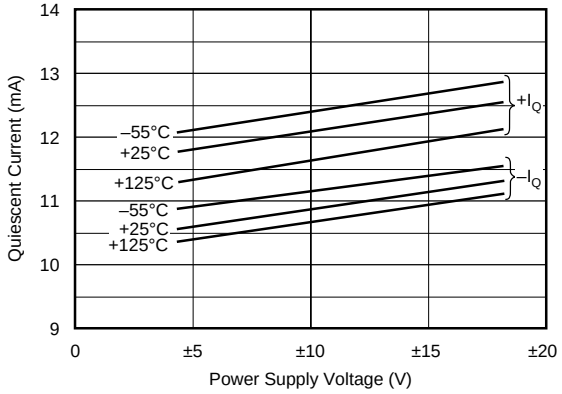
OFFSET VOLTAGE WARM-UP TIME



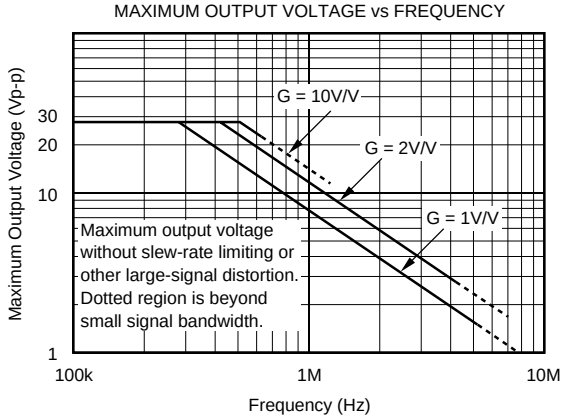
OFFSET VOLTAGE TEMPERATURE DRIFT PRODUCTION DISTRIBUTION



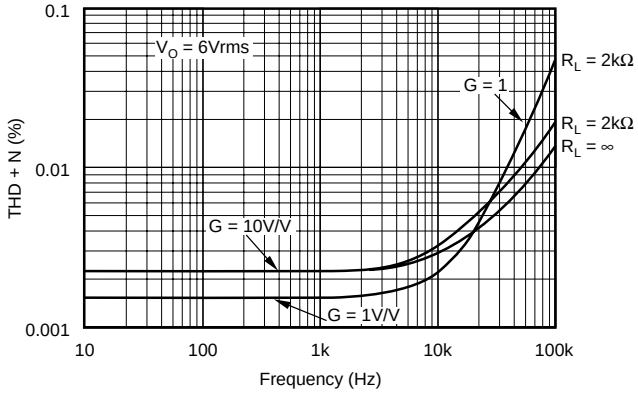
QUIESCENT CURRENT vs POWER SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



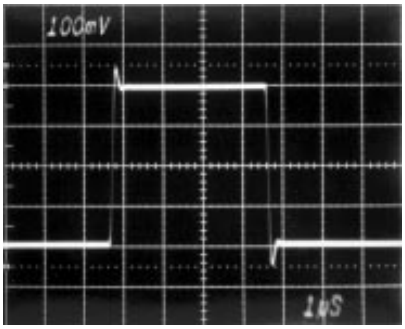
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

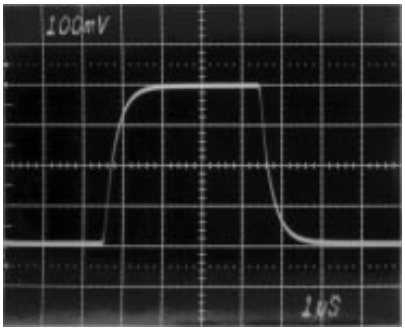
SMALL SIGNAL RESPONSE
G = 1, C_L = 50pF



100mV/div

1µs/div

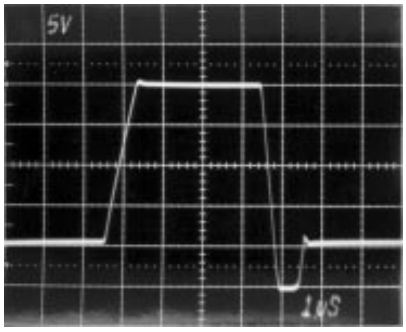
SMALL SIGNAL RESPONSE
G = 10, C_L = 50pF



100mV/div

1µs/div

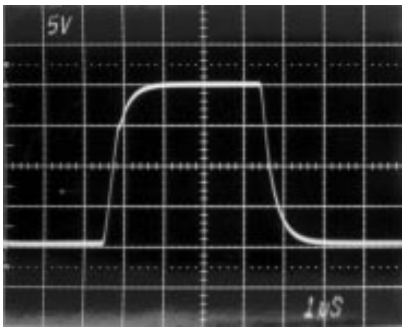
LARGE SIGNAL RESPONSE
G = 1, C_L = 50pF



5V/div

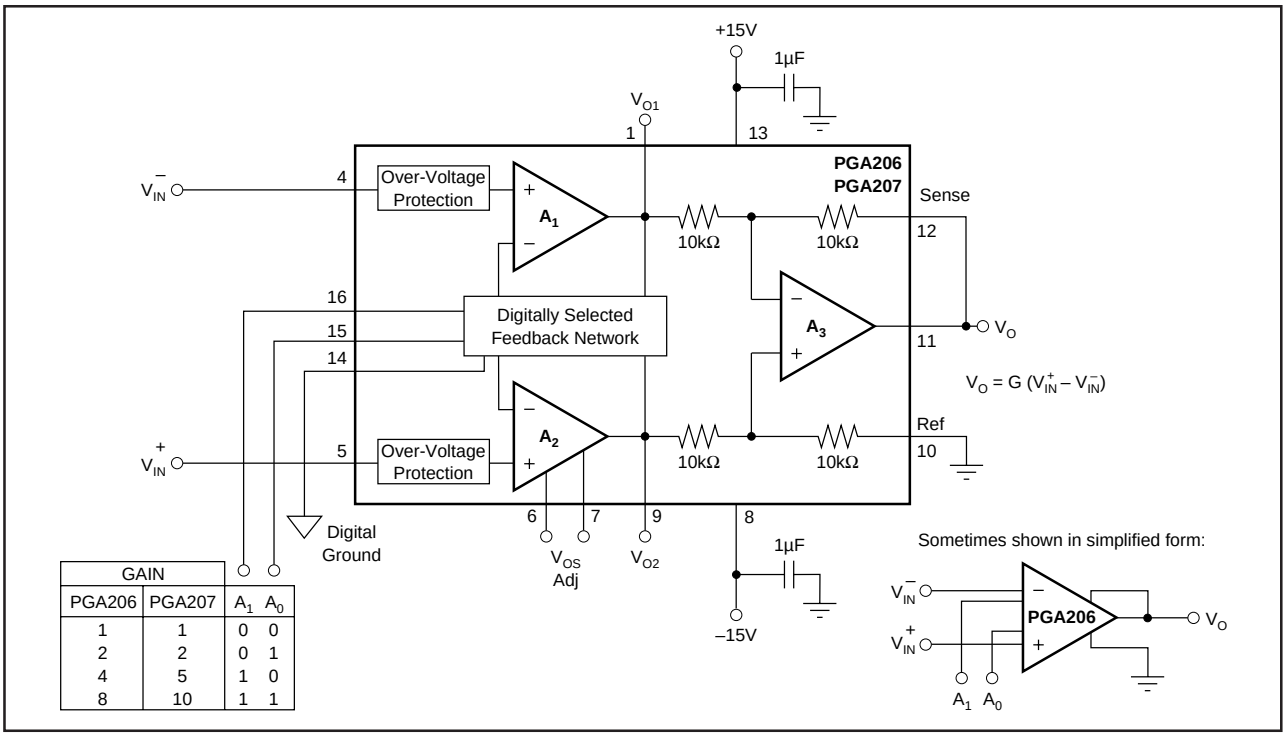
1µs/div

LARGE SIGNAL RESPONSE
G = 10, C_L = 50pF



5V/div

1µs/div



GAIN			
PGA206	PGA207	A_1	A_0
1	1	0	0
2	2	0	1
4	5	1	0
8	10	1	1

FIGURE 1. Basic Connections.

APPLICATIONS INFORMATION

Figure 1 shows the circuit diagram for basic operation of the PGA206 or PGA207. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

The output sense connection (pin 12) must be connected to the output terminal (pin 11) for proper operation. This connection can be made at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential ranging from the V– power supply to 4V less than V+. Digital ground is usually equal to analog ground potential and the two grounds are connected at the power supply. The digital inputs interface directly to CMOS and TTL logic.

A nearly constant current of approximately 1.2mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1, are not latched. A change in logic input immediately selects a new gain. Switching time of the logic is approximately 500ns. The time to respond to gain change is equal to switching time, plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to acquire gain control data from a high speed digital bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the digital latch as far as practical from analog circuitry to avoid coupling digital noise into analog input circuitry.

OFFSET VOLTAGE ADJUSTMENT

The PGA206 and PGA207 are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment. Multiplexed data acquisition systems generally correct offset by grounding the inputs of one channel to measure offset voltage. Stored offset values for each gain are then subtracted from subsequent readings of other channels.

Figure 2 shows optional offset voltage trim circuits. Offset voltage changes with the selected gain. To adjust for low offset voltage in all gains, both input and output offsets must be trimmed.

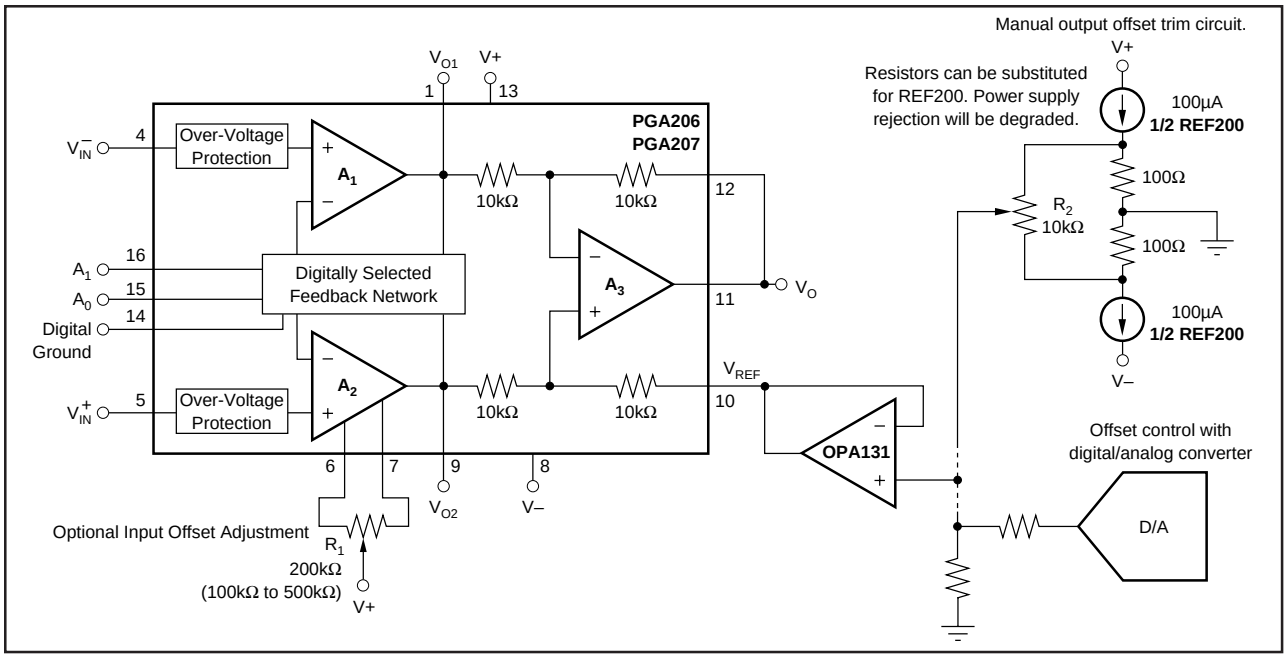


FIGURE 2. Optional Offset Voltage Trim Circuits.

R_1 adjusts the offset of the input amplifiers. Output stage offset is adjusted with R_2. A buffer op amp is required in the output offset adjustment circuit, as shown, to assure that the Ref pin is driven by a low source impedance. To adjust for low offset voltage in all gains, first adjust the input stage offset in the highest gain. Then adjust the output stage offset (R_2) in G = 1. Iterate the adjustments for lowest offset in all gains.

Offset can also be adjusted under processor control with a D/A converter as shown in Figure 2. The D/A's output voltage can be reduced with a resistor divider for better adjustment resolution, but an op amp buffer following the divider is required to provide a low source impedance to the ref terminal. A different offset value is required for each amplifier gain.

INPUT BIAS CURRENT RETURN PATH

The FET inputs of the PGA206 and PGA207 provide extremely high input impedance. Still, a path must be provided for the bias current of each input. Figure 3 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the linear input voltage range and the input amplifiers will saturate.

If the differential source resistance is low, a bias current return path can be connected to only one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 3). These applications do not require additional resistor(s) for proper operation.

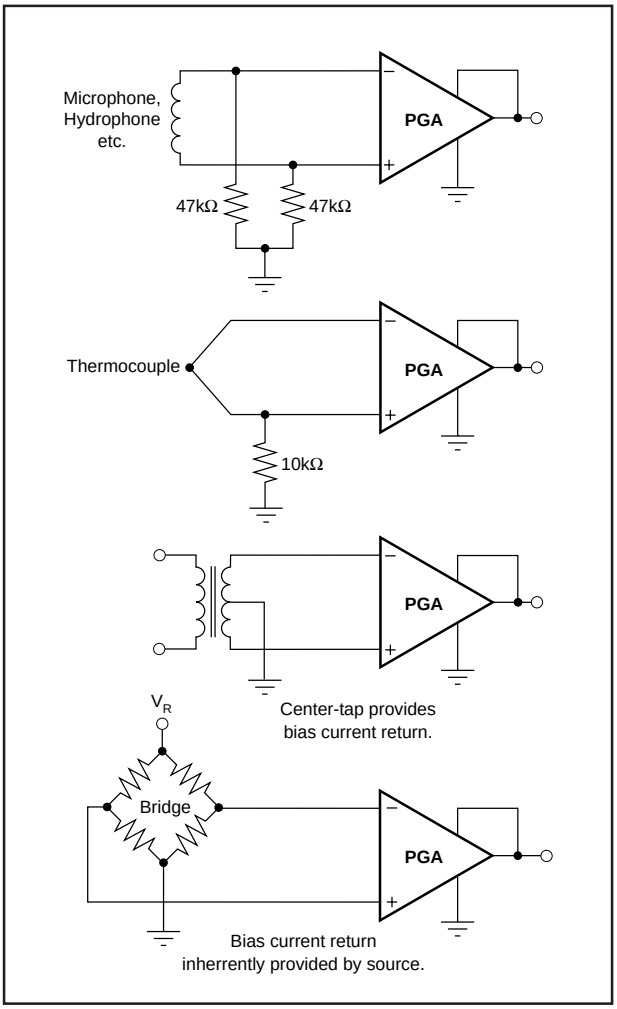


FIGURE 3. Providing an Input Bias Current Path.

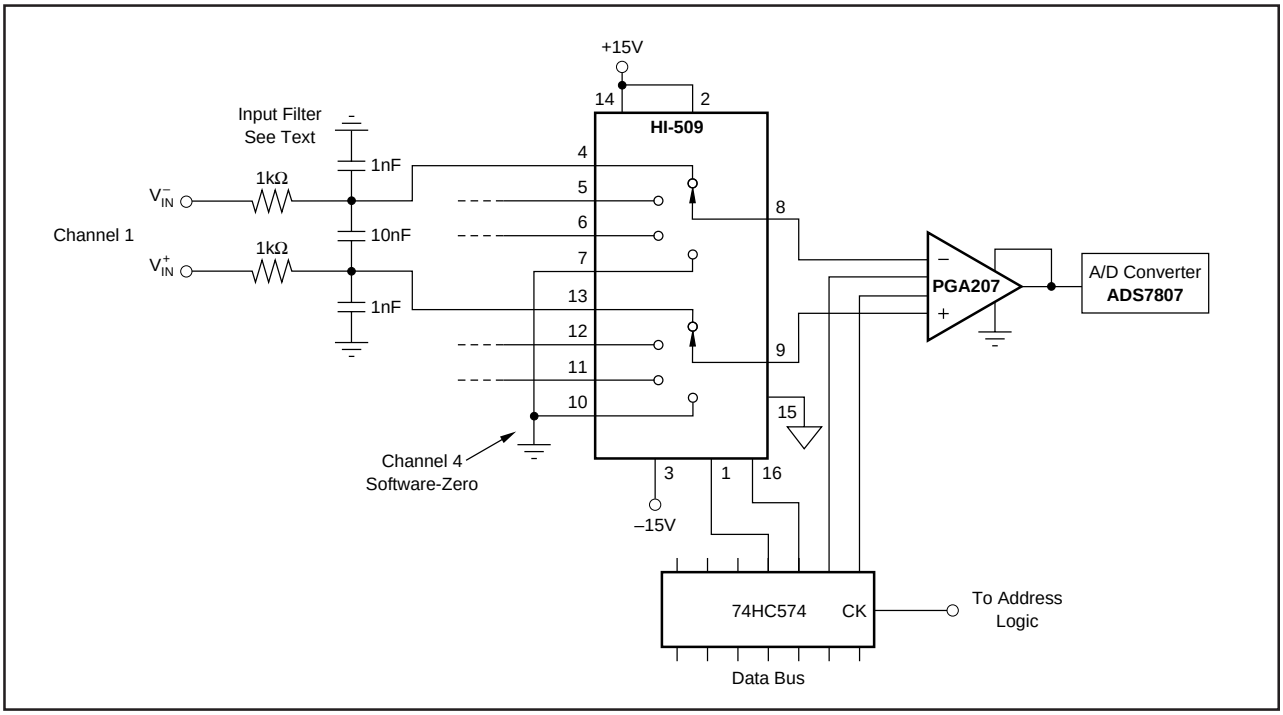


FIGURE 4. Multiplexed-Input Signal Acquisition System.

INPUT COMMON-MODE RANGE

The linear input voltage range of the PGA206 and PGA207 is from approximately 2.3V below the positive supply voltage to 1.5V above the negative supply. As a differential input voltage causes output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves "Input Common-Mode Range vs Output Voltage".

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA206 or PGA207 will be near 0V even though both inputs are overloaded. This condition can be detected by sensing the voltage on the V_{01} and V_{02} pins to determine whether they are within their linear operating range.

INPUT PROTECTION

The inputs of the PGA206 and PGA207 are individually protected for voltages up to ±40V. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value. The typical performance curve "Input Overload V/I Characteristic" shows this behavior. The inputs are protected even if no power supply voltage is applied.

MULTIPLEXED INPUTS

The PGA206 and PGA207 are ideally suited for multiple channel data acquisition. Figure 4 shows a typical application with an analog multiplexer used to connect one of four differential input signals to a single PGA207.

Careful circuit layout will help preserve accuracy of multiplexed signals. Run the inverting and non-inverting connections of each channel parallel to each other over a ground plane, or directly adjacent on top and bottom of the circuit board. Grounded guard traces between channels help reduce stray signal pick-up.

Multiplexed signals from high impedance sources require special care. As inputs are switched by the multiplexer, charge can be injected into the source, disturbing the input signal. Since many such sources involve slow signals, a simple R/C filter at the input can be used to dramatically reduce this effect. The arrangement shown filters both the differential signal and common-mode noise.

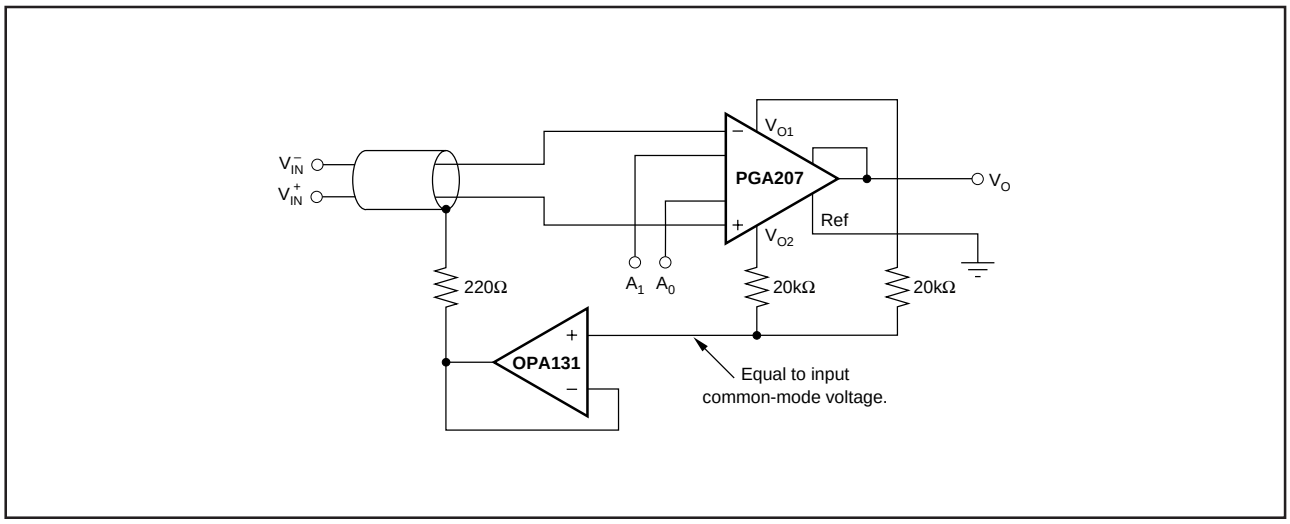
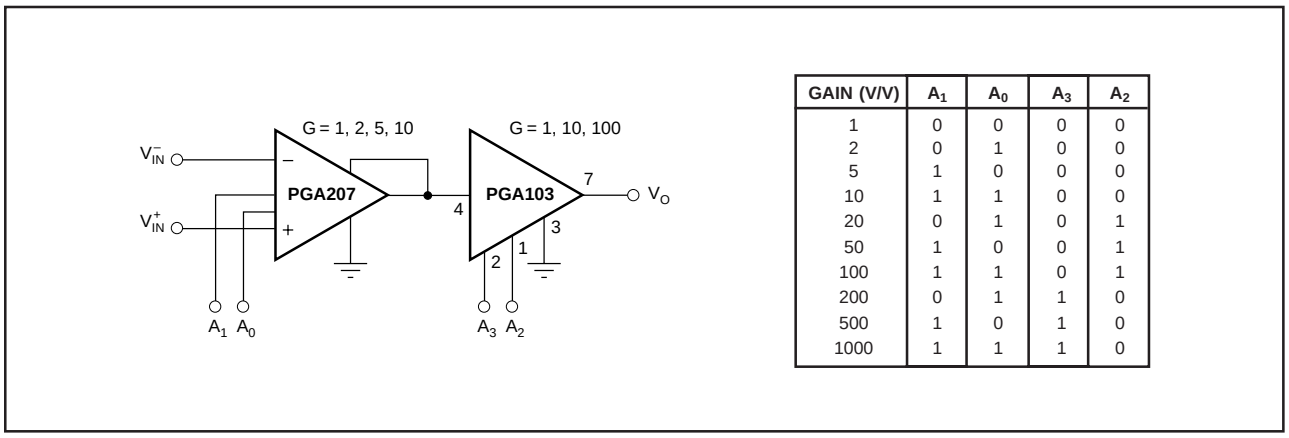


FIGURE 5. Shield Drive Circuit.



GAIN (V/V)	A_1	A_0	A_3	A_2
1	0	0	0	0
2	0	1	0	0
5	1	0	0	0
10	1	1	0	0
20	0	1	0	1
50	1	0	0	1
100	1	1	0	1
200	0	1	1	0
500	1	0	1	0
1000	1	1	1	0

FIGURE 6. Wide Gain Range Programmable IA.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA206PA	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA206PA	Samples
PGA206PAG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA206PA	Samples
PGA206UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		PGA206UA	Samples
PGA206UAG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		PGA206UA	Samples
PGA207PA	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI			
PGA207UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		PGA207UA	Samples
PGA207UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		PGA207UA	Samples
PGA207UA/1KE4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI			Samples
PGA207UAE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		PGA207UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

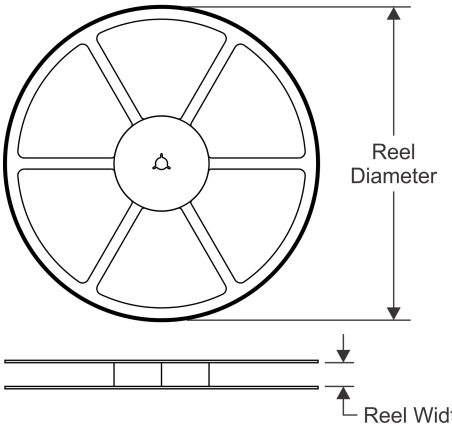
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

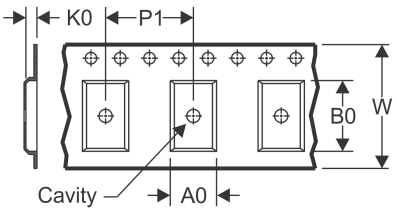
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

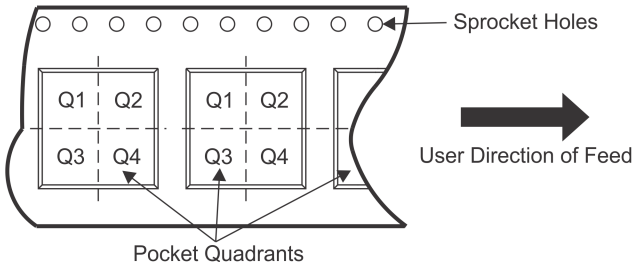


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

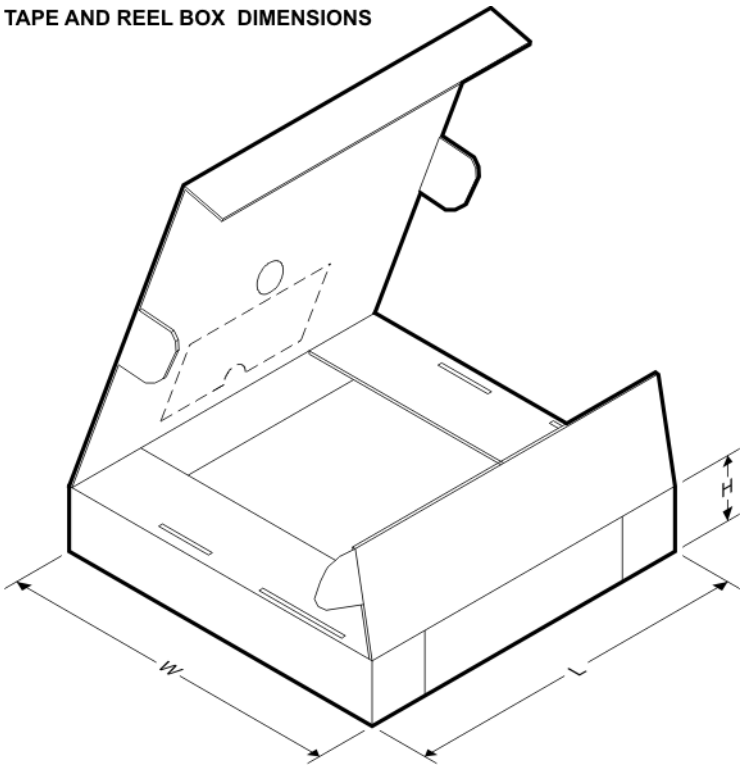
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA207UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA207UA/1K	SOIC	DW	16	1000	367.0	367.0	38.0

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