

PDP TRENCH IGBT

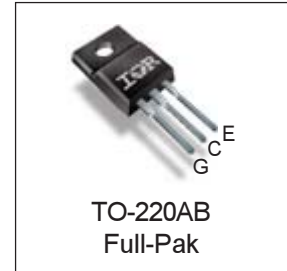
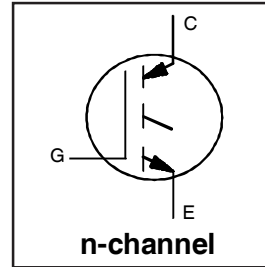
IRG71C28UPbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters

$V_{CE\ min}$	600	V
$V_{CE(on)}\ typ.\ @\ I_C = 40A$	1.70	V
$I_{RP}\ max\ @\ T_C = 25^\circ C\ ①$	225	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are 150 $^\circ C$ operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	± 30	V
$I_C\ @\ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE}\ @\ 15V$	25	A
$I_C\ @\ T_C = 100^\circ C$	Continuous Collector, $V_{GE}\ @\ 15V$	12	
$I_{RP}\ @\ T_C = 25^\circ C$	Repetitive Peak Current ①	225	
$P_D\ @\ T_C = 25^\circ C$	Power Dissipation	40	W
$P_D\ @\ T_C = 100^\circ C$	Power Dissipation	16	
	Linear Derating Factor	0.32	W/ $^\circ C$
T_J	Operating Junction and	-40 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	3.1	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient ②	—	65	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_{CE} = 1.0mA$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage③	15	—	—	V	$V_{GE} = 0V, I_{CE} = 1.0A$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.57	—	V/°C	Reference to 25°C, $I_{CE} = 1.0mA$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.25	—	V	$V_{GE} = 15V, I_{CE} = 12A$ ③
		—	1.42	—		$V_{GE} = 15V, I_{CE} = 24A$ ③
		—	1.70	1.95		$V_{GE} = 15V, I_{CE} = 40A$ ③
		—	1.96	—		$V_{GE} = 15V, I_{CE} = 70A$ ③
		—	2.97	—		$V_{GE} = 15V, I_{CE} = 160A$ ③
		—	1.75	—		$V_{GE} = 15V, I_{CE} = 40A, T_J = 150^{\circ}C$ ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	$V_{CE} = V_{GE}, I_{CE} = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I_{CES}	Collector-to-Emitter Leakage Current	—	0.5	20	μA	$V_{CE} = 600V, V_{GE} = 0V$
		—	30	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 100^{\circ}C$
		—	90	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 125^{\circ}C$
		—	305	—		$V_{CE} = 600V, V_{GE} = 0V, T_J = 150^{\circ}C$
I_{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100		$V_{GE} = -30V$
g_{fe}	Forward Transconductance	—	55	—	S	$V_{CE} = 25V, I_{CE} = 40A$
Q_g	Total Gate Charge	—	70	—	nC	$V_{CE} = 400V, I_C = 40A, V_{GE} = 15V$ ③
Q_{gc}	Gate-to-Collector Charge	—	25	—		
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	$I_C = 40A, V_{CC} = 400V$ $R_G = 22\Omega, L=100\mu H$ $T_J = 25^{\circ}C$
t_r	Rise time	—	35	—		
$t_{d(off)}$	Turn-Off delay time	—	260	—		
t_f	Fall time	—	145	—		
$t_{d(on)}$	Turn-On delay time	—	25	—	ns	$I_C = 40A, V_{CC} = 400V$ $R_G = 22\Omega, L=100\mu H$ $T_J = 150^{\circ}C$
t_r	Rise time	—	40	—		
$t_{d(off)}$	Turn-Off delay time	—	280	—		
t_f	Fall time	—	320	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G= 5.1\Omega$
E_{PULSE}	Energy per Pulse	—	770	—	μJ	$L = 220nH, C= 0.40\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G= 5.1\Omega, T_J = 25^{\circ}C$
		—	930	—		$L = 220nH, C= 0.40\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G= 5.1\Omega, T_J = 100^{\circ}C$
ESD	Human Body Model	Class H1C (2000V) (Per JEDEC standard JESD22-A114)				
	Machine Model	Class M4 (425V) (Per EIA/JEDEC standard EIA/JESD22-A115)				
C_{ies}	Input Capacitance	—	1880	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	75	—		$V_{CE} = 30V$
C_{res}	Reverse Transfer Capacitance	—	45	—		$f = 1.0MHz$
L_C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle ≤ 0.02 , $t_{on} = 1.0\mu\text{sec}$.
- ② R_θ is measured at T_J of approximately 90°C .
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

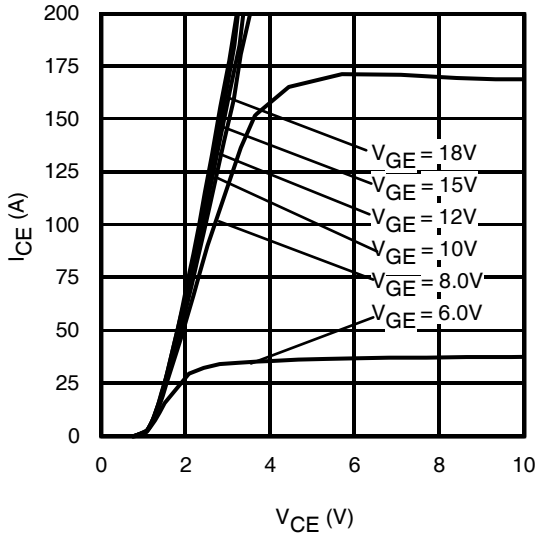


Fig 1. Typical Output Characteristics @ 25°C

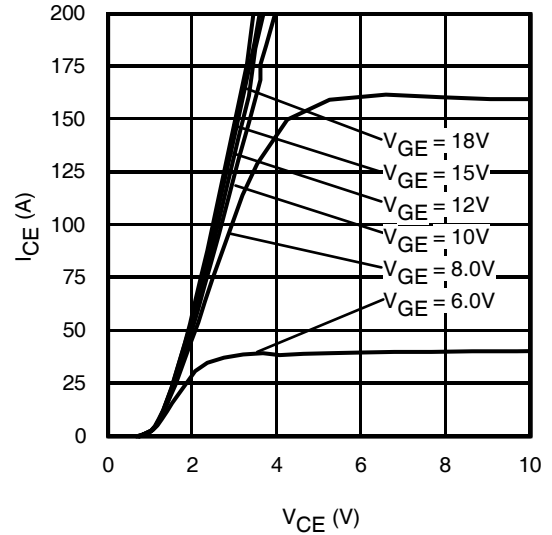


Fig 2. Typical Output Characteristics @ 75°C

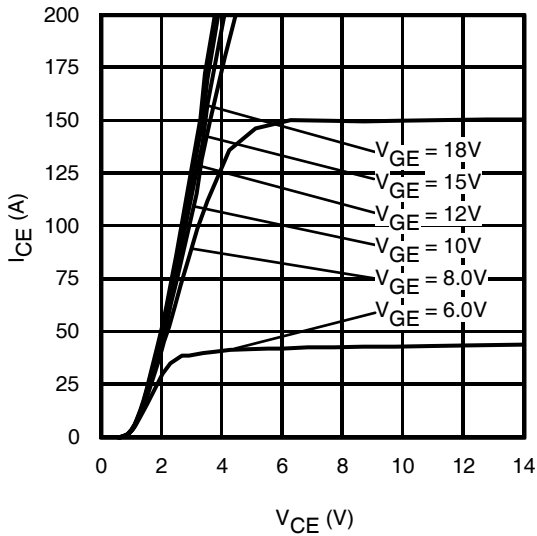


Fig 3. Typical Output Characteristics @ 125°C

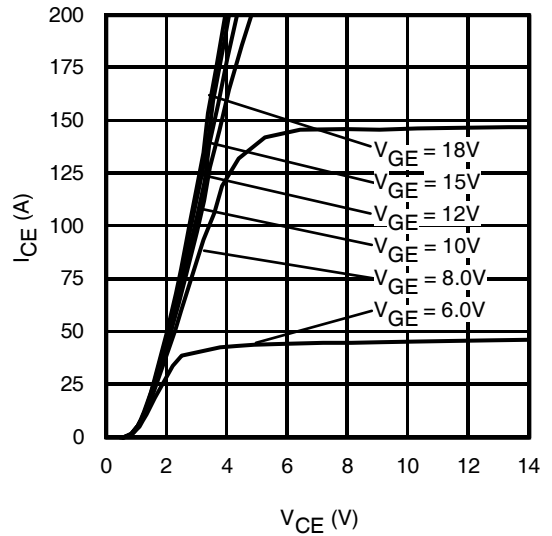


Fig 4. Typical Output Characteristics @ 150°C

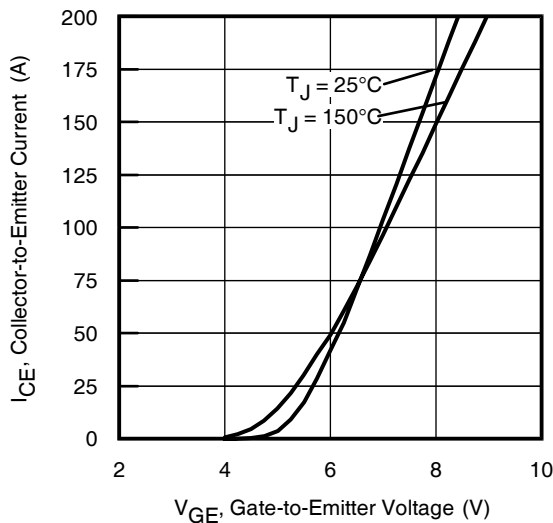


Fig 5. Typical Transfer Characteristics

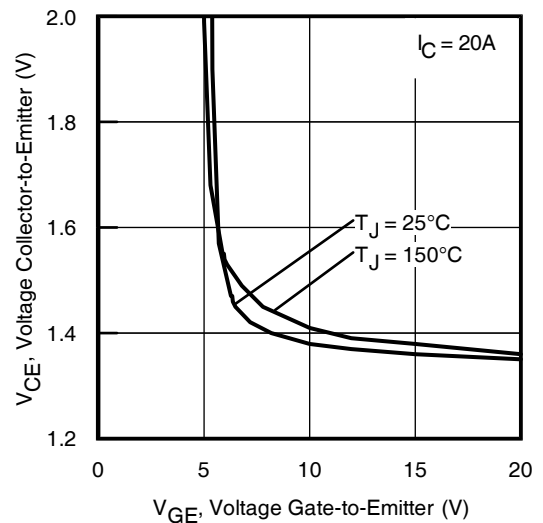


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

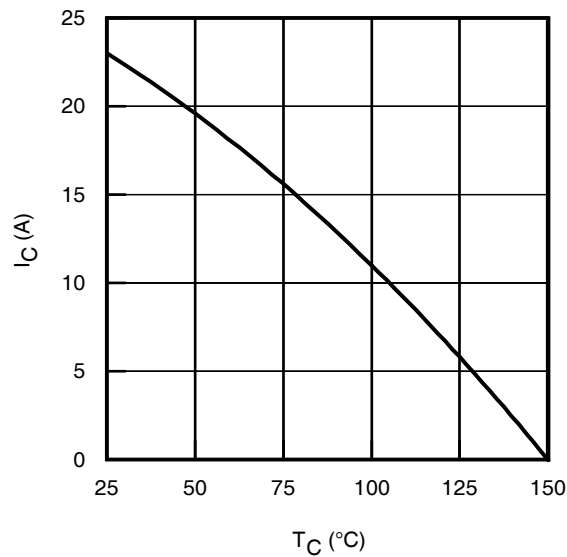


Fig 7. Maximum Collector Current vs. Case Temperature

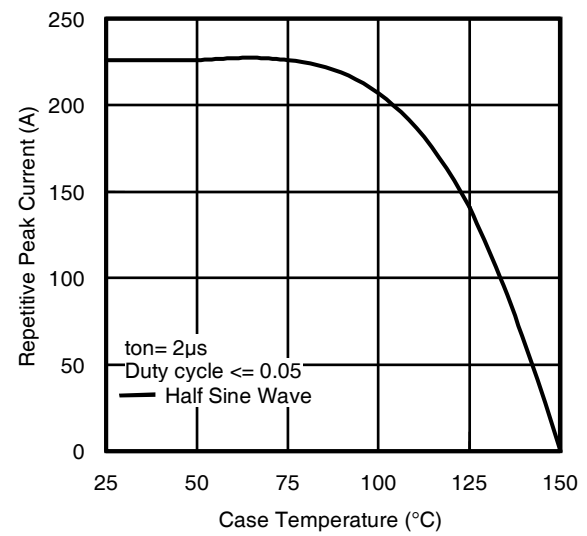


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

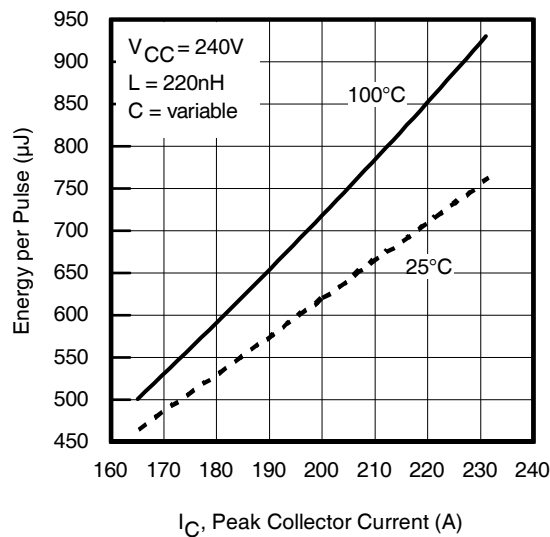


Fig 9. Typical E_{PULSE} vs. Collector Current

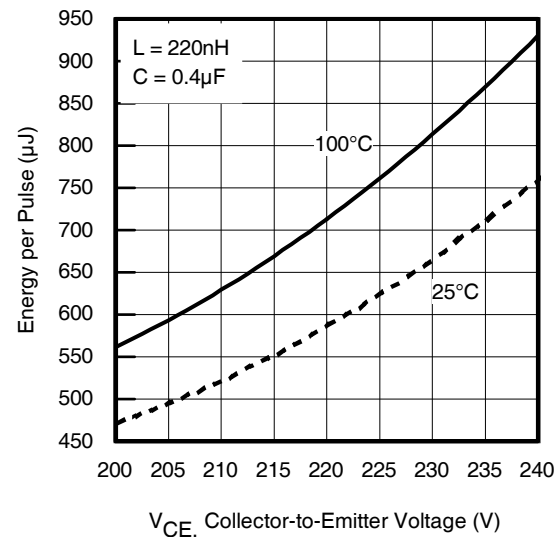


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

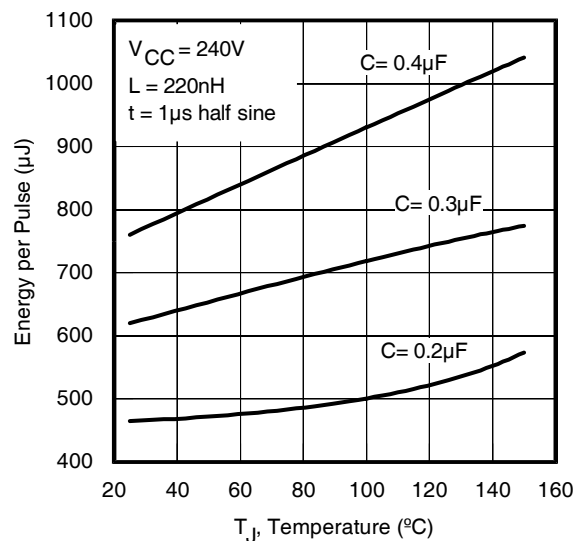


Fig 11. E_{PULSE} vs. Temperature

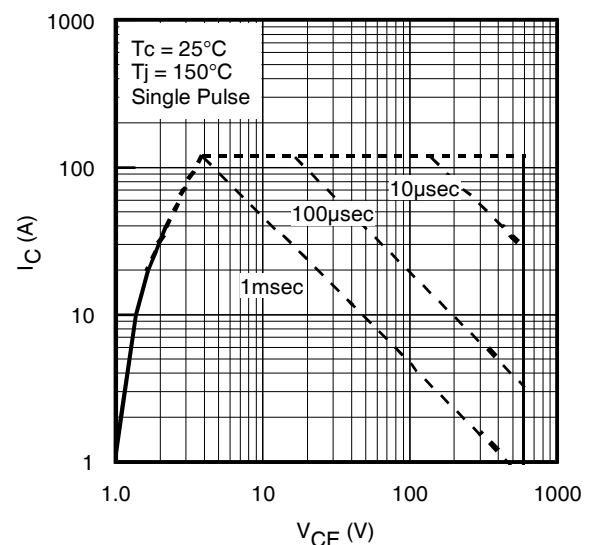


Fig 12. Forward Bias Safe Operating Area

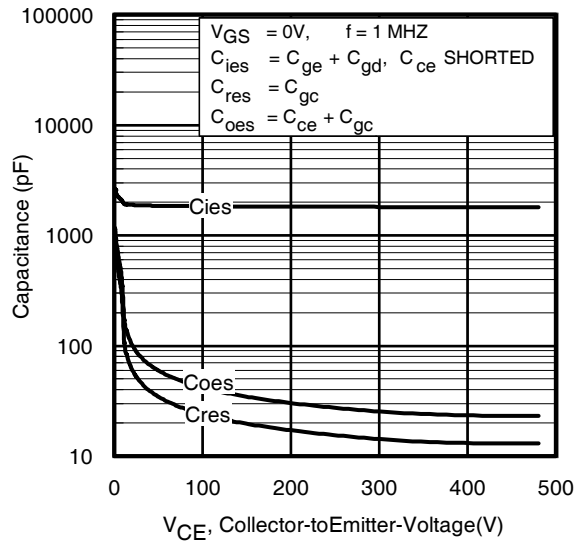


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

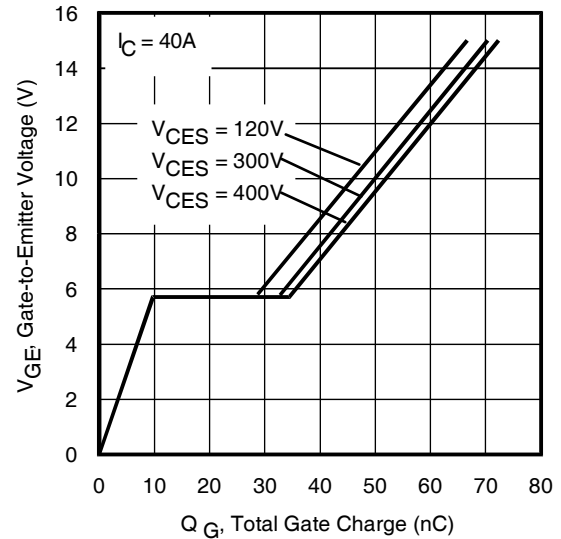


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

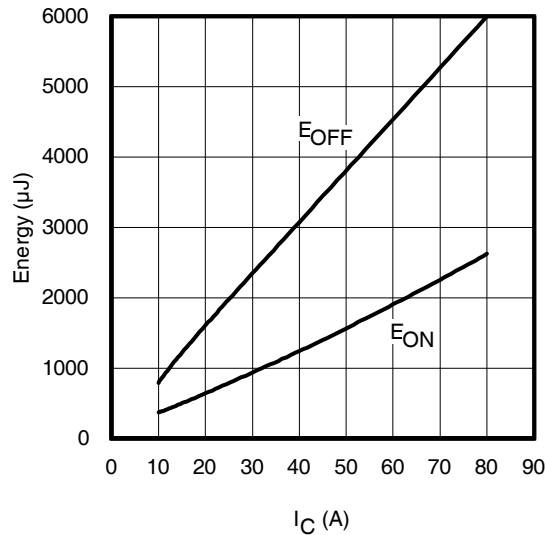


Fig 15 - Typ. Energy Loss vs. I_C

$T_J = 150^\circ C; L = 250\mu H; V_{CE} = 400V, R_G = 22\Omega; V_{GE} = 15V$

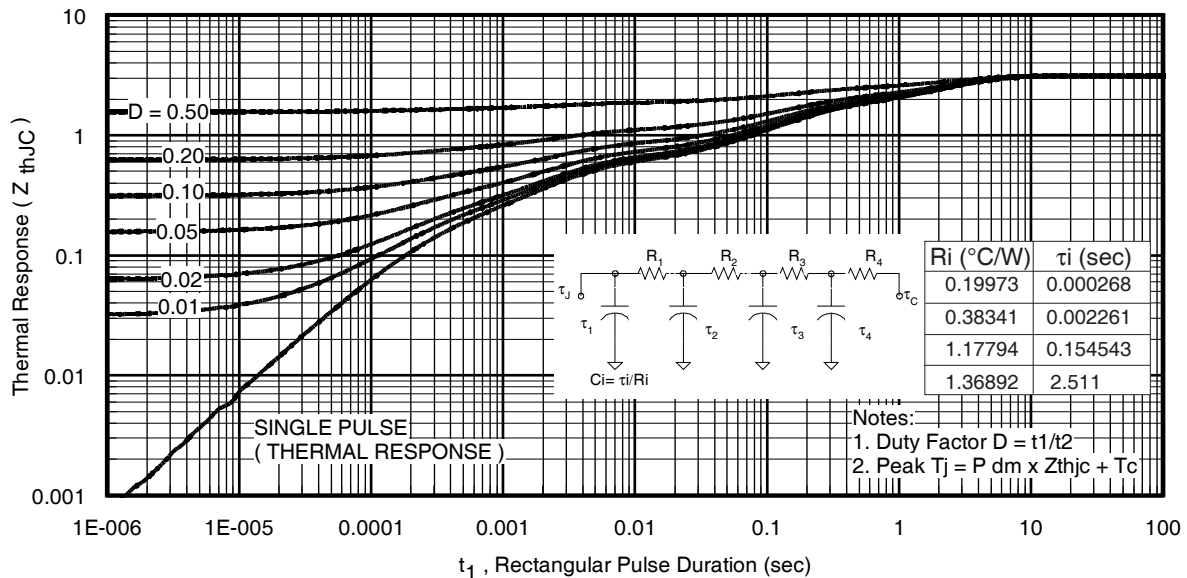


Fig 16. Maximum Effective Transient Thermal Impedance, Junction-to-Case

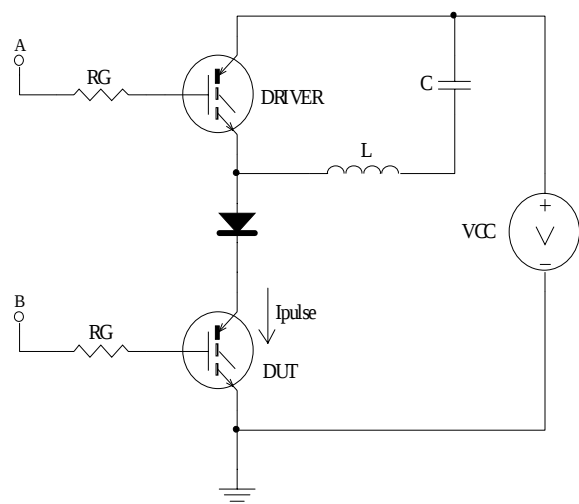


Fig 16a. t_{st} and E_{PULSE} Test Circuit

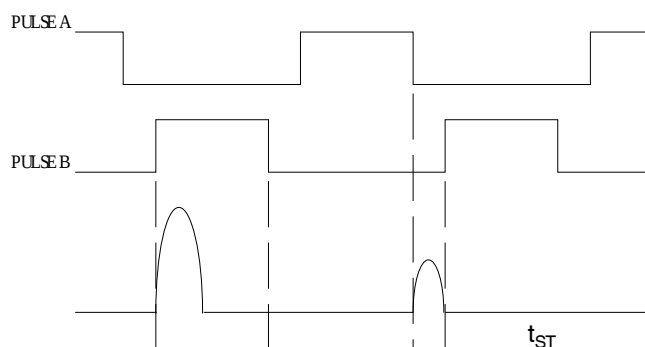


Fig 16b. t_{st} Test Waveforms

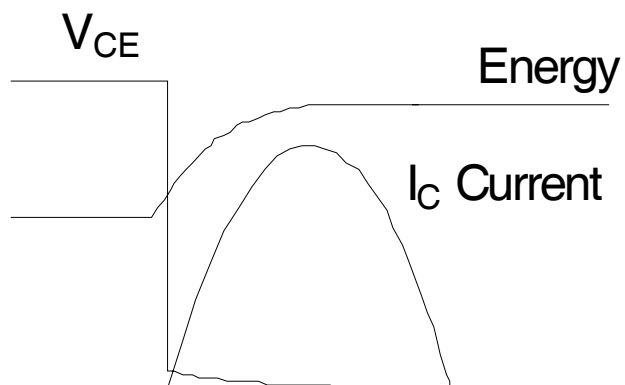


Fig 16c. E_{PULSE} Test Waveforms

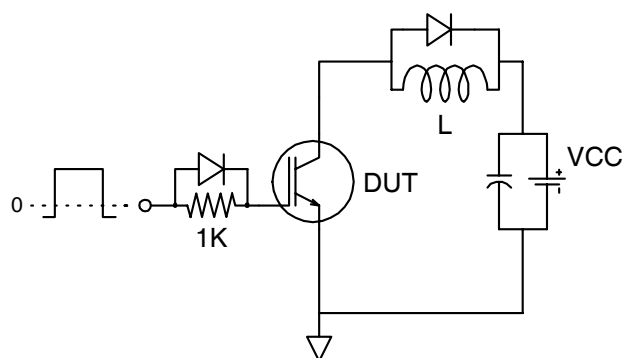
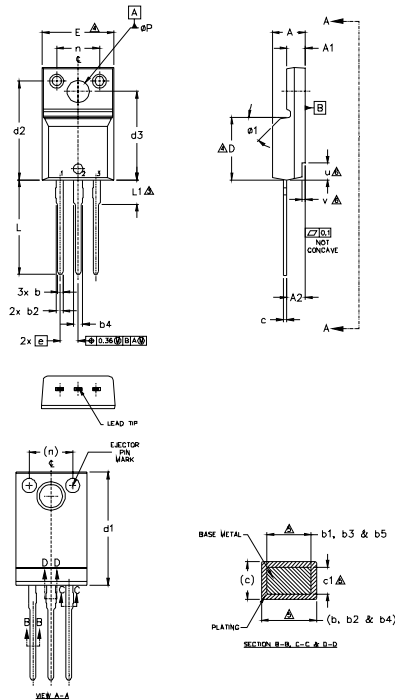


Fig. 17 - Gate Charge Circuit (turn-off)

TO-220AB Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	5
A1	2.57	2.83	.101	.111	
A2	2.51	2.93	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	5
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	5
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	5
c1	0.33	0.58	.013	.023	
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	4
d3	12.30	12.93	.484	.509	
E	9.63	10.75	.379	.423	4
e	2.54	BSC	.100	BSC	
L	13.20	13.72	.520	.540	3
L1	3.37	3.67	.122	.145	
n	6.05	6.60	.238	.260	6
øP	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	6
v	0.40	0.50	.016	.020	
ø1	—	45°	—	45°	

- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M-1994.
 - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
 - 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
 - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
 - 7.0 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

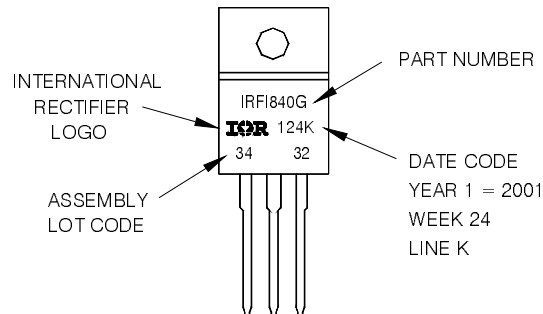
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- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

TO-220AB Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24, 2001
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB Full-Pak package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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