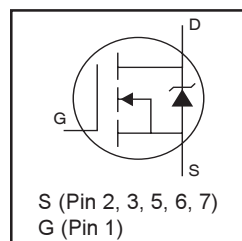


AUIRF1324S-7P

HEXFET® Power MOSFET

Features

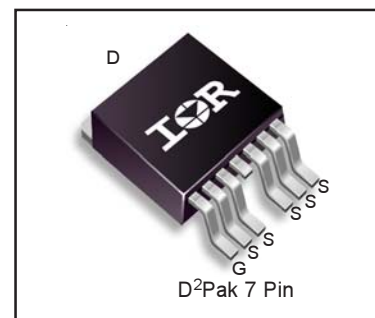
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *



$V_{(BR)DSS}$		24V
$R_{DS(on)}$	typ.	0.8mΩ
	max.	1.0mΩ
I_D (Silicon Limited)		429A ①
I_D (Package Limited)		240A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	429①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	303①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	240	
I_{DM}	Pulsed Drain Current ②	1640	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	230	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	1.6	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D²Pak ⑤	—	40	

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

Static Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	24	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.80	1.0	m Ω	$V_{GS} = 10V, I_D = 160A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	270	—	—	S	$V_{DS} = 50V, I_D = 160A$
R_G	Internal Gate Resistance	—	3.0	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 19V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	180	252	nC	$I_D = 75A$
Q_{gs}	Gate-to-Source Charge	—	47	—		$V_{DS} = 12V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	58	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	122	—		$I_D = 75A, V_{DS} = 0V, V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 16V$
t_r	Rise Time	—	240	—		$I_D = 160A$
$t_{d(off)}$	Turn-Off Delay Time	—	86	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	93	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	7700	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	3380	—		$V_{DS} = 19V$
C_{rss}	Reverse Transfer Capacitance	—	1930	—		$f = 1.0MHz$, See Fig.5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	4780	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 19V$ ⑦, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	4970	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 19V$ ⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	429①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1636		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 160A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	71	107	ns	$T_J = 25^\circ\text{C}$ $V_R = 20V$,
		—	74	110		$T_J = 125^\circ\text{C}$ $I_F = 160A$
Q_{rr}	Reverse Recovery Charge	—	83	120	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	92	140		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	2.0	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.(Refer to AN-1140 <http://www.irf.com/technical-info/appnotes/an-1140.pdf>)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.018mH$
 $R_G = 25\Omega$, $I_{AS} = 160A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 160A$, $di/dt \leq 600A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101) ^{††}	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D2 PAK 7 Pin	MSL1
ESD	Machine Model	Class M4 AEC-Q101-002	
	Human Body Model	Class H3A AEC-Q101-001	
	Charged Device Model	Class C5 AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions to AEC-Q101 requirements are noted in the qualification report.

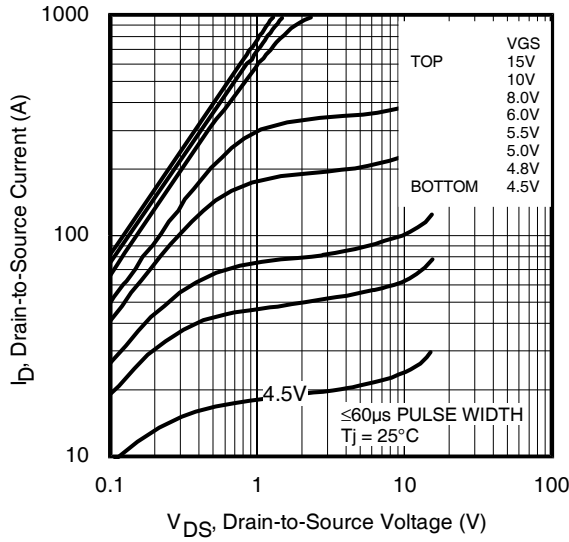


Fig 1. Typical Output Characteristics

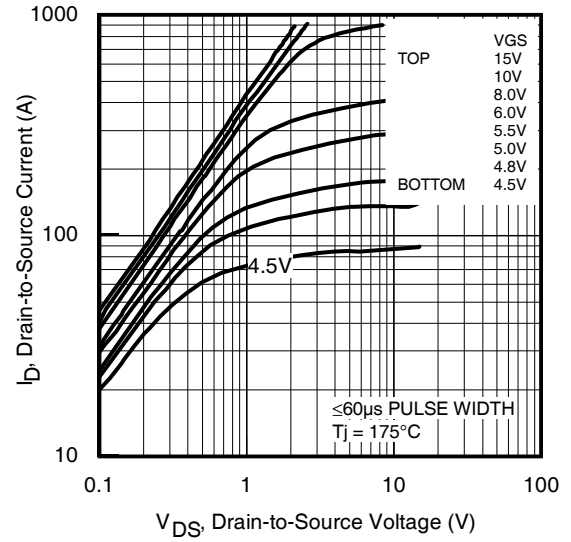


Fig 2. Typical Output Characteristics

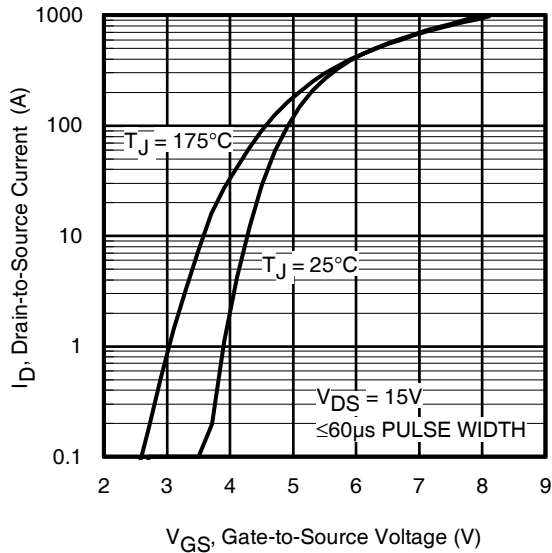


Fig 3. Typical Transfer Characteristics

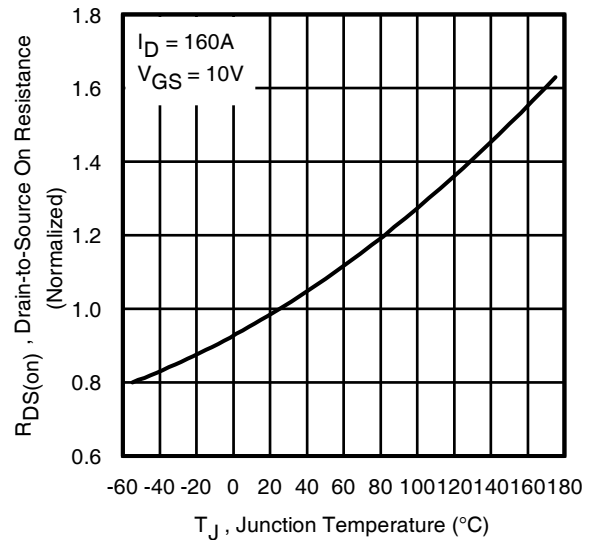


Fig 4. Normalized On-Resistance vs. Temperature

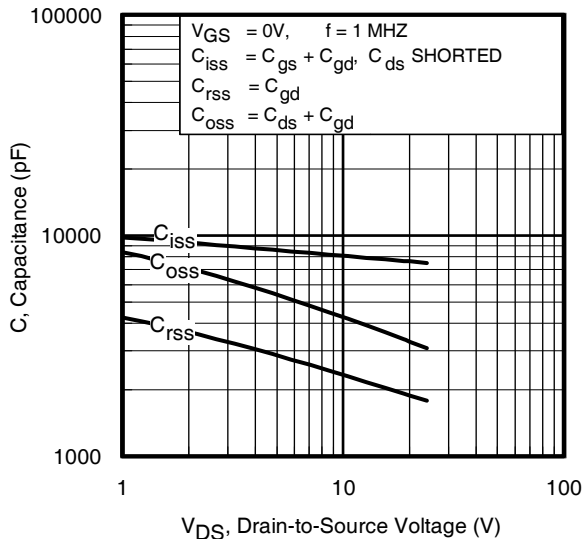


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

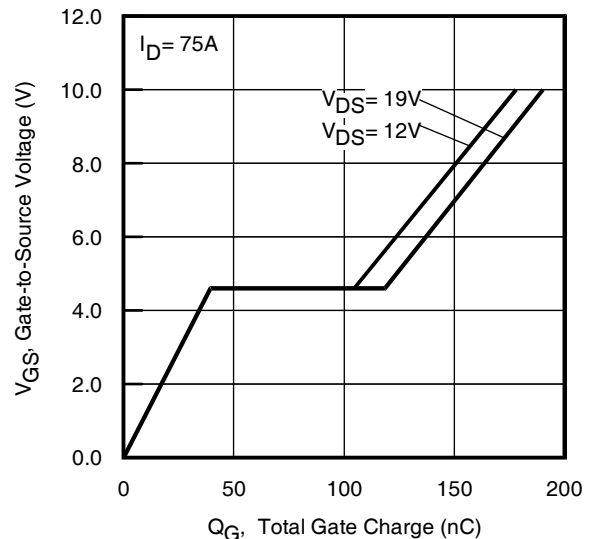


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

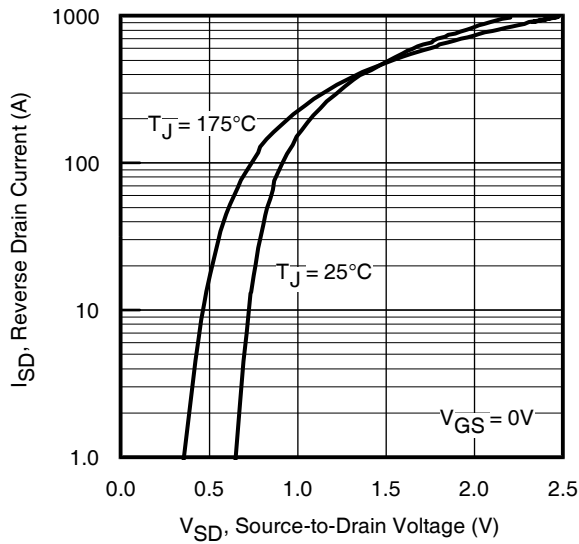


Fig 7. Typical Source-Drain Diode Forward Voltage

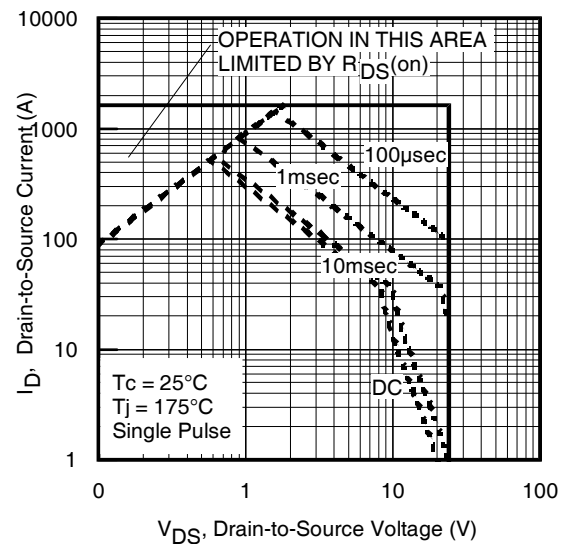


Fig 8. Maximum Safe Operating Area

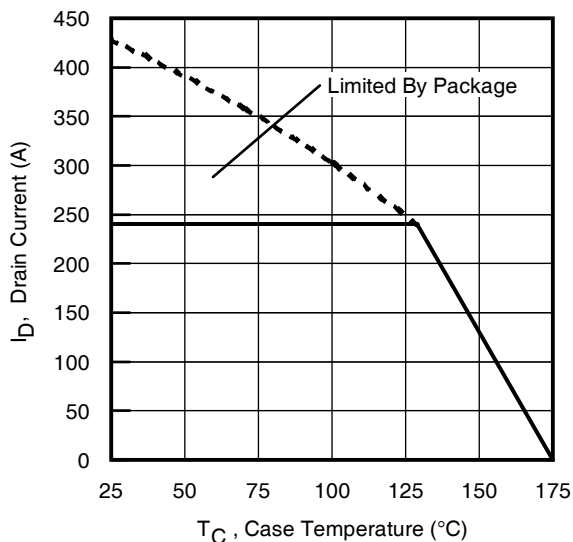


Fig 9. Maximum Drain Current vs. Case Temperature

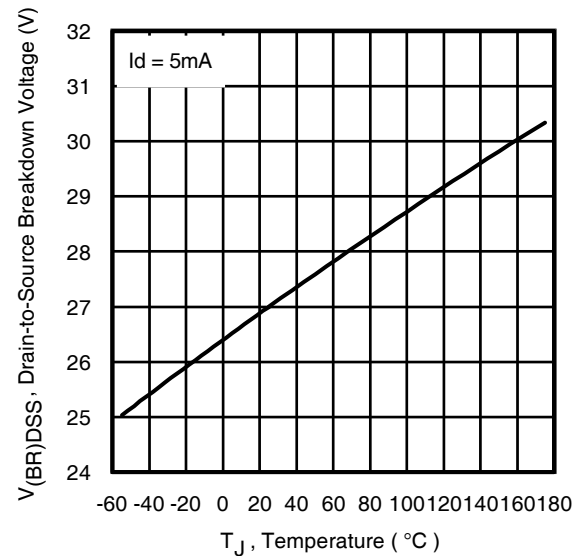


Fig 10. Drain-to-Source Breakdown Voltage

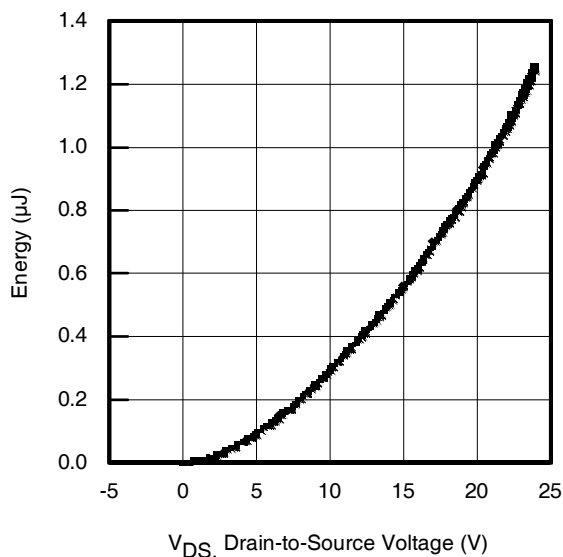


Fig 11. Typical C_{OSS} Stored Energy

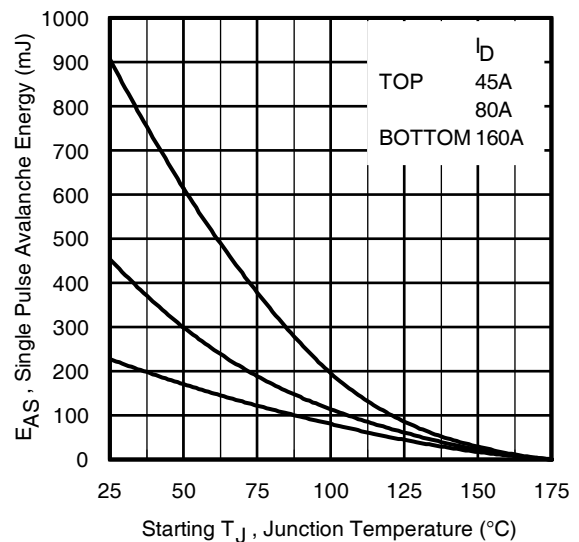


Fig 12. Maximum Avalanche Energy vs. Drain Current

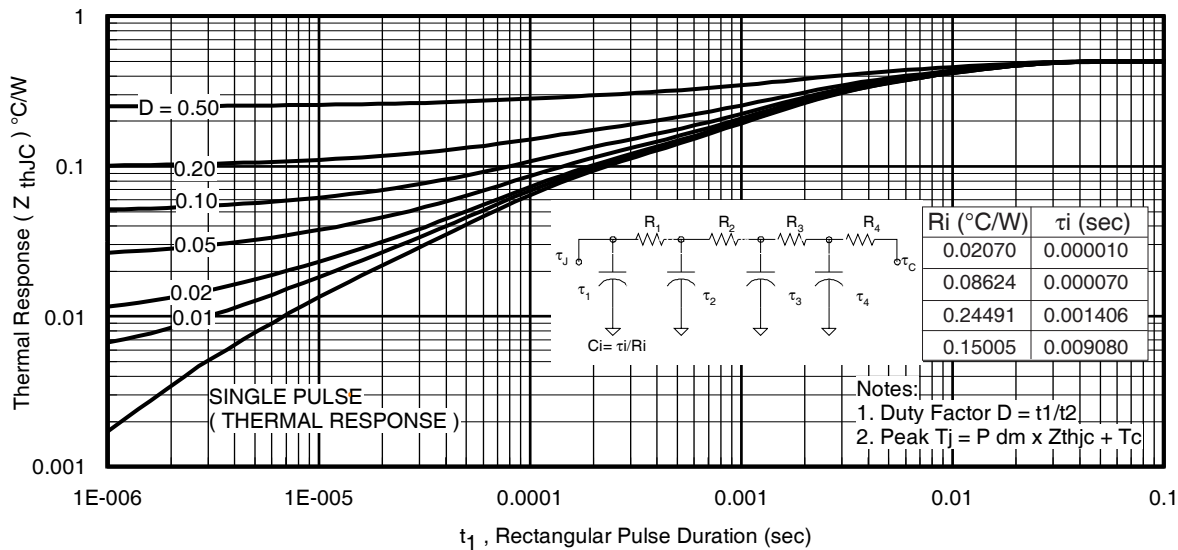


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

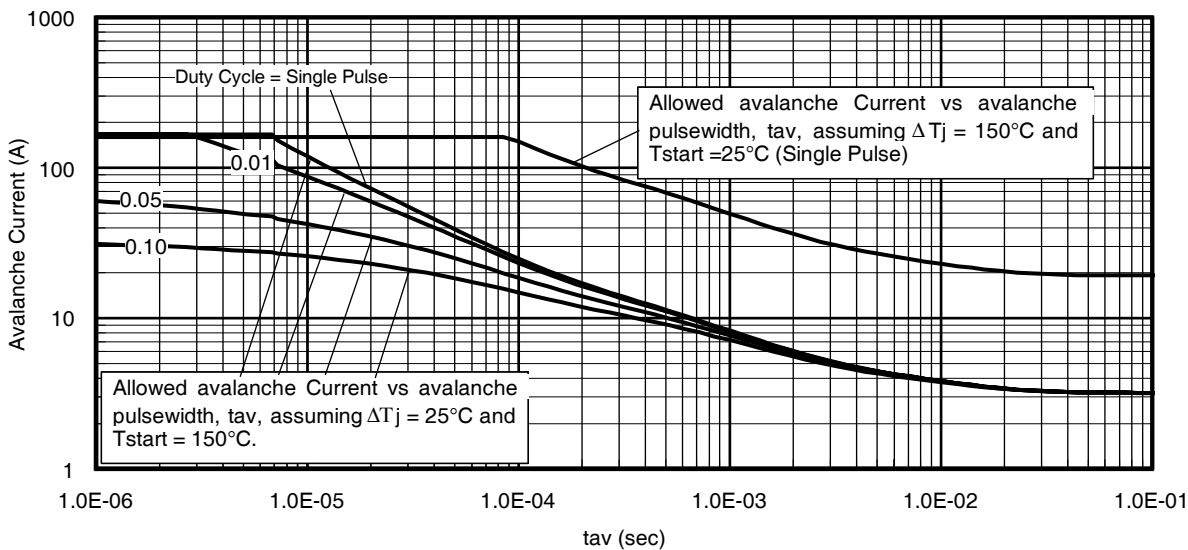


Fig 14. Typical Avalanche Current vs.Pulsewidth

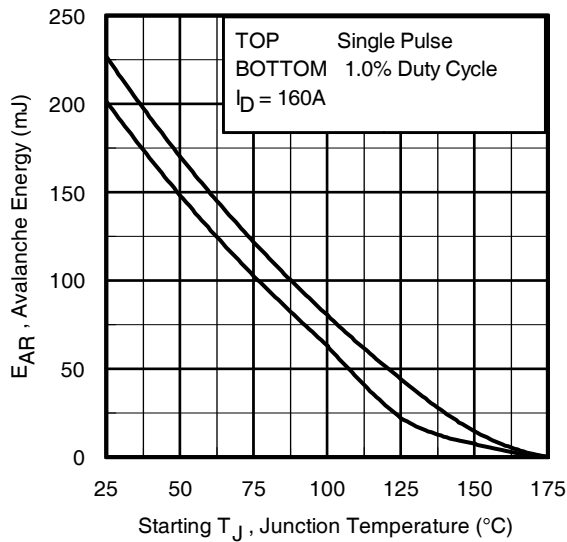


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figure 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

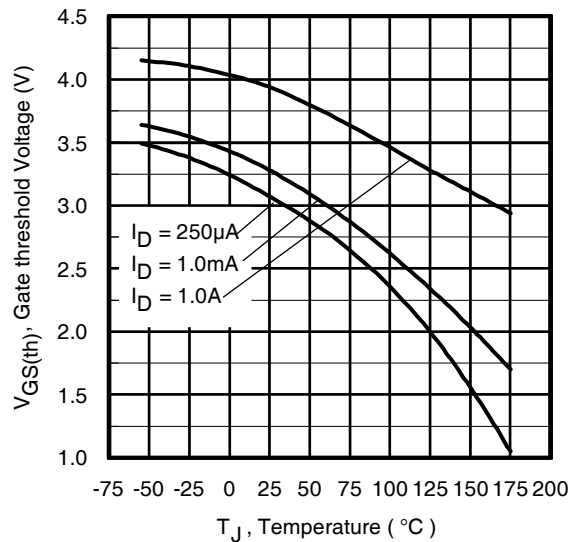


Fig 16. Threshold Voltage Vs. Temperature

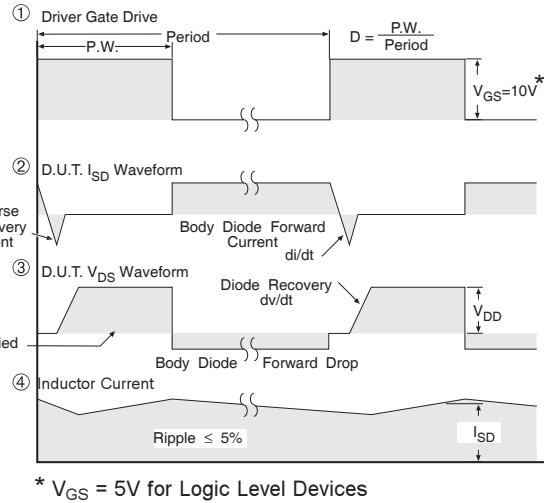
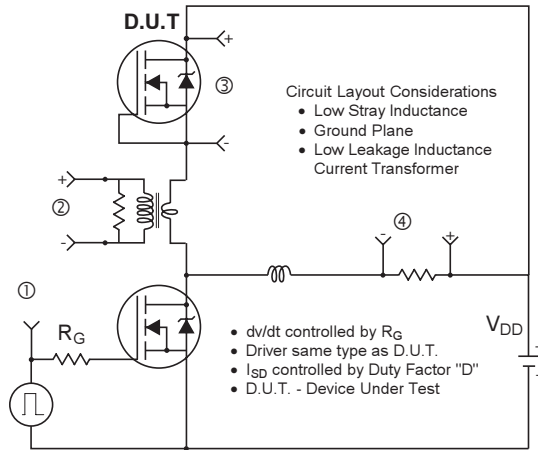


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

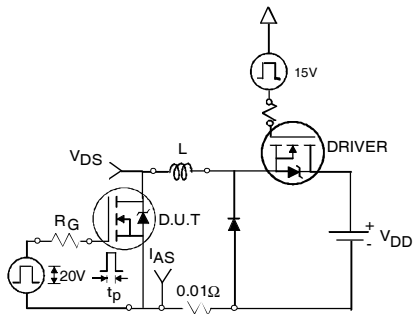


Fig 22a. Unclamped Inductive Test Circuit

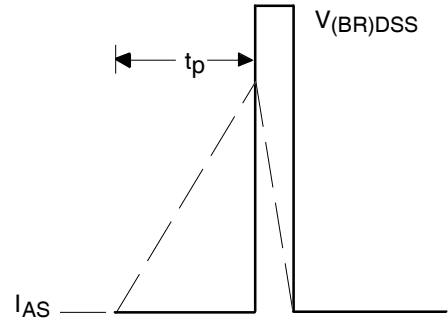


Fig 22b. Unclamped Inductive Waveforms

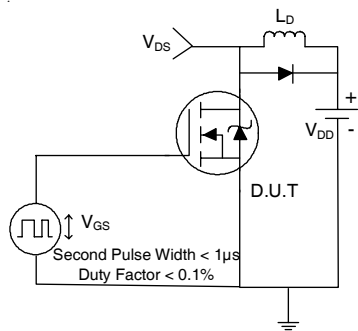


Fig 23a. Switching Time Test Circuit

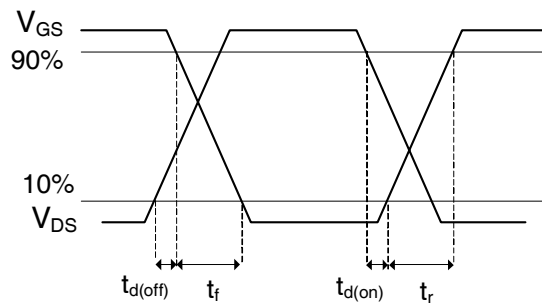


Fig 23b. Switching Time Waveforms

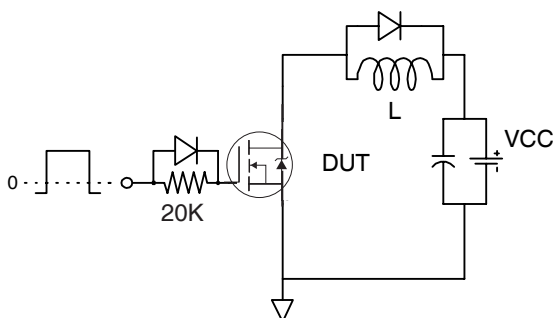


Fig 24a. Gate Charge Test Circuit

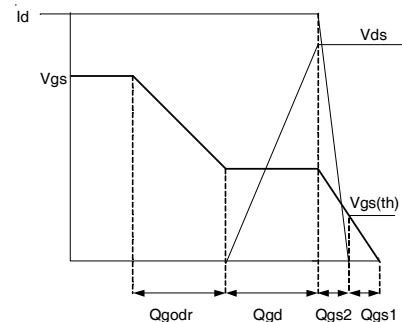
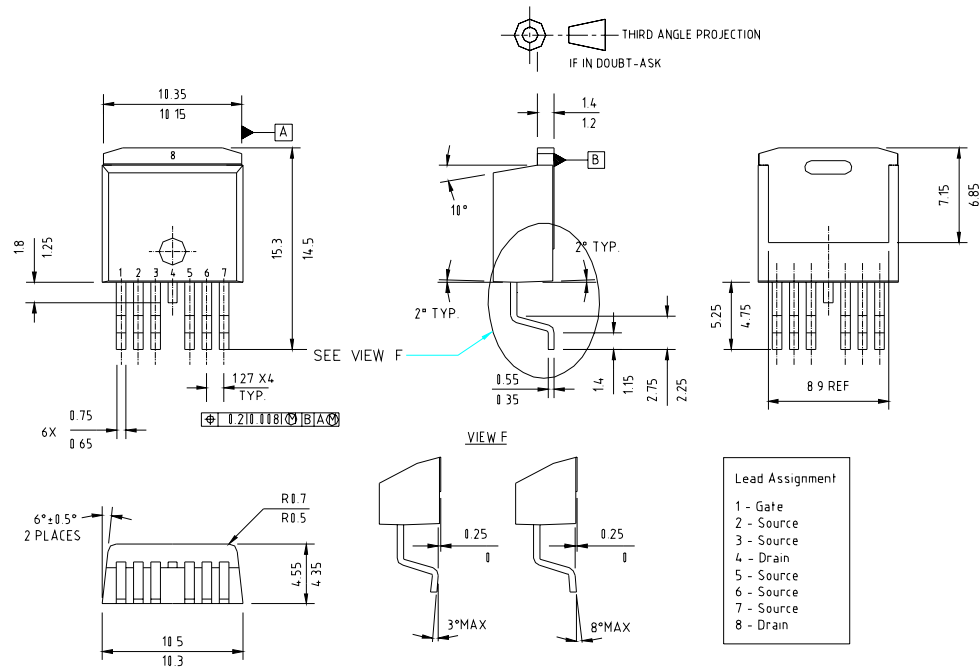


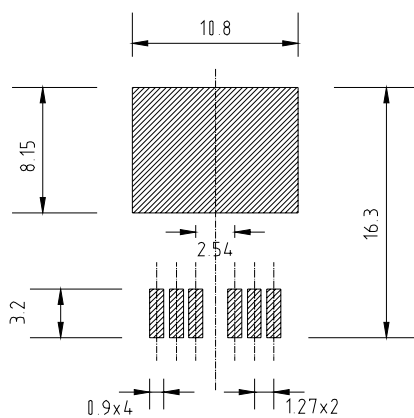
Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)

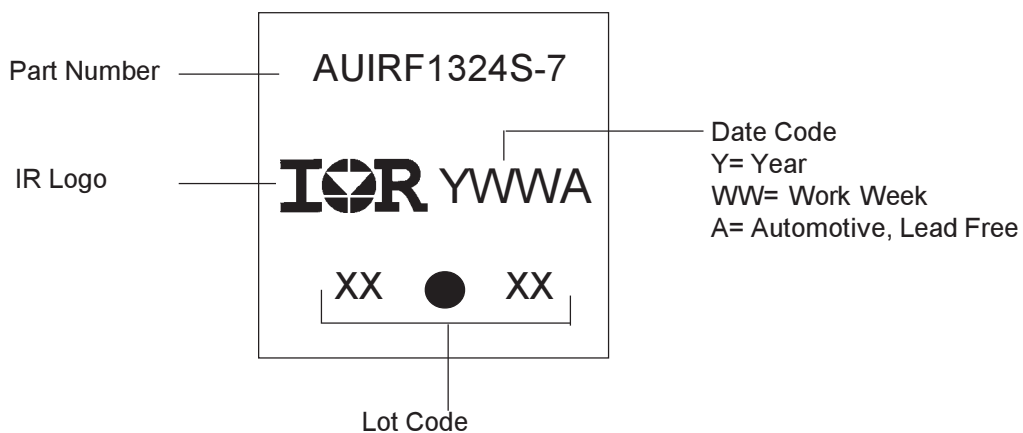


RECOMMENDED FOOTPRINT



REV	DATE	MODIFICATION
-	18/13/13	RAISED IAW ECN 3426
Rev1	07/14/13	CHANGED IAW ECN 3438
A	23/14/14	ADD LEAD ASSIGNMENT

D²Pak - 7 Pin Part Marking Information



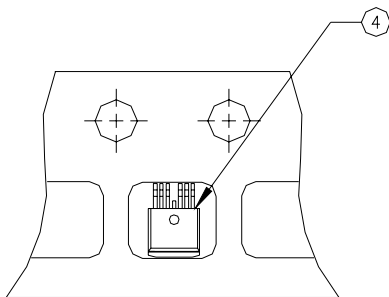
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/www.irf.com>

D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

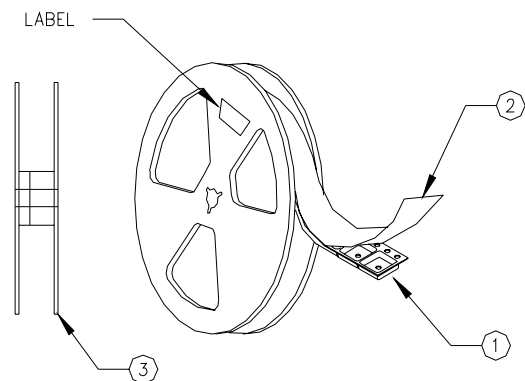
1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF1324S-7P	D2Pak	Tube	50	AUIRF1324S-7P
		Tape and Reel Left	800	AUIRF1324S-7PTRL
		Tape and Reel Right	800	AUIRF1324S-7PTRR

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For technical support, please contact IR's Technical Assistance Center

<http://www.irf.com/technical-info/>

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