

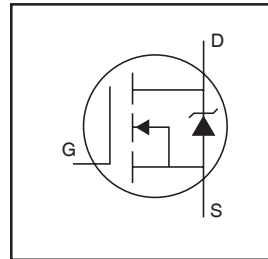
# AUIRFS4310 AUIRFS4310

## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

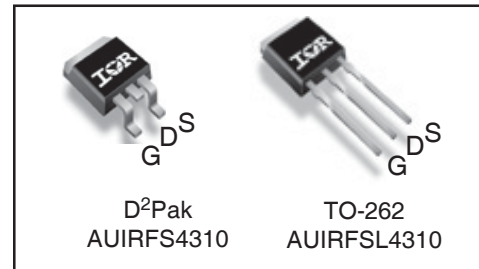
## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



## HEXFET® Power MOSFET

$V_{(BR)DSS}$	<b>100V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>5.6mΩ</b>
<b>max.</b>	<b>7.0mΩ</b>
$I_D$ (Silicon Limited)	<b>130A</b> ①
$I_D$ (Package Limited)	<b>75A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	130①	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	92①	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited)	75	
$I_{DM}$	Pulsed Drain Current ②	550	
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally limited) ③	980	mJ
$I_{AR}$	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy		mJ
$dV/dt$	Peak Diode Recovery ④	14	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑥	—	40	

HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

**Static Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.064	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.6	7.0	m $\Omega$	$V_{GS} = 10V, I_D = 75A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
gfs	Forward Transconductance	160	—	—	S	$V_{DS} = 50V, I_D = 75A$
$R_G$	Gate Input Resistance	—	1.4	—	$\Omega$	f = 1MHz, open drain
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	170	250	nC	$I_D = 75A$
$Q_{gs}$	Gate-to-Source Charge	—	46	—		$V_{DS} = 80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	62	—		$V_{GS} = 10V$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	$V_{DD} = 65V$
$t_r$	Rise Time	—	110	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	68	—		$R_G = 2.6\Omega$
$t_f$	Fall Time	—	78	—		$V_{GS} = 10V$ ⑤
$C_{iss}$	Input Capacitance	—	7670	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	540	—		$V_{DS} = 50V$
$C_{rss}$	Reverse Transfer Capacitance	—	280	—		f = 1.0MHz
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	650	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑦, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	720.1	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑧, See Fig. 5

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	130	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ②⑦	—	—	550		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ⑤
$t_{rr}$	Reverse Recovery Time	—	45	68	ns	$T_J = 25^\circ\text{C}$ $V_R = 85V,$ $T_J = 125^\circ\text{C}$ $I_F = 75A$ $di/dt = 100A/\mu s$ ⑤
$Q_{rr}$	Reverse Recovery Charge	—	82	120		
		—	120	180	nC	$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	3.3	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.35\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 75A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ④  $I_{SD} \leq 75A$ ,  $di/dt \leq 550A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

- ⑥  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

## Qualification Information<sup>†</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q101) <sup>††</sup>	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
		TO-262	N/A
<b>Moisture Sensitivity Level</b>		D <sup>2</sup> PAK	MSL1
<b>ESD</b>	Machine Model	Class M4(425V) (per AEC-Q101-002)	
	Human Body Model	Class H2(4000V) (per AEC-Q101-001)	
	Charged Device Model	Class C4 (1000V) (per AEC-Q101-005)	
<b>RoHS Compliant</b>		Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

<sup>††</sup> Exceptions to AEC-Q101 requirements are noted in the qualification report.

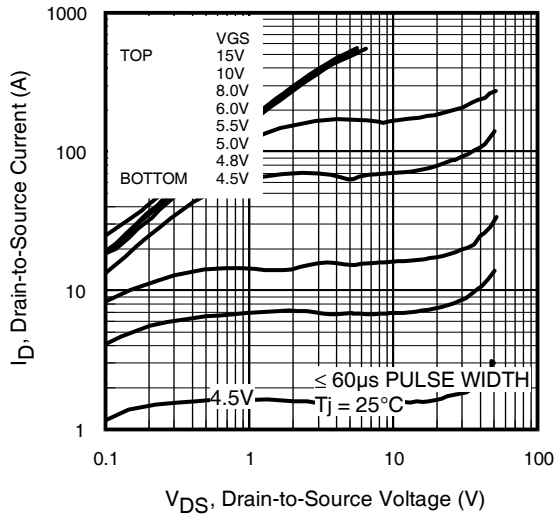


Fig 1. Typical Output Characteristics

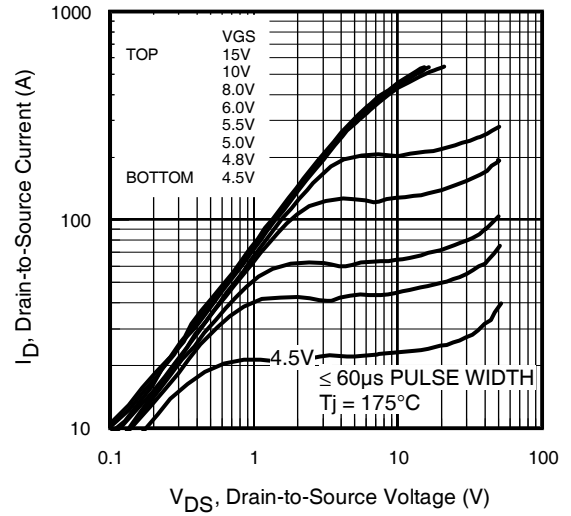


Fig 2. Typical Output Characteristics

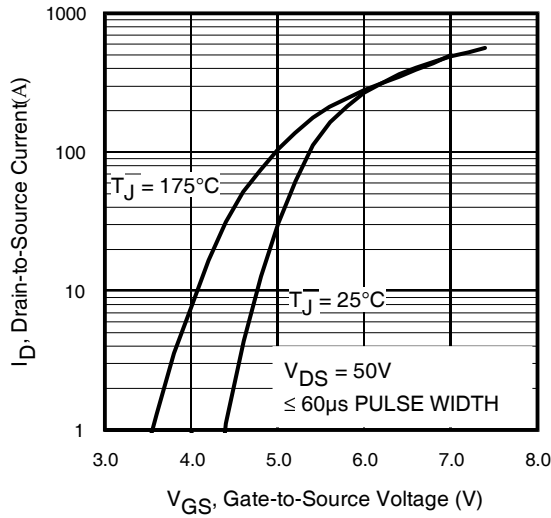


Fig 3. Typical Transfer Characteristics

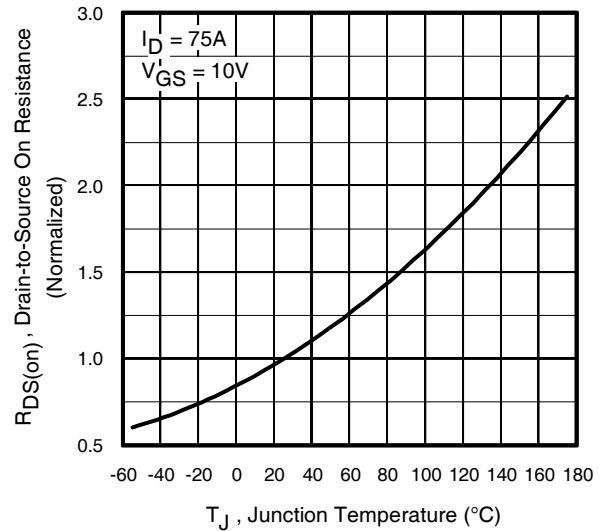


Fig 4. Normalized On-Resistance vs. Temperature

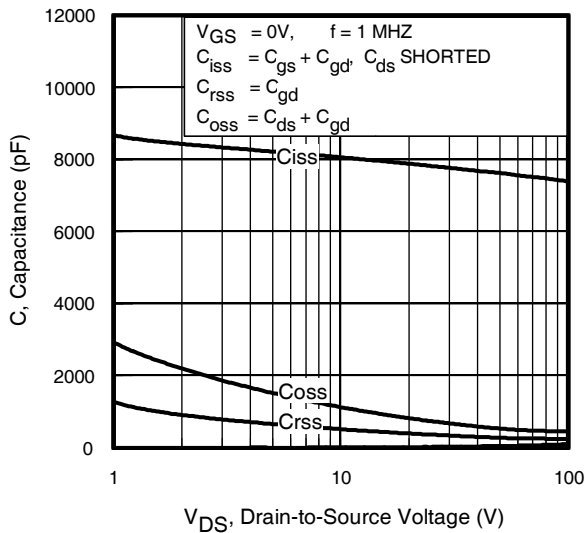


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

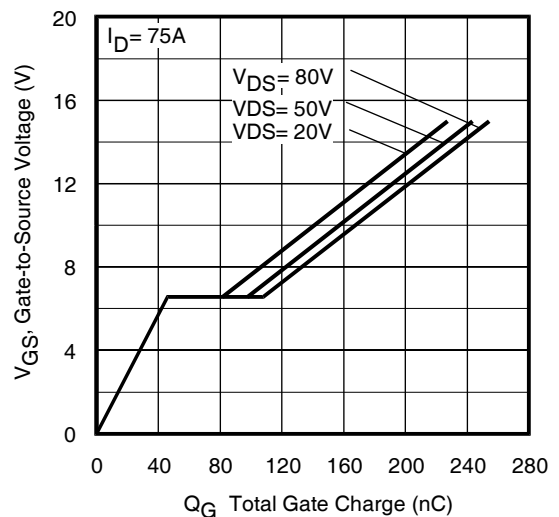
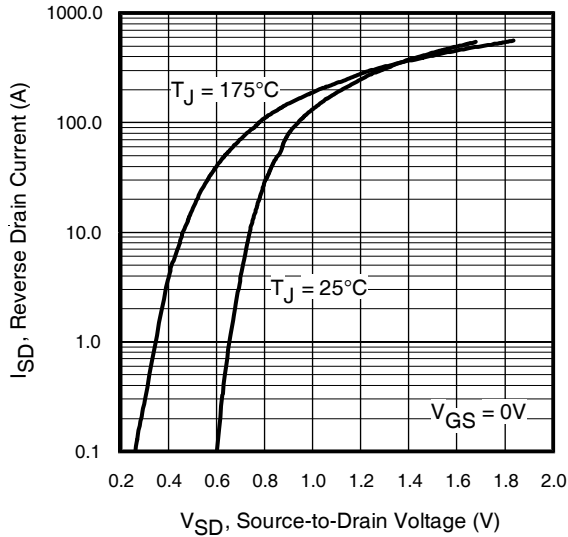
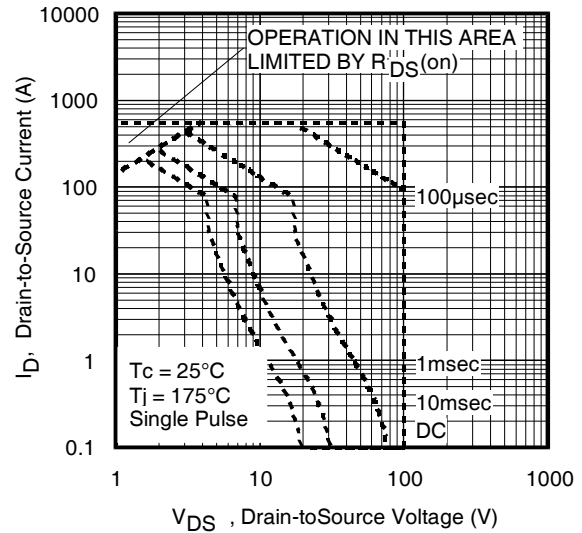


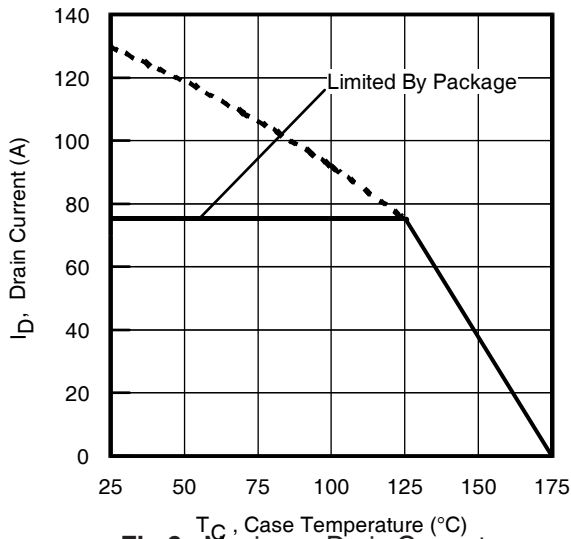
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



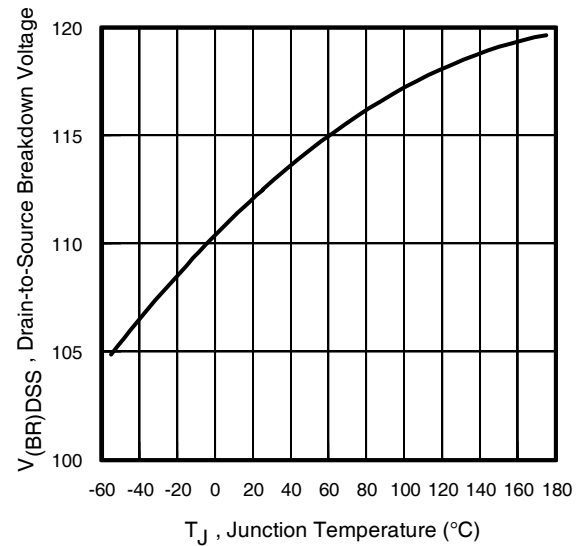
**Fig 7.** Typical Source-Drain Diode Forward Voltage



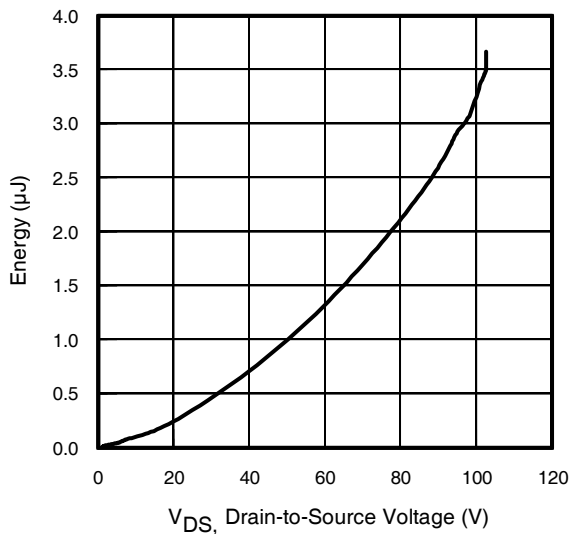
**Fig 8.** Maximum Safe Operating Area



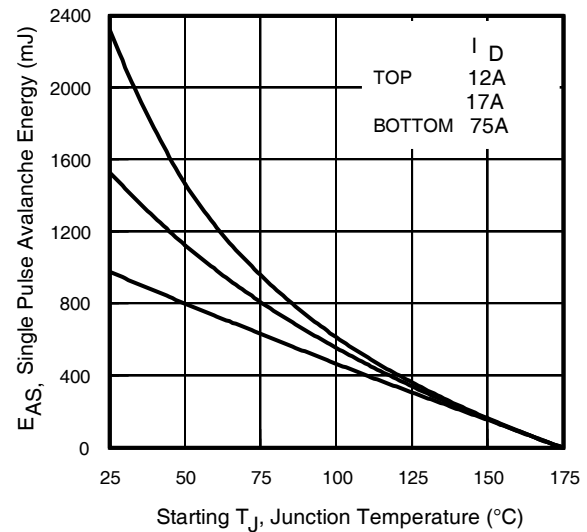
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. Drain Current

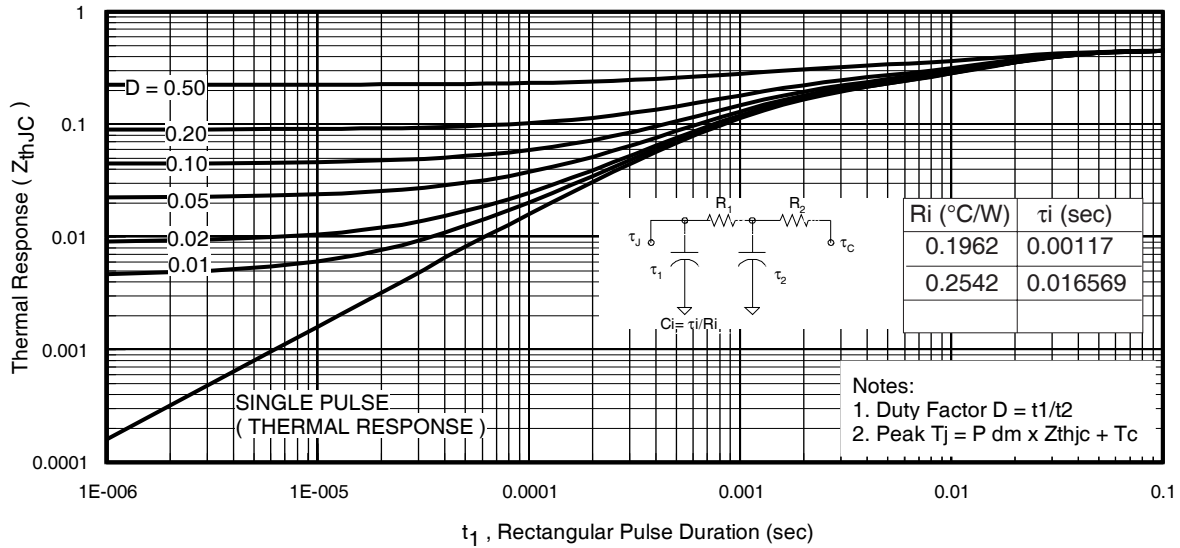


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

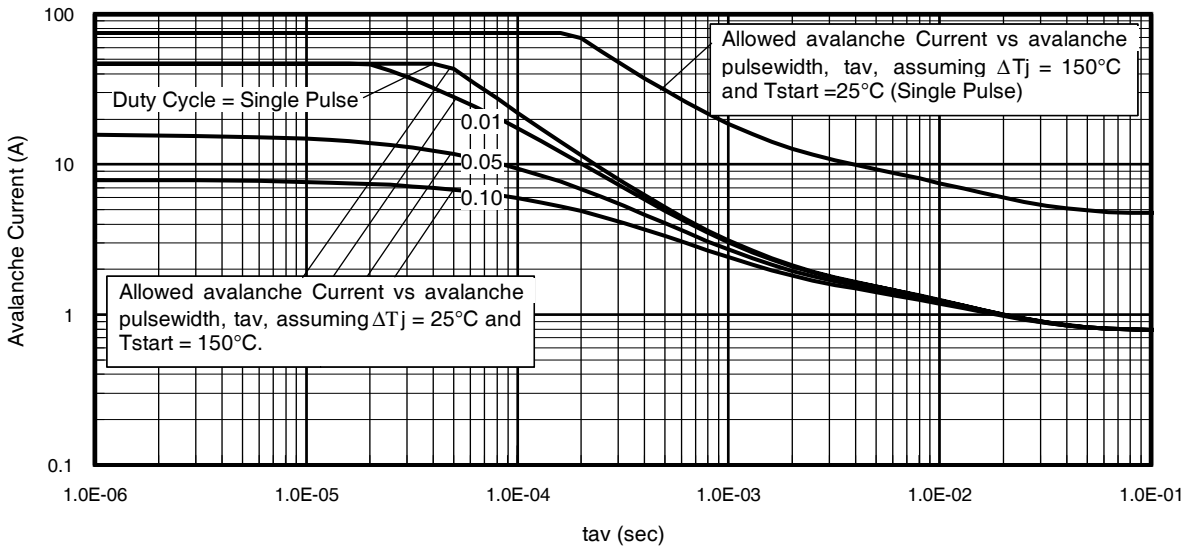


Fig 14. Typical Avalanche Current vs. Pulsewidth

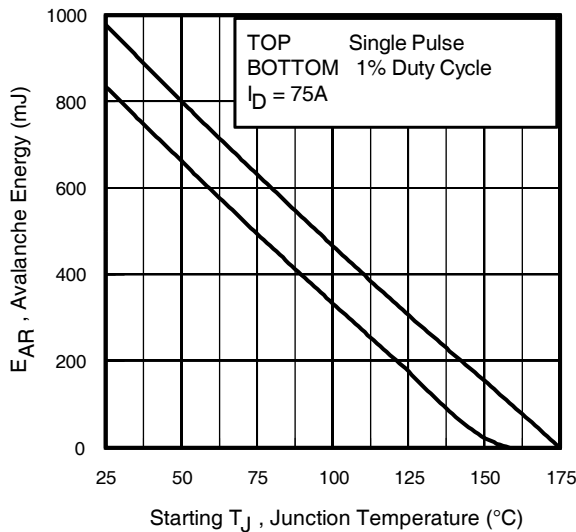


Fig 15. Maximum Avalanche Energy vs. Temperature

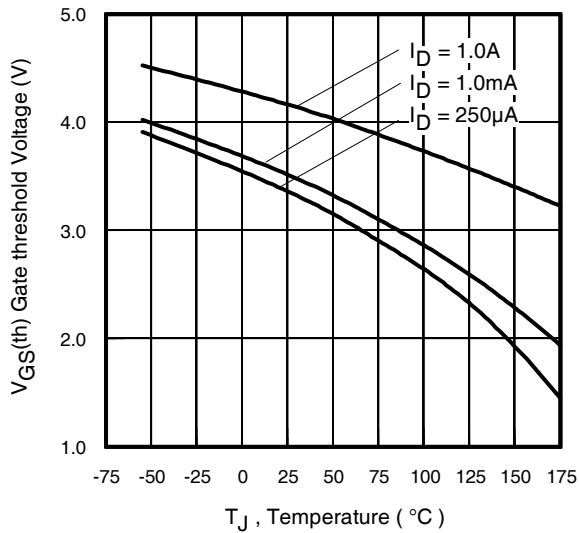
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither  $T_{jmax}$  nor  $I_{av} (max)$  is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_D (ave)$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^{\circ}\text{C}$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

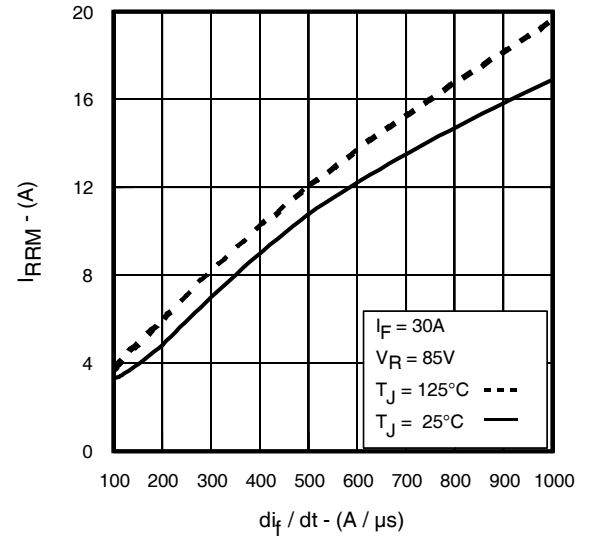
$$P_D (ave) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

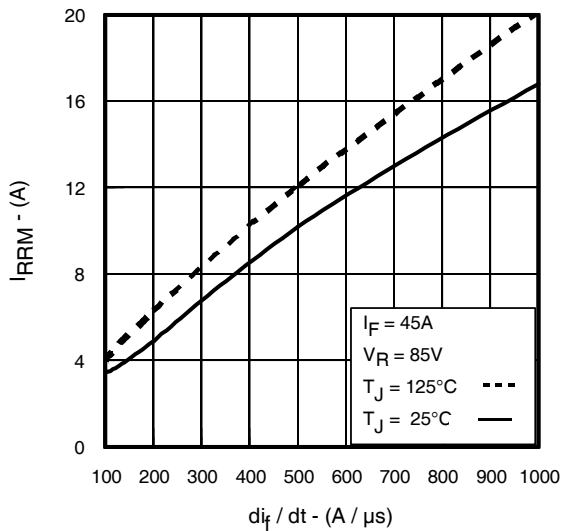
$$E_{AS} (AR) = P_D (ave) \cdot t_{av}$$



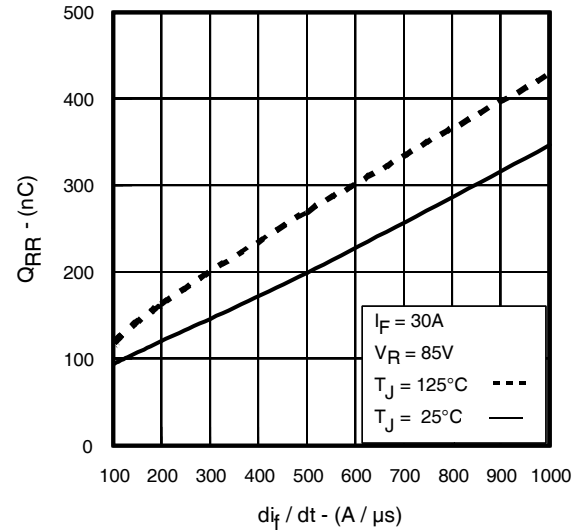
**Fig. 16.** Threshold Voltage Vs. Temperature



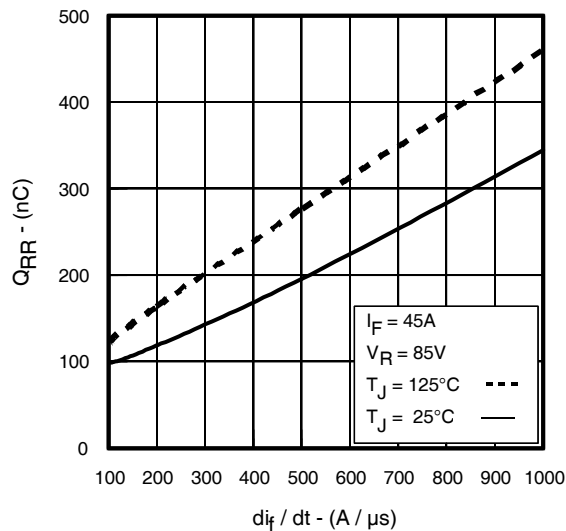
**Fig. 17 -** Typical Recovery Current vs.  $di_T/dt$



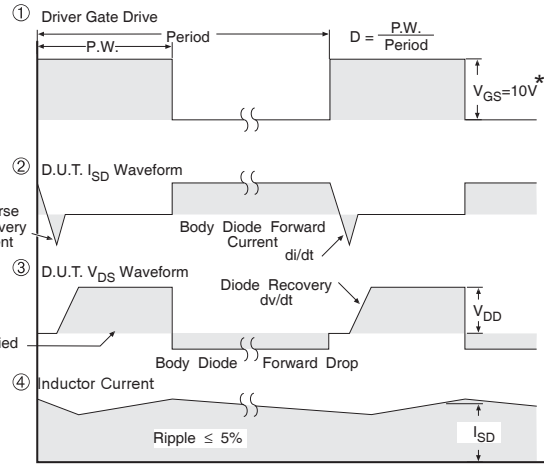
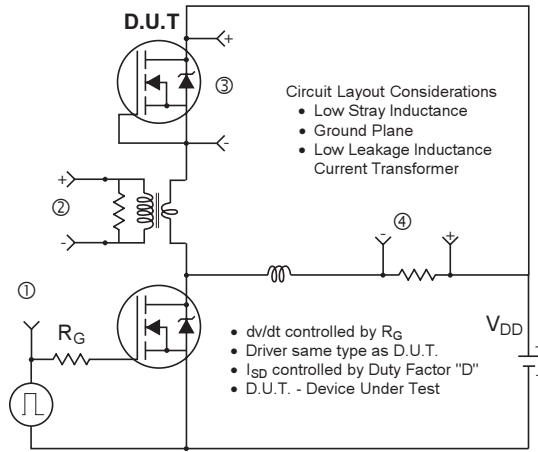
**Fig. 18 -** Typical Recovery Current vs.  $di_T/dt$



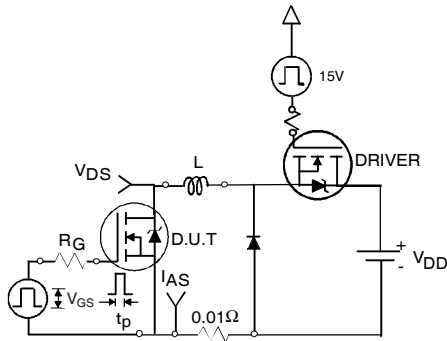
**Fig. 19 -** Typical Stored Charge vs.  $di_T/dt$



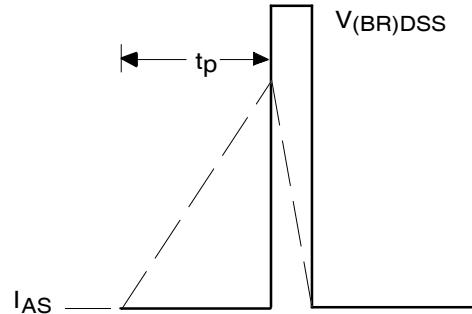
**Fig. 20 -** Typical Stored Charge vs.  $di_T/dt$



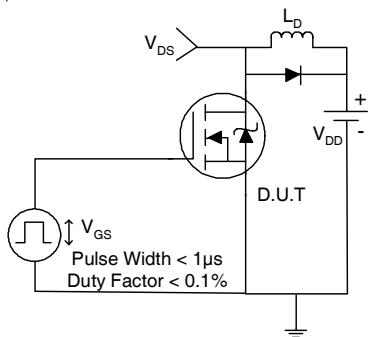
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



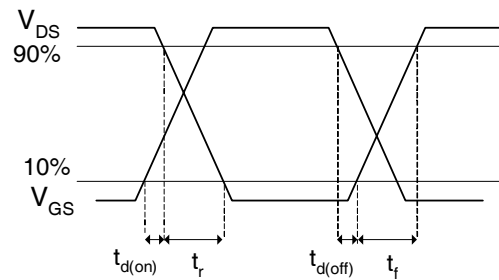
**Fig 22a. Unclamped Inductive Test Circuit**



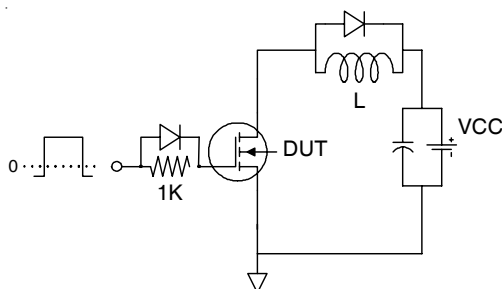
**Fig 22b. Unclamped Inductive Waveforms**



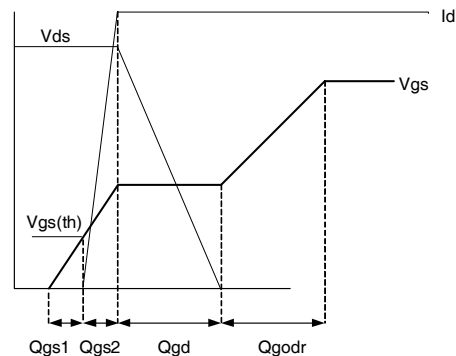
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



**Fig 24a. Gate Charge Test Circuit**

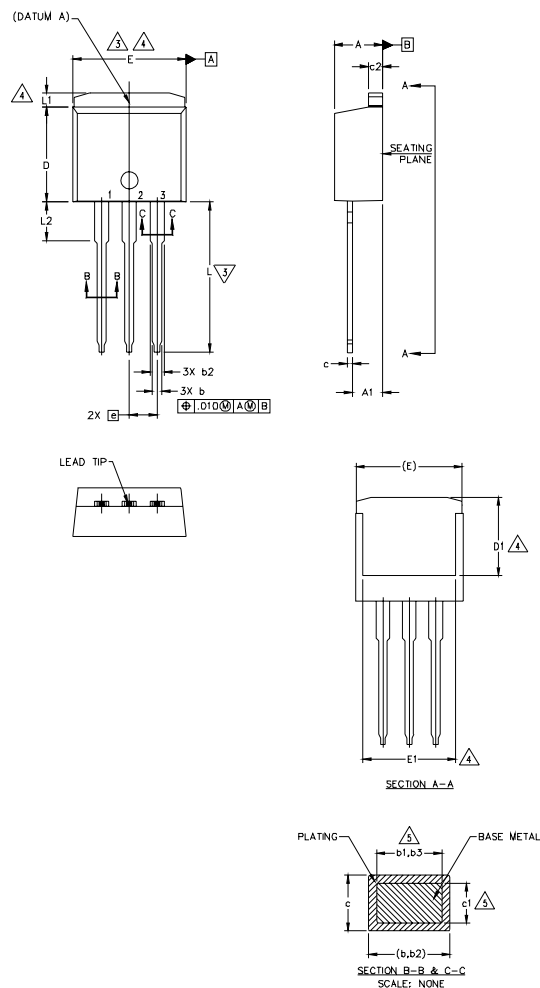


**Fig 24b. Gate Charge Waveform**



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	4
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	

### LEAD ASSIGNMENTS

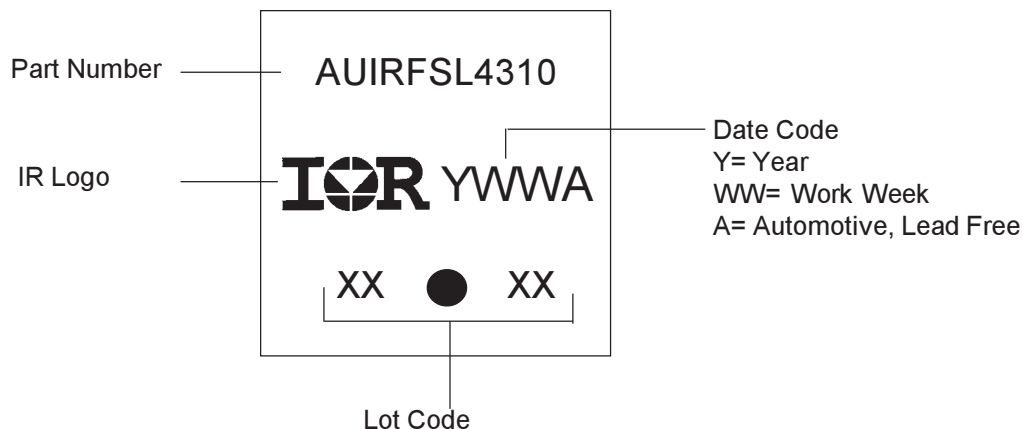
#### HEXFET

- 1.— GATE
- 2.— DRAIN
- 3.— SOURCE
- 4.— DRAIN

#### IGBTs, CoPACK

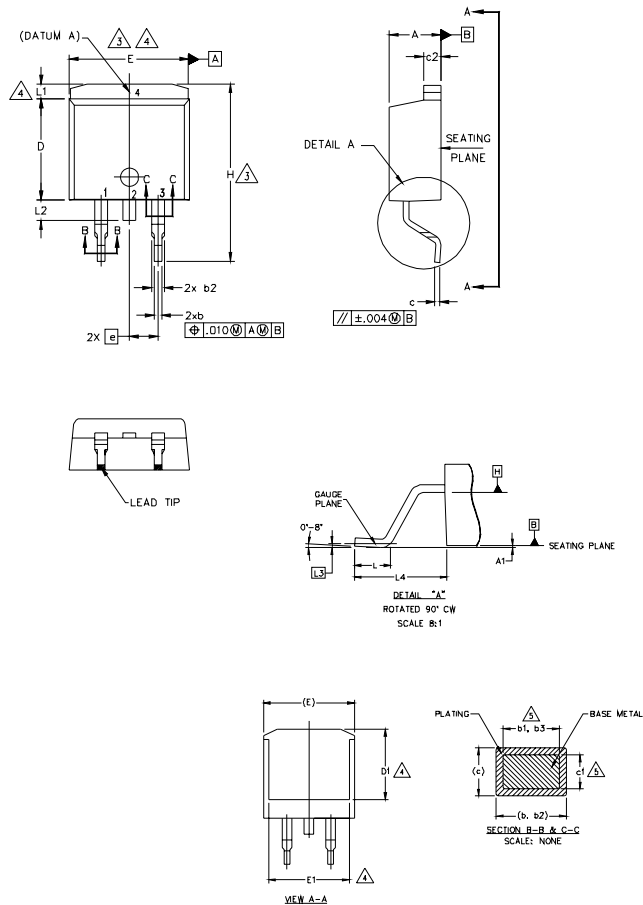
- 1.— GATE
- 2.— COLLECTOR
- 3.— EMITTER
- 4.— COLLECTOR

## TO-262 Part Marking Information



## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	4
L2	1.27	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.— GATE
- 2, 4.— DRAIN
- 3.— SOURCE

#### IGBTs, CoPACK

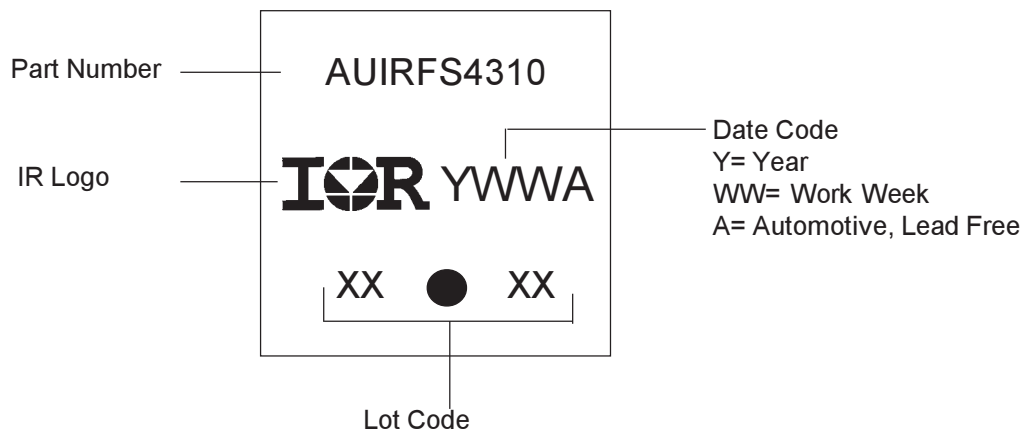
- 1.— GATE
- 2, 4.— COLLECTOR
- 3.— EMITTER

#### DIODES

- 1.— ANODE \*
- 2, 4.— CATHODE
- 3.— ANODE

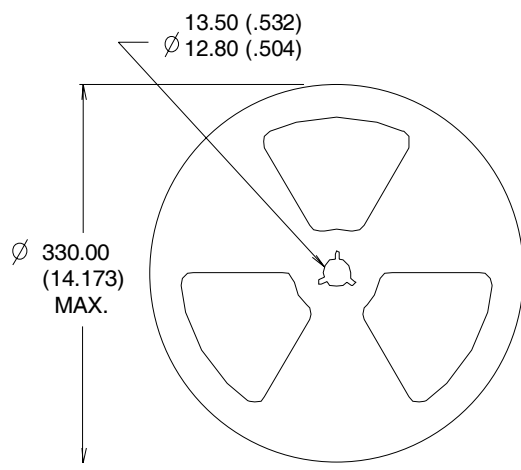
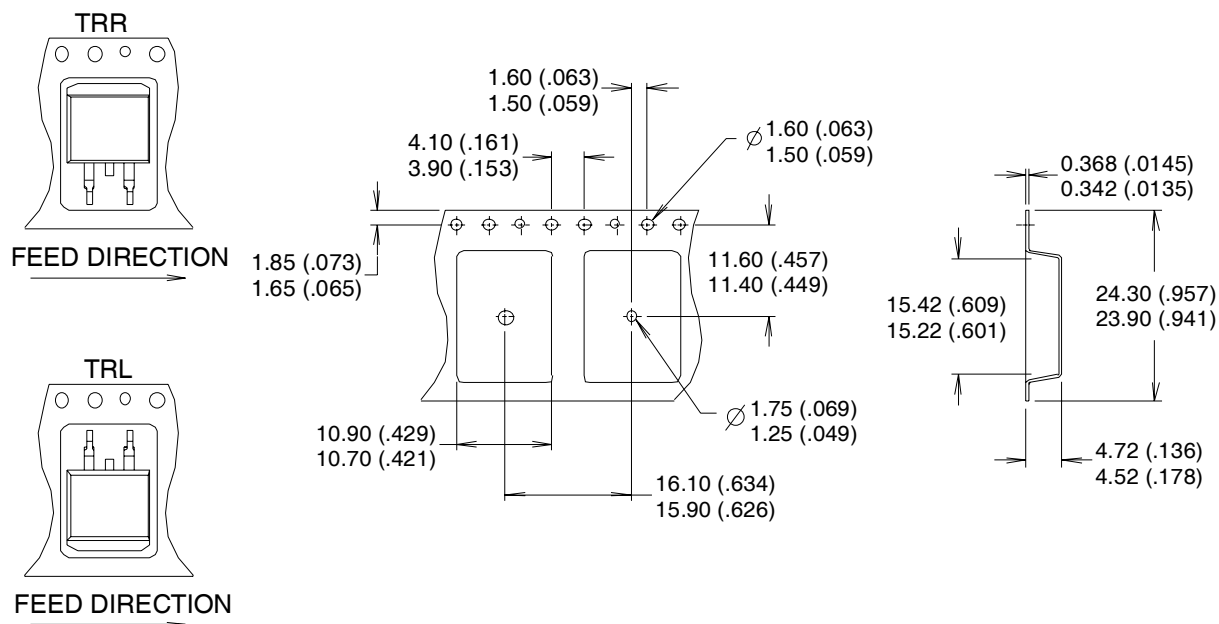
\* PART DEPENDENT.

## D<sup>2</sup>Pak (TO-263AB) Part Marking Information



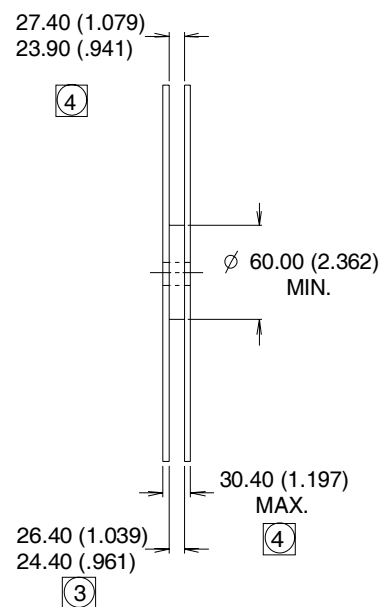
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information



### NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



**Ordering Information**

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFSL4310	TO-262	Tube	50	AUIRFSL4310
AUIRFS4310	D2Pak	Tube	50	AUIRFS4310
		Tape and Reel Left	800	AUIRFS4310TRL
		Tape and Reel Right	800	AUIRFS4310TRR

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