Synchronous Buck FET Driver Optimized for High-Frequency Applications

Check for Samples: TPS51604

FEATURES

- **Reduced Dead-Time Drive Circuit for Optimized CCM**
- **Automatic Zero Crossing Detection for Optimized DCM Efficiency**
- **Multiple Low-Power Modes for Optimized Light-Load Efficiency**
- **Optimized Signal Path Delays for High-Frequency Operation**
- **Integrated BST Switch Drive Strength Optimized for Ultrabook FETs**
- **Optimized for 5-V FET Drive**
- **Conversion Input Voltage Range (V_{IN}): 4.5 V to 28 V**
- **Small, 2 mm x 2 mm, 8-Pin, WSON Power Pad Package**

APPLICATIONS

- **High Frequency CPU V_{CORE} Applications Powered By:**
  - **Adapter**
  - **Battery**
  - **NVDC**
  - **5-V or 12-V Rails**

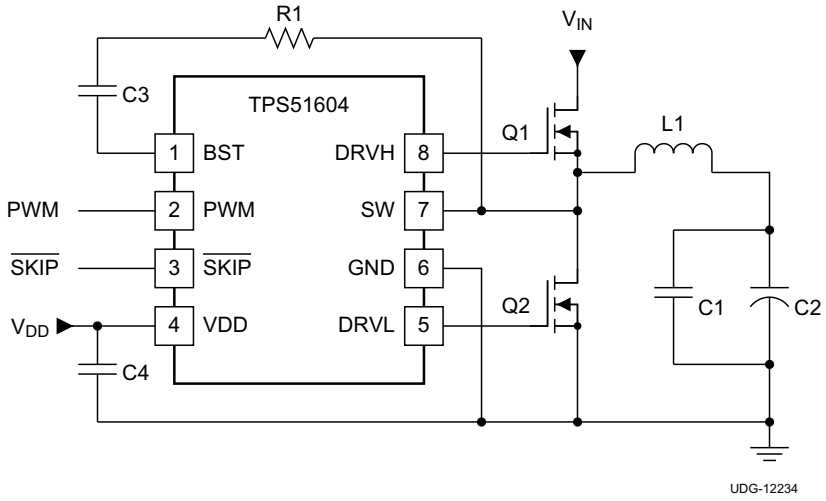
DESCRIPTION

The TPS51604 drivers are optimized for high-frequency CPU V_{CORE} applications. Advanced features such as reduced dead-time drive and Auto Zero Crossing are used to optimize efficiency over the entire load range.

The $\overline{SKIP}$ pin provides immediate CCM operation to support controlled management of the output voltage. In addition, the TPS51604 supports two low-power modes. With the PWM input in tri-state, quiescent current is reduced to 130 µA, with immediate response. When $\overline{SKIP}$ is held at tri-state, the current is reduced to 8 µA (typically 20 µs is required to resume switching). Paired with the appropriate TI controller, the drivers deliver an exceptionally high performance power supply system.

The TPS51604 is packaged in a space saving, thermally enhanced 8-pin, 2 mm x 2 mm WSON package and operates from –40°C to 105°C.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD	–0.3	6	V
	PWM, $\overline{SKIP}$	–0.3	6	
Output voltage	BST	–0.3	35	V
	BST (transient < 20 ns)	–0.3	38	
	BST to SW; DRVH to SW	–0.3	6	
	SW	–2	30	
	DRVH, SW (transient < 20 ns)	–5	38	
	DRVL	–0.3	6	
Ground pins	GND to PAD	–0.3	0.3	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51604 WSON (DSG) (8 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	63.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	74.1	
θ_{JB}	Junction-to-board thermal resistance	34.3	
ψ_{JT}	Junction-to-top characterization parameter	2.0	
ψ_{JB}	Junction-to-board characterization parameter	34.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	11.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage	VDD	4.5	5.0	5.5	V
	PWM, $\overline{SKIP}$	–0.1		5.5	
Output voltage	BST	–0.1		34	V
	BST to SW; DRVH to SW	–0.1		5.5	
	SW	–1.0		28	
	DRVL	–0.1		5.5	
Ground pins	GND to PAD	–0.1		0.1	V
Operating junction temperature, T_J		–40		105	°C

ELECTRICAL CHARACTERISTICS

These specifications apply for T_J = –40°C to 105°C and VDD = 5.0V unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VDD INPUT SUPPLY						
I_{CC}	Supply current (operating)	$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = High		160	600	µA
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Low		250		
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Float		130		
		$V_{\overline{SKIP}}$ = Float		8		
VDD UNDERVOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	UVLO threshold	Rising threshold			4.15	V
		Falling threshold	3.7			
V_{UVHYS}	UVLO hysteresis			0.2		V
PWM AND $\overline{SKIP}$ I/O SPECIFICATIONS						
R_I	Input impedance	Pull up to VDD		1.7		MΩ
		Pull down (to GND)		800		kΩ
V_{IL}	Low-level input voltage				0.6	V
V_{IH}	High-level input voltage		2.65			
V_{IHH}	Hysteresis			0.2		
V_{TS}	Tri-state voltage		1.3		2.0	
$t_{THOLD(off1)}$	Tri-state activation time (falling) PWM			60		ns
$t_{THOLD(off2)}$	Tri-state activation time (rising) PWM			60		
t_{TSKF}	Tri-state activation time (falling) $\overline{SKIP}$			1		µs
t_{TSKR}	Tri-state activation time (rising) $\overline{SKIP}$			1		
$t_{3RD(PWM)}$	Tri-state exit time PWM				100	ns
$t_{3RD(\overline{SKIP})}$	Tri-state exit time $\overline{SKIP}$				50	µs
HIGH-SIDE GATE DRIVER (DRVH)						
$t_{R(DRVH)}$	Rise time	DRVH rising, C_{DRVH} = 3.3 nF; 20% to 80%		30		ns
$t_{RPD(DRVH)}$	Rise time propogation delay	C_{DRVH} = 3.3 nF		40		ns
R_{SRC}	Source resistance	Source resistance, (V_{BST}– V_{SW}) = 5 V, high state, (V_{BST}–V_{DRVH}) = 0.1 V		4	8	Ω
$t_{F(DRVH)}$	Fall time	DRVH falling, C_{DRVH} = 3.3 nF		8		ns
$t_{FPD(DRVH)}$	Fall-time propagation delay	C_{DRVH} = 3.3 nF		25		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{BST}–V_{SW}) forced to 5 V, low state (V_{DRVH}–V_{SW}) = 0.1 V		0.5	1.6	Ω
R_{DRVH}	DRVH to SW resistance(1)			100		kΩ
LOW-SIDE GATE DRIVER (DRVL)						
$t_{R(DRVL)}$	Rise time	DRVL rising, C_{DRVL} = 3.3 nF; 20% to 80%		15		ns
$t_{RPD(DRVL)}$	Rise time propogation delay	C_{DRVL} = 3.3 nF		35		ns
R_{SRC}	Source resistance	Source resistance, (V_{VDD}–GND) = 5 V, high state, (V_{VDD}–V_{DRVL}) = 0.1 V		1.5	3	Ω
$t_{F(DRVL)}$	Fall time	DRVL falling, C_{DRVL} = 3.3 nF		10		ns
$t_{FPD(DRVL)}$	Fall-time propagation delay	C_{DRVL}= 3.3 nF		15		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{VDD}– GND) = 5 V, low state, (V_{DRVL}–GND) = 0.1 V		0.4	1.6	Ω
R_{DRVL}	DRVL to GND resistance(1)			100		kΩ

(1) Specified by design. Not production tested.

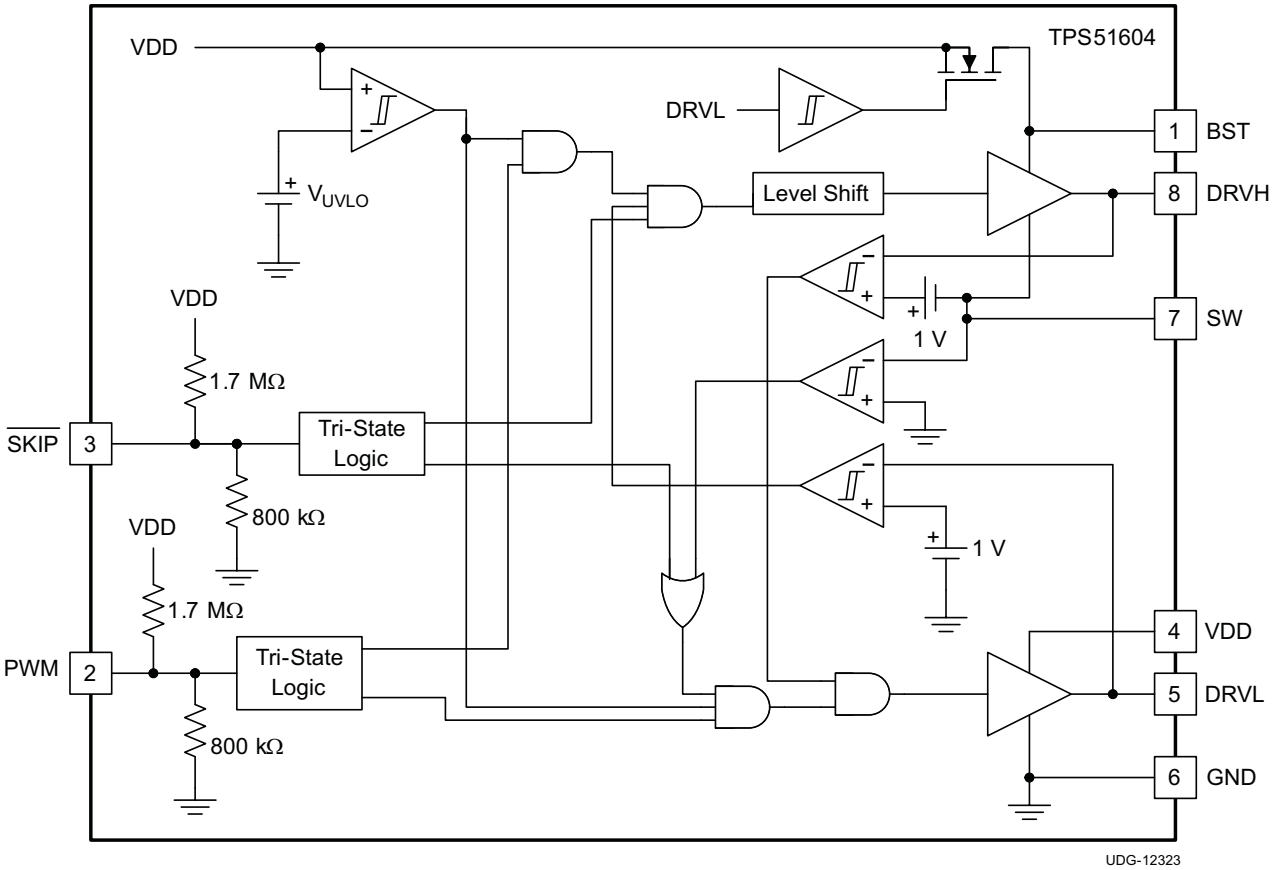
ELECTRICAL CHARACTERISTICS (continued)

These specifications apply for T_J = –40°C to 105°C and VDD = 5.0V unless otherwise specified.

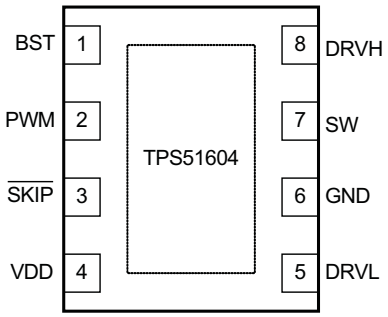
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER DEAD-TIME						
$t_{R(DT)}$	Rising edge		0	20	35	ns
$t_{F(DT)}$	Falling edge		0	10	25	ns
ZERO CROSSING COMPARATOR						
V_{ZX}	Zero crossing offset	SW voltage rising	–2.25	0	2.00	mV
BOOTSTRAP SWITCH						
V_{FBST}	Forward voltage	I_F = 10 mA		120	240	mV
I_{RLEAK}	Reverse leakage	(V_{BST} – V_{VDD}) = 25 V			2	µA
$R_{DS(on)}$	On-resistance			12	24	Ω

DEVICE INFORMATION

Functional Block Diagram



DSG
8 PINS
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BST	1	I	High-side N-channel FET bootstrap voltage input; power supply for high-side driver.
DRVH	8	O	High-side N-channel gate drive output.
DRVL	5	O	Synchronous low-side N-channel gate drive output
GND	6	–	Synchronous low-side N-channel gate drive return and IC reference.
PWM	2	I	PWM input. A tri-state voltage on this pin turns OFF both the high-side (DRVH) and low-side drivers (DRVL)
$\overline{\text{SKIP}}$	3	I	When $\overline{\text{SKIP}}$ is LO, the zero crossing comparator is active; the power chain enters discontinuous conduction mode when the inductor current reaches zero. When $\overline{\text{SKIP}}$ is HI, the zero crossing comparator is disabled, and the driver outputs follow the PWM input. A tri-state voltage on $\overline{\text{SKIP}}$ puts the driver into a very low power state.
SW	7	I/O	High-side N-channel gate drive return. Also, zero-crossing sense input.
VDD	4	I	5-V power supply input; decouple to GND with a ceramic capacitor with a value of 1 µF or greater.
Thermal Pad		–	Tie to system GND plane with multiple vias.

(1) I=Input, O=Output

TYPICAL CHARACTERISTICS

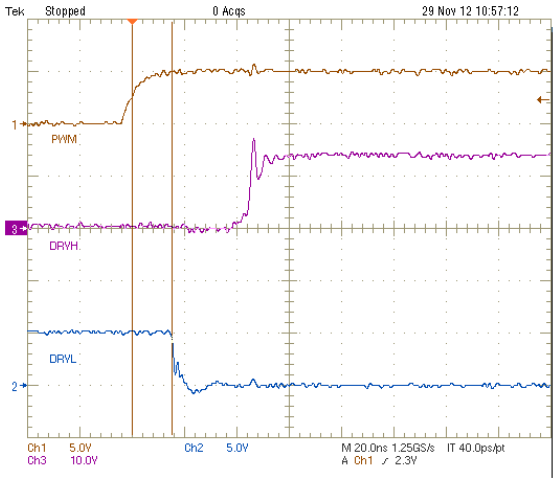


Figure 1. PWM High to DRVL Low

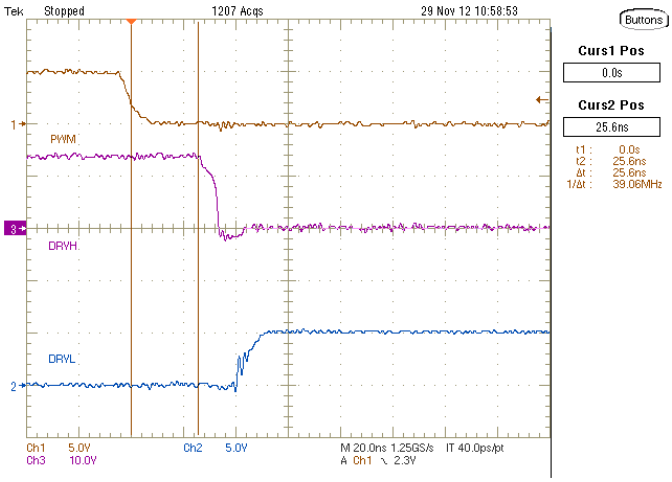


Figure 2. PWM Low to DRVH Low

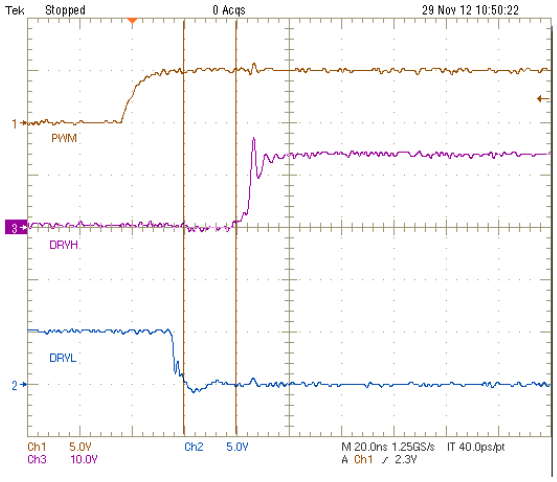


Figure 3. DRVL Low to DRVH High

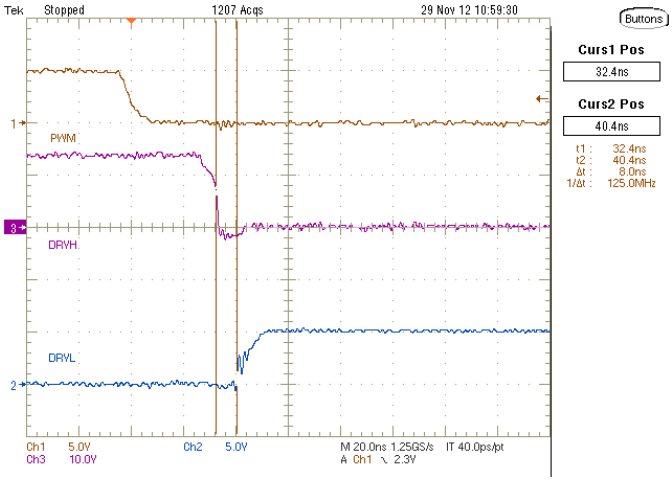


Figure 4. DRVH Low DRVL High

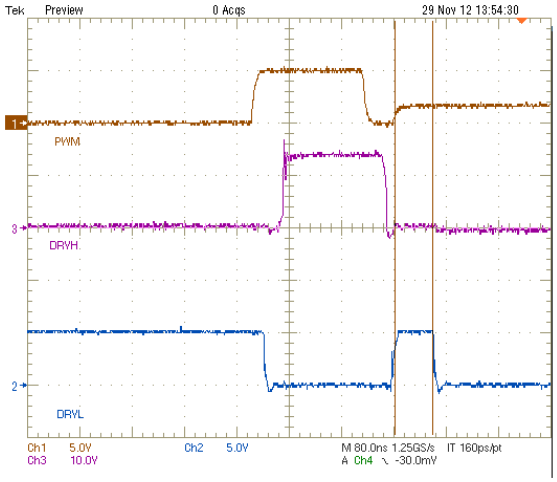


Figure 5. PWM Low to Tri-state

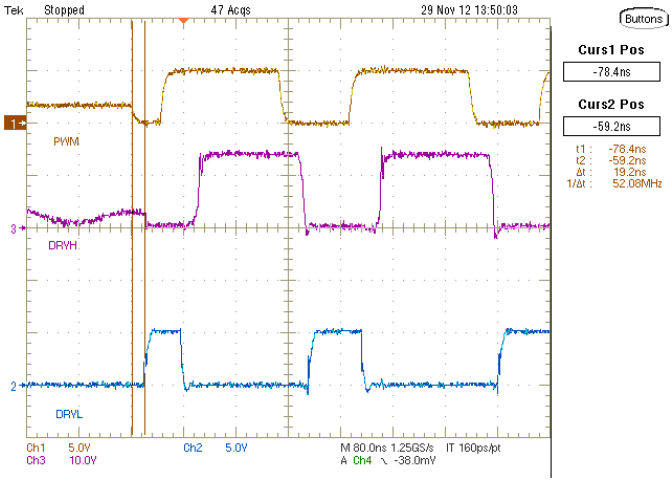


Figure 6. PWM Tri-State to Low

TYPICAL CHARACTERISTICS (continued)

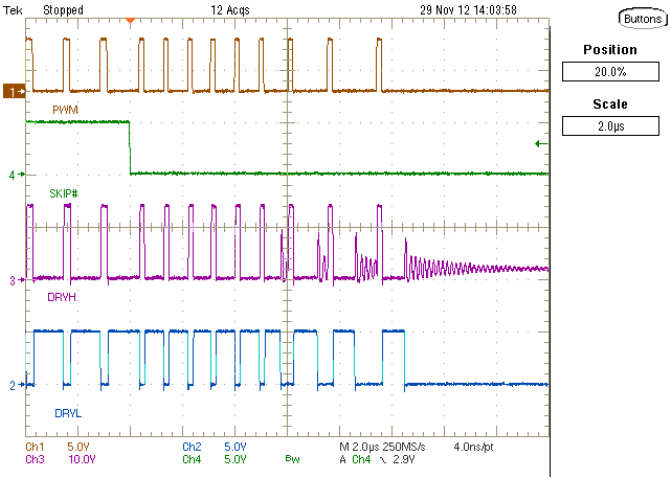


Figure 7. SKIP Mode Entry

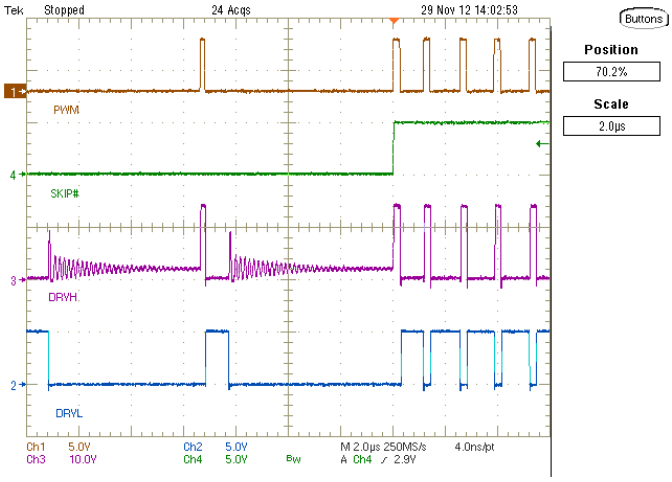


Figure 8. SKIP Mode Exit

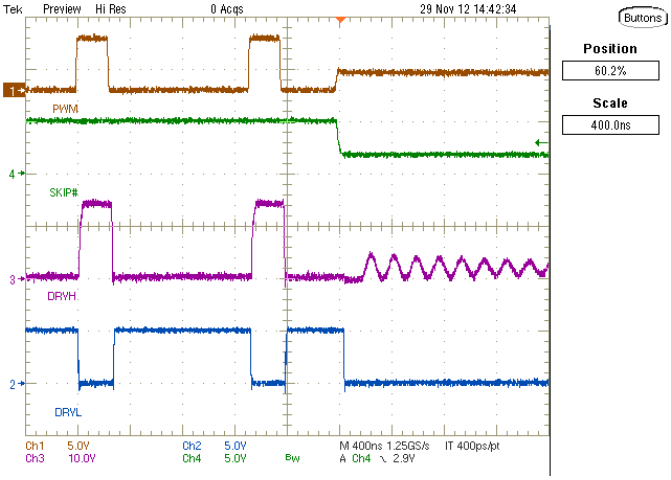


Figure 9. Very-Low-Power Mode Entry

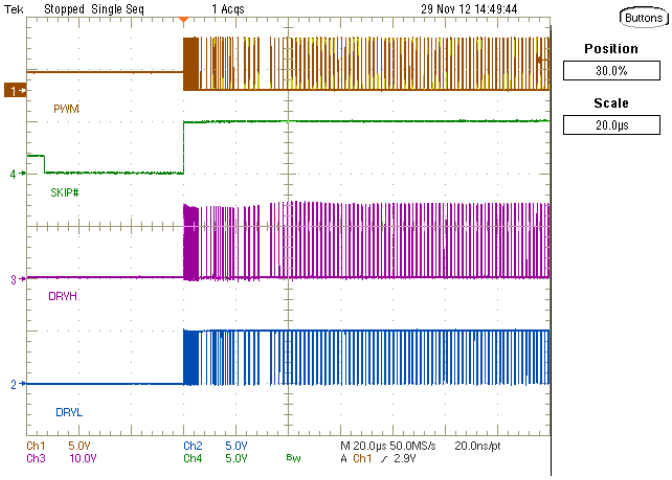


Figure 10. Very-Low-Power Mode Exit

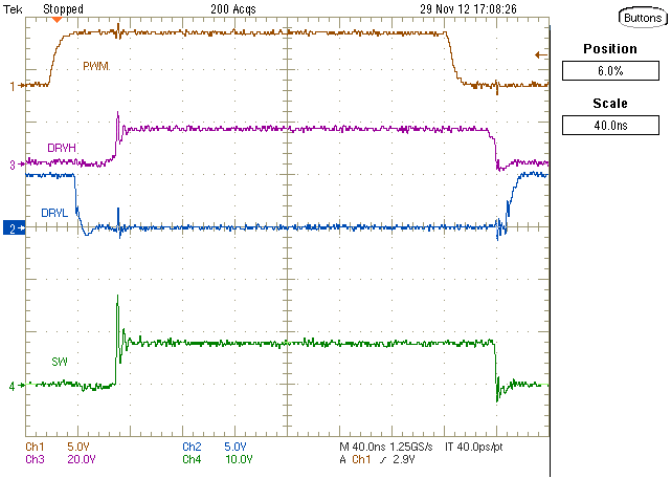


Figure 11. SW Node-Ringing at V_{IN} = 8 V

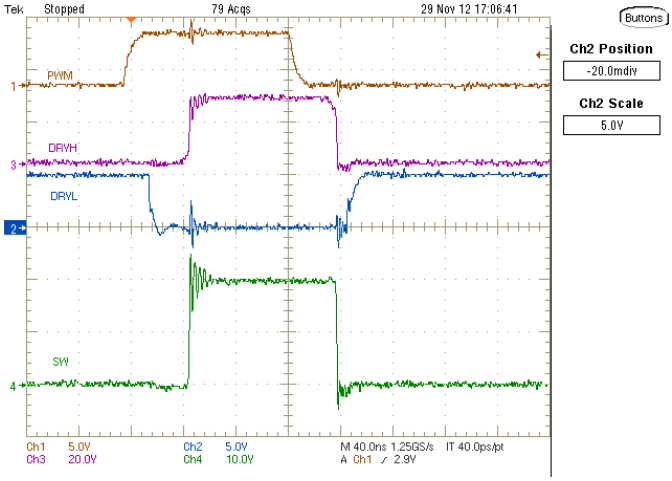


Figure 12. SW Node-Ringing at V_{IN} = 20 V

TYPICAL CHARACTERISTICS

Powerblock MOSFET: CSD87330(SLPS284) , Inductor: 0.22 µF, 1.1 mΩ DCR

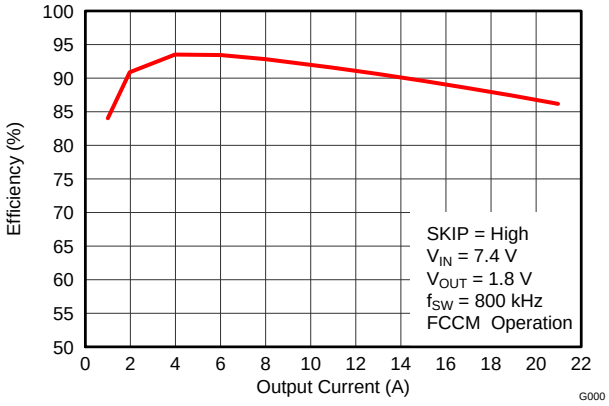


Figure 13. Efficiency vs. Output Current

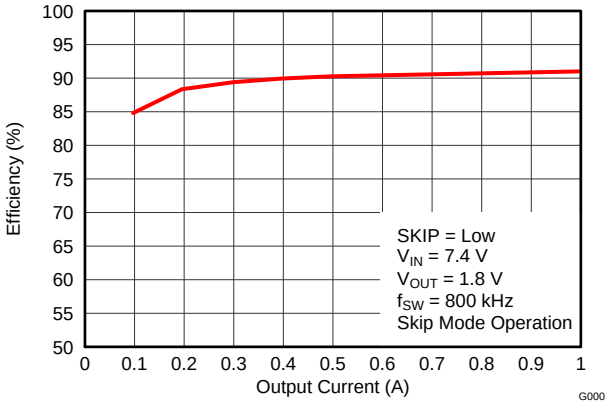


Figure 14. Efficiency vs. Output Current

DETAILED DESCRIPTION

The TPS51604 is a synchronous buck MOSFET driver designed to drive both high-side and low-side MOSFETs. It allows high-frequency operation with current driving capability matched to the application. The integrated boost switch is internal. The TPS51604 employs dead-time reduction control and shoot-through protection; which helps avoid simultaneous conduction of high-side and low-side MOSFETs. Also, the drivers improve light-load efficiency with integrated DCM mode operation using adaptive crossing detection. Typical applications yield a steady-state duty cycle of 60% or less. For high steady-state duty cycle applications, including a small external Schottky diode may help to ensure sufficient charging of the bootstrap capacitor.

Undervoltage Lockout Protection (UVLO)

The undervoltage lockout (UVLO) comparator evaluates the VDD voltage level. As V_{VDD} rises, both DRVH and DRVL hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H})., Then the driver becomes operational and responds to PWM and $\overline{SKIP}$ commands. If VDD falls below the lower UVLO threshold (V_{UVLO_L} = V_{UVLO_H} – Hysteresis), the device disables the driver and drives the outputs of DRVH and DRVL actively low. Figure 15 shows this function.

CAUTION

Do not start the driver in the very low power mode ($\overline{SKIP}$ = Tri-state).

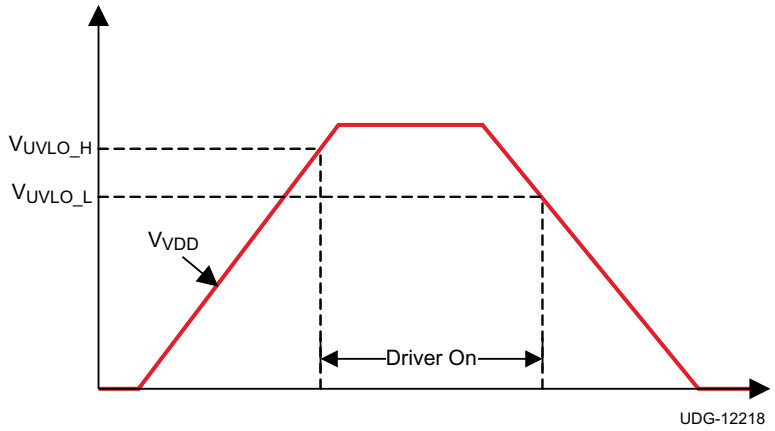


Figure 15. UVLO Operation

PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pull-up to maintain the voltage within the tri-state window during low-power modes. Operation into and out of tri-state mode follows the timing diagram outlined in Figure 16.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3 V (typ.) and 5.0 V (typ.) PWM drive signals.

When the PWM exits tri-state, the driver enters CCM for a period of 4 µs, regardless of the state of the $\overline{SKIP}$ pin. Normal operation requires this time period in order for the auto-zero comparator to resume.

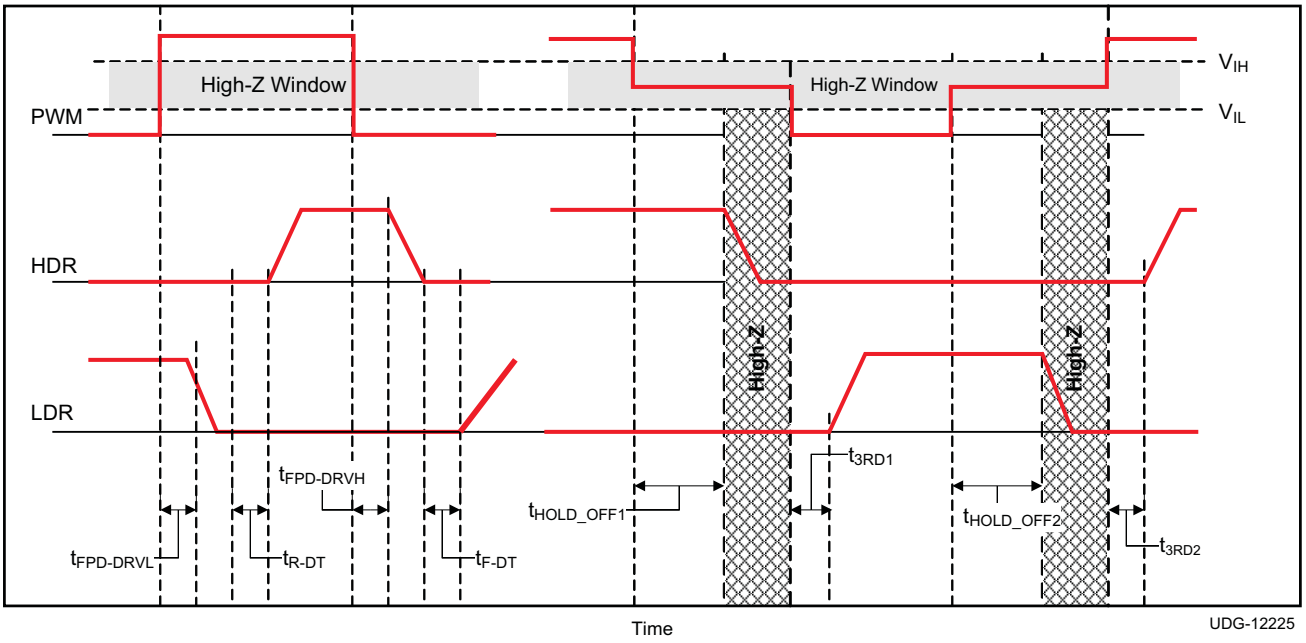


Figure 16. PWM Tri-State Timing Diagram

$\overline{\text{SKIP}}$ Pin

The $\overline{\text{SKIP}}$ pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When $\overline{\text{SKIP}}$ is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When $\overline{\text{SKIP}}$ is high, the ZX comparator disables, and the converter enters FCCM mode. When both $\overline{\text{SKIP}}$ and PWM are tri-stated, normal operation forces the gate driver outputs low and the driver enters a very-low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When either $\overline{\text{SKIP}}$ is pulled low, the driver wakes up and is able to accept PWM pulses in less than 50µs.

Table 1 shows the logic functions of UVLO, PWM, $\overline{\text{SKIP}}$ DRVH and DRVL.

Table 1. Logic Functions of the TPS51604

UVLO	PWM	$\overline{\text{SKIP}}$	DRVL	DRVL	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High(1)	Low	DCM(1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	Low power
Inactive	—	Tri-state	Low	Low	Very Low power

(1) Until zero crossing protection occurs.

Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

Adaptive Deadtime Control and Shoot-Through Protection

The driver utilizes an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and maintain high efficiency. When the PWM input voltage becomes high, the low-side MOSFET gate voltage begins to fall after a propagation delay. At the same time, DRVL voltage is sensed, and high-side driving voltage starts to increase after DRVL voltage is lower than a proper threshold.

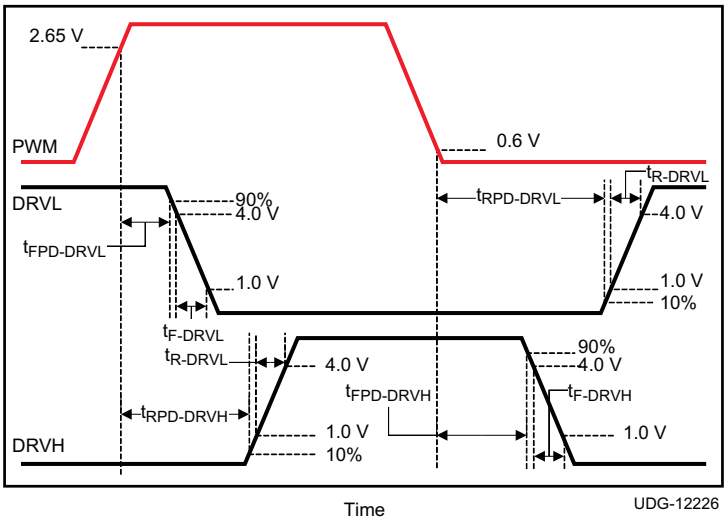


Figure 17. Rise/Fall Timing and Propagation Delay Definitions

Normal operation manages to near zero the dead-time between the low-side gate turn-off to high-side gate voltage turn-on and high-side gate turn-off to low-side gate turn-on in order to avoid simultaneous conduction of both MOSFETs as well as to reduce body diode conduction and recovery losses. This also reduces ringing on the leading edge of the SW waveform.

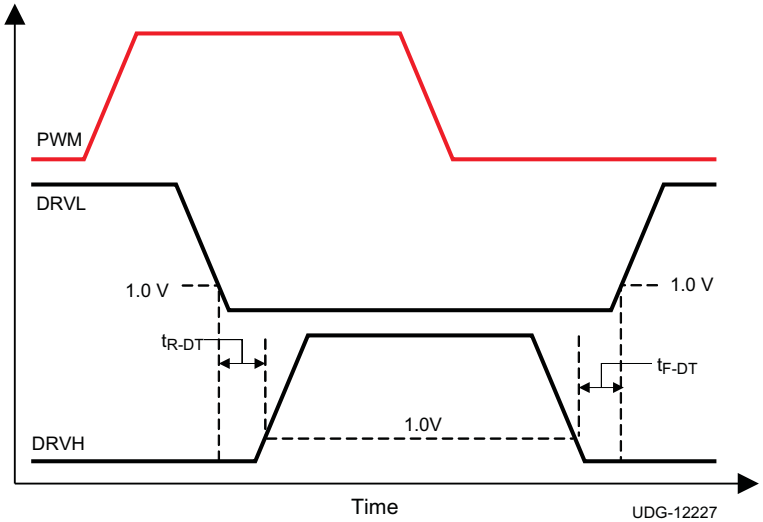


Figure 18. Dead-Time Definitions

Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BST pin is replaced by a FET which is gated by the DRVL signal.

Layout Guidelines

To improve the switching characteristics and design efficiency, these layout rules must be considered.

- Locate the driver as close as possible to the MOSFETs.
- Locate the VDD and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the switch-node as for the GND.
- Use wide traces for DRVH and DRVL closely following the related SW and GND traces. A width of between 80 and 100 mils is preferable where possible.
- Place the bypass capacitors as close as possible to the driver.
- Avoid PWM and enable traces going close to the SW and pad where high dV/dT voltage can induce significant noise into the relatively high impedance leads.

A poor layout can decrease the reliability of the entire system.

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Aligned package description throughout datasheet.	1
• Removed Ordering Information table.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51604DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1604	Samples
TPS51604DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1604	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

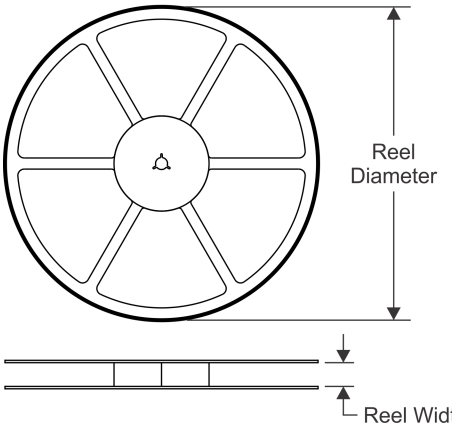
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

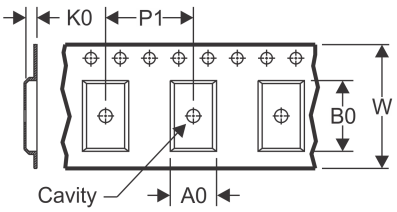
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

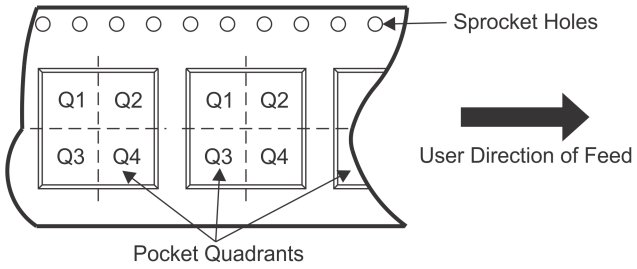


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

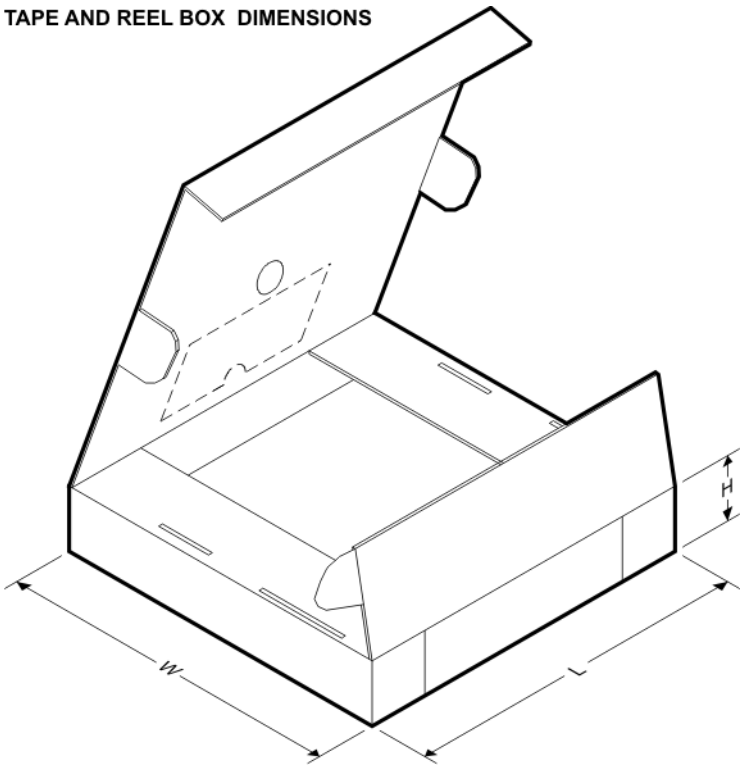
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51604DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51604DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

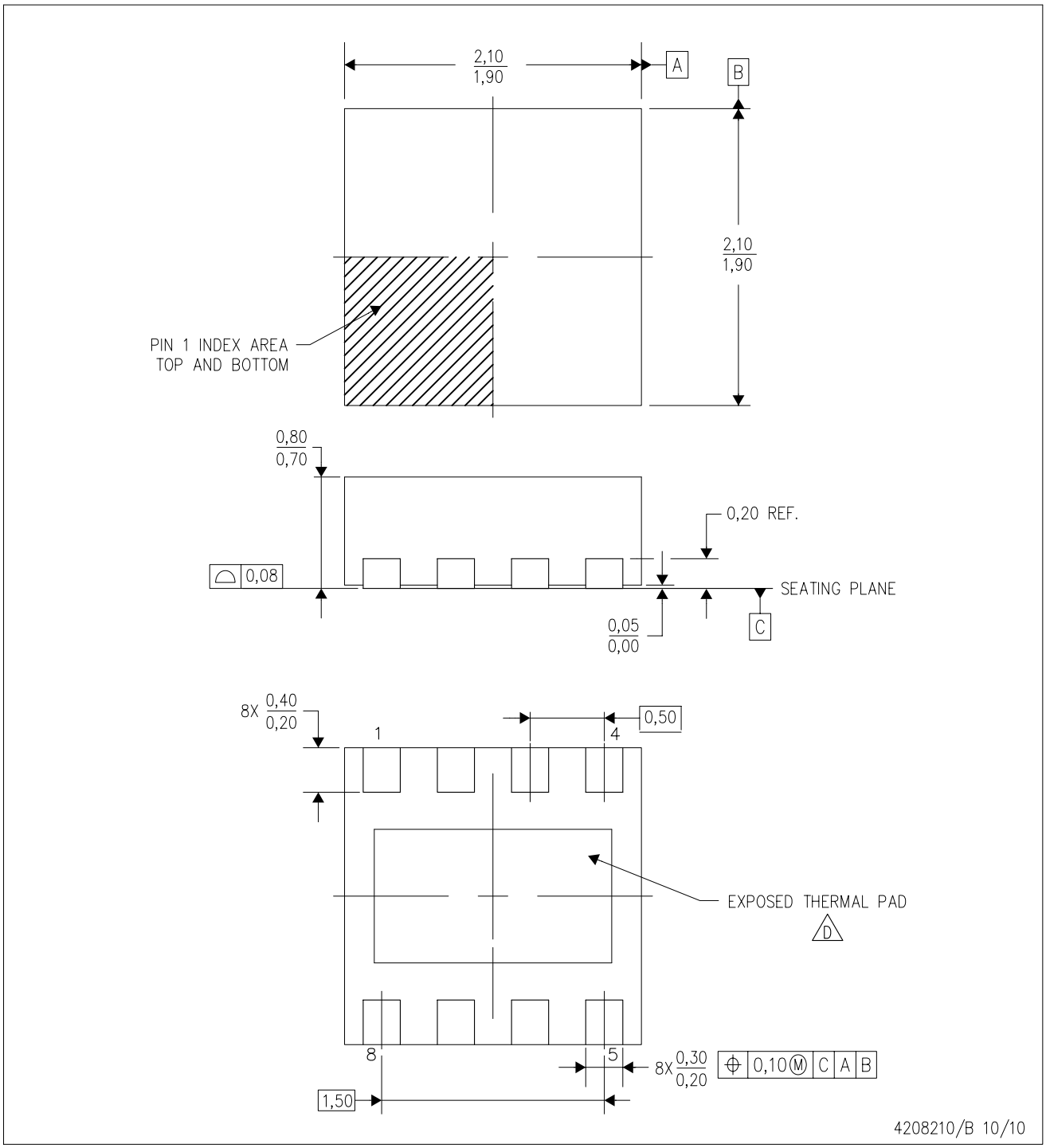
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51604DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS51604DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

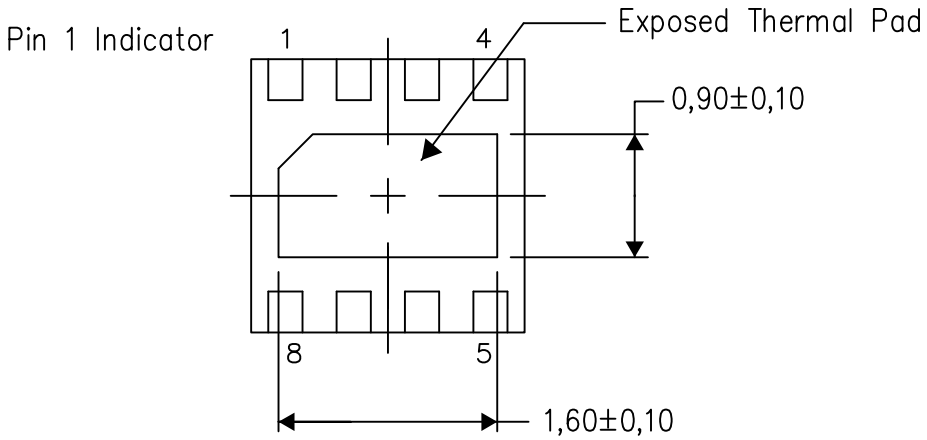
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



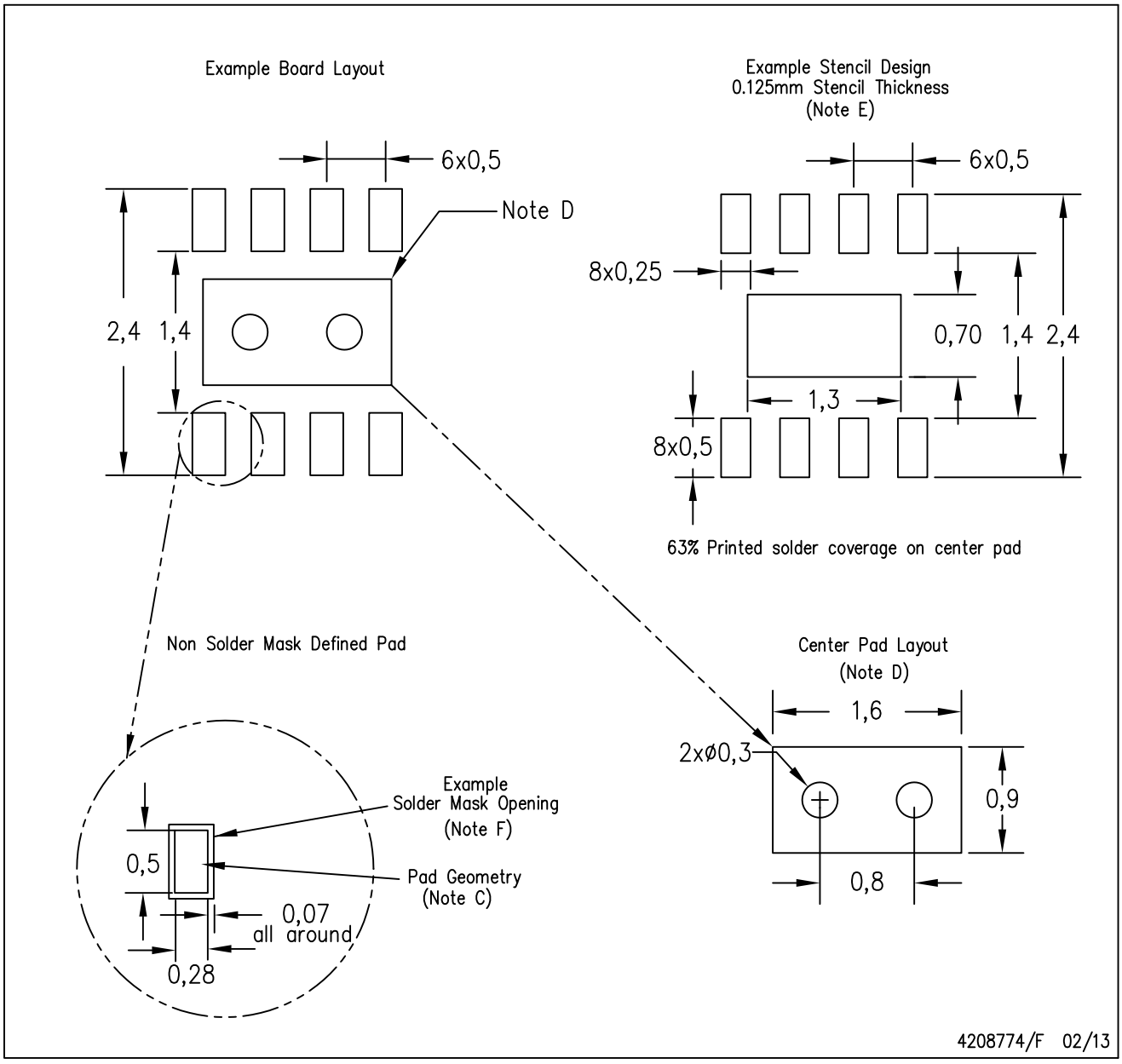
Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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