

CMOS Digital Integrated Circuit Silicon Monolithic

# TC358768AXBG/TC358778XBG

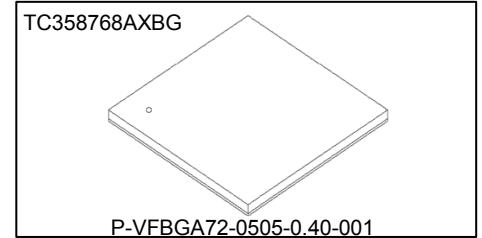
Mobile Peripheral Devices

## Overview

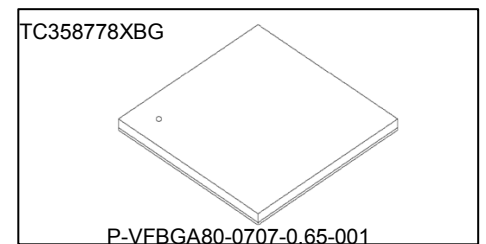
Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I<sup>2</sup>C or SPI.

### Features

- DSI-TX Interface
  - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
    - Support DSI Video Mode data transfer
    - DCS Command for panel register access
  - ✧ Supports up to 1 Gbps per data lane
  - ✧ Supports 1, 2, 3 or 4 data lanes
  - ✧ Supports video data formats
    - RGB888/666/565
- RGB Interface
  - ✧ Supports data formats
    - 24-bit data bus
      - RGB888/666/565 data formats
  - ✧ Up to 166 MHz input clock
  - ✧ Support VSYNC/HSYNC polarity option (default LOW)
  - ✧ Support DE polarity option (default High)
- I<sup>2</sup>C/SPI Slave Interface (Option to select either I<sup>2</sup>C or SPI interface)
  - ✧ I<sup>2</sup>C Interface (when CS=L)
    - Support for normal (100KHz), fast mode (400 kHz) and Special mode (1 MHz)
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
  - ✧ SPI interface (when CS=H)
    - SPI interface support for up to 25 MHz operation.
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
  - ✧ 2 GPIO signals
    - Two GPIO signals can be configured as SPI signals (SPI\_SS and SPI\_MISO)
    - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
  - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
  - ✧ Core and MIPI® D-PHY: 1.2V
  - ✧ I/O: 1.8V – 3.3V
- Typical Power Consumption
  - ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz ➔ 66.7 mW
  - ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz ➔ 91.4 mW
  - ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.



Weight: 32.0 mg (Typ.)



Weight: 66.1 mg (Typ.)

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**REFERENCES**

1. MIPI DSI, "mipi\_DSI\_specification\_v01-02-00, June 28, 2010"
2. MIPI DCS "DRAFT mipi\_DCS\_specification\_v01-02-00\_r0-02, December 2008"
3. MIPI D-PHY, "mipi\_D-PHY\_specification\_v01-00-00, May 14, 2009"
4. I<sup>2</sup>C bus specification, version 2.1, January 2000, Philips Semiconductor

## 1. Overview

The Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I<sup>2</sup>C or SPI.

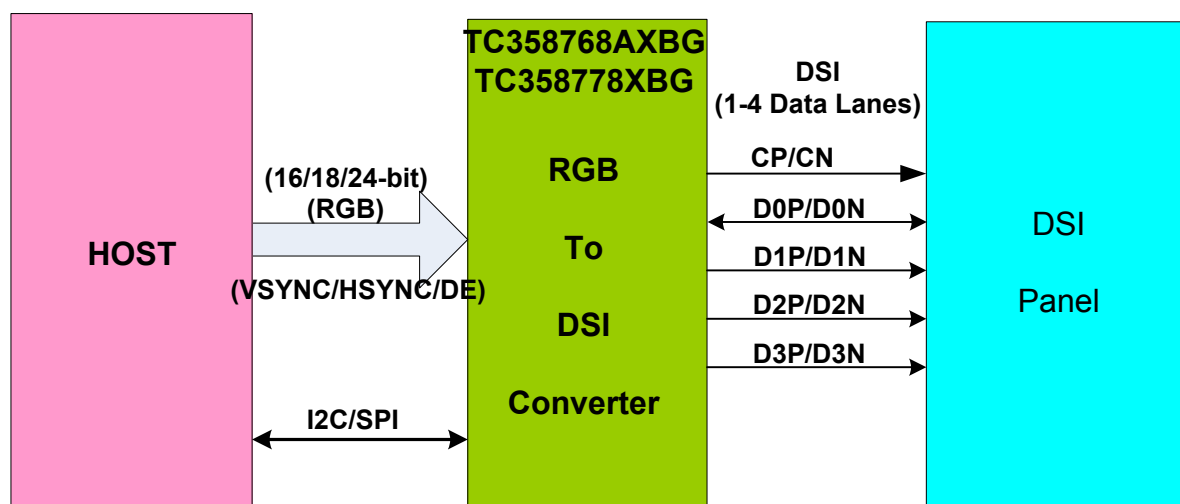


Figure 1.1 System Overview with TC358768AXBG/TC358778XBG in RGB to DSI-TX

## 2. Features

Below are the main features supported by TC358768AXBG/TC358778XBG.

- DSI-TX Interface
  - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
    - Support DSI Video Mode data transfer
    - DCS Command for panel register access
  - ✧ Supports up to 1 Gbps per data lane
  - ✧ Supports 1, 2, 3 or 4 data lanes
  - ✧ Supports video data formats
    - RGB888/666/565
- RGB Interface
  - ✧ Supports data formats
    - 24-bit data bus
      - RGB888/666/565 data formats
  - ✧ Up to 166 MHz input clock
  - ✧ Support VSYNC/HSYNC polarity option (default LOW)
  - ✧ Support DE polarity option (default High)
- I<sup>2</sup>C/SPI Slave Interface (Option to select either I<sup>2</sup>C or SPI interface)
  - ✧ I<sup>2</sup>C Interface (when CS=L)
    - Support for normal (100 kHz), fast mode (400 kHz) and Special mode (1 MHz)
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
  - ✧ SPI interface (when CS =H)
    - SPI interface support for up to 25 MHz operation.
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
  - ✧ 2 GPIO signals
    - Two GPIO signals can be configured as SPI signals (SPI\_SS and SPI\_MISO)
    - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
  - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
  - ✧ Core and MIPI® D-PHY: 1.2 V
  - ✧ I/O: 1.8 V to 3.3 V

- Typical Power Consumption

- ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz → 66.7 mW
- ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz → 91.4 mW

|                                | VDDC      | VDDIO     | VDDMIPI   | Total Power |    |
|--------------------------------|-----------|-----------|-----------|-------------|----|
|                                | 1.2 V     | 3.3 V     | 1.2 V     |             |    |
| 1080P Video                    | 42.8 mA   | 0.4 mA    | 32.3 mA   | 91.44       | mW |
|                                | 51.36 mW  | 1.32 mW   | 38.76 mW  |             |    |
| WXGA Video                     | 34.71 mA  | 0.167 mA  | 20.36 mA  | 66.64       | mW |
|                                | 41.652 mW | 0.551 mW  | 24.432 mW |             |    |
| Power Down<br>w/o PCLK, RefClk | 0.074 mA  | 0.025 mA  | 0.004 mA  | 176.1       | μW |
|                                | 0.089 mW  | 0.0825 mW | 0.0048 mW |             |    |

- ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.

### 3. External Pins

#### 3.1. TC358768AXBG pinout description

TC358768AXBG resides in BGA72 pin packages. The following table gives the signals of TC358768AXBG and their function.

**Table 3.1 TC358768AXBG Functional Signal List**

| Group                              | Pin Name            | I/O | Type | Function                                                                                                               | Note |
|------------------------------------|---------------------|-----|------|------------------------------------------------------------------------------------------------------------------------|------|
| System:<br>Reset &<br>Clock<br>(4) | RESX                | I   | Sch  | System reset input, active low                                                                                         |      |
|                                    | REFCLK              | I   | N    | Reference clock input (6MHz - 40MHz)                                                                                   |      |
|                                    | MSEL                | I   | N    | Mode Select<br>1'b0: Test mode<br>1'b1: Normal mode                                                                    |      |
|                                    | CS                  | I   | N    | Configuration Select<br>- When CS=L, enable I <sup>2</sup> C interface<br>- When CS=H, enable SPI interface            |      |
| MIPI-DSI<br>(10)                   | MIPI_CP             |     | PHY  | MIPI-DSI clock positive                                                                                                |      |
|                                    | MIPI_CN             |     | PHY  | MIPI-DSI clock negative                                                                                                |      |
|                                    | MIPI_D0P            |     | PHY  | MIPI-DSI Data 0 positive                                                                                               |      |
|                                    | MIPI_D0N            |     | PHY  | MIPI-DSI Data 0 negative                                                                                               |      |
|                                    | MIPI_D1P            |     | PHY  | MIPI-DSI Data 1 positive                                                                                               |      |
|                                    | MIPI_D1N            |     | PHY  | MIPI-DSI Data 1 negative                                                                                               |      |
|                                    | MIPI_D2P            |     | PHY  | MIPI-DSI Data 2 positive                                                                                               |      |
|                                    | MIPI_D2N            |     | PHY  | MIPI-DSI Data 2 negative                                                                                               |      |
|                                    | MIPI_D3P            |     | PHY  | MIPI-DSI Data 3 positive                                                                                               |      |
|                                    | MIPI_D3N            |     | PHY  | MIPI-DSI Data 3 negative                                                                                               |      |
| I2C<br>(2)                         | I2C_SCL             | OD  | Sch  | I <sup>2</sup> C serial clock or SPI_SCLK                                                                              | 4 mA |
|                                    | I2C_SDA             | OD  | Sch  | I <sup>2</sup> C serial data or SPI_MOSI                                                                               | 4 mA |
| Parallel<br>Port IF<br>(28)        | PD[23:0]            | I   | N    | Parallel Port Input Data<br>Note: PD[23:16] can be configure to be GPIO[10:3]                                          |      |
|                                    | VSYNC               | I   | N    | Parallel port VSYNC signal                                                                                             |      |
|                                    | HSYNC               | I   | N    | Parallel port HSYNC signal                                                                                             |      |
|                                    | DE                  | I   | N    | Parallel Port DE signal                                                                                                |      |
|                                    | PCLK                | I   | N    | Parallel Port Clock signal                                                                                             |      |
| GPIO<br>(2)                        | GPIO[2:1]           | I/O | N    | GPIO[2:1] signals<br>- (GPIO[1] option to become SPI_SS or INT signal)<br>- (GPIO[2] option to become SPI_MISO signal) | 4 mA |
| POWER<br>(9)                       | VDDC (1.2 V)        | NA  |      | VDD for Internal Core (3)                                                                                              |      |
|                                    | VDDIO (1.8 V-3.3 V) | NA  |      | VDDIO is for IO power supply (4)                                                                                       |      |
|                                    | VDD_MIPI (1.2 V)    | NA  |      | VDD for the MIPI (2)                                                                                                   |      |
| GROUND<br>(17)                     | VSS                 | NA  |      | Ground                                                                                                                 |      |

### 3.2. TC358768AXBG BGA72 Pin Count Summary

Table 3.2 TC358768AXBG BGA 72 Pin Count Summary

| Group Name       | Pin Count | Notes                   |
|------------------|-----------|-------------------------|
| SYSTEM           | 4         |                         |
| MIPI-DSI         | 10        |                         |
| I2C IF           | 2         |                         |
| GPIO             | 2         |                         |
| Parallel Port IF | 28        |                         |
| POWER            | 9         | IO, MIPI and Core Power |
| GROUND           | 17        |                         |
| <b>TOTAL</b>     | <b>72</b> |                         |

### 3.3. TC358778XBG pinout description

TC358778XBG resides in BGA80 pin packages. The following table gives the signals of TC358778XBG and their function.

**Table 3.3 TC358778XBG Functional Signal List**

| Group                              | Pin Name            | I/O | Type | Function                                                                                                              | Note |
|------------------------------------|---------------------|-----|------|-----------------------------------------------------------------------------------------------------------------------|------|
| System:<br>Reset &<br>Clock<br>(4) | RESX                | I   | Sch  | System reset input, active low                                                                                        |      |
|                                    | REFCLK              | I   | N    | Reference clock input (6MHz - 40MHz)                                                                                  |      |
|                                    | MSEL                | I   | N    | Mode Select<br>1'b0: Test mode<br>1'b1: Normal mode                                                                   |      |
|                                    | CS                  | I   | N    | Configuration Select<br>- When CS=L, enable I <sup>2</sup> C interface<br>- When CS=H, enable SPI interface           |      |
| MIPI-DSI<br>(10)                   | MIPI_CP             |     | PHY  | MIPI-DSI clock positive                                                                                               |      |
|                                    | MIPI_CN             |     | PHY  | MIPI-DSI clock negative                                                                                               |      |
|                                    | MIPI_D0P            |     | PHY  | MIPI-DSI Data 0 positive                                                                                              |      |
|                                    | MIPI_D0N            |     | PHY  | MIPI-DSI Data 0 negative                                                                                              |      |
|                                    | MIPI_D1P            |     | PHY  | MIPI-DSI Data 1 positive                                                                                              |      |
|                                    | MIPI_D1N            |     | PHY  | MIPI-DSI Data 1 negative                                                                                              |      |
|                                    | MIPI_D2P            |     | PHY  | MIPI-DSI Data 2positive                                                                                               |      |
|                                    | MIPI_D2N            |     | PHY  | MIPI-DSI Data 2negative                                                                                               |      |
|                                    | MIPI_D3P            |     | PHY  | MIPI-DSI Data 3positive                                                                                               |      |
|                                    | MIPI_D3N            |     | PHY  | MIPI-DSI Data 3 negative                                                                                              |      |
| I2C IF<br>(2)                      | I2C_SCL             | OD  | Sch  | I <sup>2</sup> C serial clock or SPI_SCLK                                                                             | 4 mA |
|                                    | I2C_SDA             | OD  | Sch  | I <sup>2</sup> C serial data or SPI_MOSI                                                                              | 4 mA |
| Parallel<br>Port IF<br>(28)        | PD[23:0]            | I   | N    | Parallel Port Input Data<br>Note: PD[23:16] can be configure to be GPIO[10:3]                                         |      |
|                                    | VSYNC               | I   | N    | Parallel port VSYNC signal                                                                                            |      |
|                                    | HSYNC               | I   | N    | Parallel port HSYNC signal                                                                                            |      |
|                                    | DE                  | I   | N    | Parallel Port DE signal                                                                                               |      |
|                                    | PCLK                | I   | N    | Parallel Port Clock signal                                                                                            |      |
| GPIO<br>(2)                        | GPIO[2:1]           | I/O | N    | GPIO[2:1] signals<br>- (GPIO[1] option to become SPI_SSor INT signal)<br>- (GPIO[2] option to become SPI_MISO signal) | 4 mA |
| POWER<br>(9)                       | VDDC (1.2V)         | NA  |      | VDD for Internal Core (3)                                                                                             |      |
|                                    | VDDIO (1.8V - 3.3V) | NA  |      | VDDIO is for IO power supply (4)                                                                                      |      |
|                                    | VDD_MIPI (1.2V)     | NA  |      | VDD for the MIPI (2)                                                                                                  |      |
| GROUND<br>(25)                     | VSS                 | NA  |      | Ground                                                                                                                |      |

### 3.4. TC358778XBG BGA80 Pin Count Summary

Table 3.4 TC358778XBG BGA 80 Pin Count Summary

| Group Name       | Pin Count | Notes                   |
|------------------|-----------|-------------------------|
| SYSTEM           | 4         |                         |
| MIPI-DSI         | 10        |                         |
| I2C IF           | 2         |                         |
| GPIO             | 2         |                         |
| Parallel Port IF | 28        |                         |
| POWER            | 9         | IO, MIPI and Core Power |
| GROUND           | 25        |                         |
| <b>TOTAL</b>     | <b>80</b> |                         |

### 3.5. TC358768AXBG Pin Layout

|                   |                   |                    |                   |                   |                    |                       |                       |                       |
|-------------------|-------------------|--------------------|-------------------|-------------------|--------------------|-----------------------|-----------------------|-----------------------|
| <b>A1</b><br>VSS  | <b>A2</b><br>PD17 | <b>A3</b><br>PD19  | <b>A4</b><br>PD21 | <b>A5</b><br>PD23 | <b>A6</b><br>GPIO2 | <b>A7</b><br>I2C_SCL  | <b>A8</b><br>MSEL     | <b>A9</b><br>VSS      |
| <b>B1</b><br>VDDC | <b>B2</b><br>PD16 | <b>B3</b><br>PD18  | <b>B4</b><br>PD20 | <b>B5</b><br>PD22 | <b>B6</b><br>GPIO1 | <b>B7</b><br>I2C_SDA  | <b>B8</b><br>RESX     | <b>B9</b><br>VDDIO    |
| <b>C1</b><br>PD15 | <b>C2</b><br>PD14 | <b>C3</b><br>VSS   | <b>C4</b><br>VSS  | <b>C5</b><br>VSS  | <b>C6</b><br>VSS   | <b>C7</b><br>VDD_MIPI | <b>C8</b><br>MIPI_D3P | <b>C9</b><br>MIPI_D3N |
| <b>D1</b><br>PD13 | <b>D2</b><br>PD12 | <b>D3</b><br>VSS   |                   |                   |                    | <b>D7</b><br>VSS      | <b>D8</b><br>MIPI_D2P | <b>D9</b><br>MIPI_D2N |
| <b>E1</b><br>VSS  | <b>E2</b><br>VSS  | <b>E3</b><br>VDDC  |                   |                   |                    | <b>E7</b><br>VDD_MIPI | <b>E8</b><br>MIPI_CP  | <b>E9</b><br>MIPI_CN  |
| <b>F1</b><br>VSS  | <b>F2</b><br>VSS  | <b>F3</b><br>VSS   |                   |                   |                    | <b>F7</b><br>VSS      | <b>F8</b><br>MIPI_D1P | <b>F9</b><br>MIPI_D1N |
| <b>G1</b><br>PD11 | <b>G2</b><br>PD10 | <b>G3</b><br>VDDIO | <b>G4</b><br>VSS  | <b>G5</b><br>VSS  | <b>G6</b><br>VDDIO | <b>G7</b><br>VDDIO    | <b>G8</b><br>MIPI_D0P | <b>G9</b><br>MIPI_D0N |
| <b>H1</b><br>VDDC | <b>H2</b><br>PD8  | <b>H3</b><br>PD6   | <b>H4</b><br>PD4  | <b>H5</b><br>PD2  | <b>H6</b><br>PD0   | <b>H7</b><br>PCLK     | <b>H8</b><br>DE       | <b>H9</b><br>CS       |
| <b>J1</b><br>VSS  | <b>J2</b><br>PD9  | <b>J3</b><br>PD7   | <b>J4</b><br>PD5  | <b>J5</b><br>PD3  | <b>J6</b><br>PD1   | <b>J7</b><br>REFCLK   | <b>J8</b><br>VSYNC    | <b>J9</b><br>HSYNC    |

**Figure 3.1 TC358768AXBG 72-Pin Layout (Top View)**

### 3.6. TC358778XBG Pin Layout

|       |      |      |      |       |        |      |         |          |          |
|-------|------|------|------|-------|--------|------|---------|----------|----------|
| A1    | A2   | A3   | A4   | A5    | A6     | A7   | A8      | A9       | A10      |
| VSS   | PD17 | PD19 | PD21 | PD23  | GPIO2  | VDDC | I2C_SCL | MSEL     | VSS      |
| B1    | B2   | B3   | B4   | B5    | B6     | B7   | B8      | B9       | B10      |
| VDDC  | PD16 | PD18 | PD20 | PD22  | GPIO1  | VSS  | I2C_SDA | RESX     | VDDIO    |
| C1    | C2   | C3   | C4   | C5    | C6     | C7   | C8      | C9       | C10      |
| PD15  | PD14 |      |      |       |        |      |         | MIPI_D3P | MIPI_D3N |
| D1    | D2   | D3   | D4   | D5    | D6     | D7   | D8      | D9       | D10      |
| PD13  | PD12 |      | VSS  | VSS   | VSS    | VSS  |         | MIPI_D2P | MIPI_D2N |
| E1    | E2   | E3   | E4   | E5    | E6     | E7   | E8      | E9       | E10      |
| PD11  | PD10 |      | VSS  | VSS   | VSS    | VSS  |         | VSS      | VDD_MIPI |
| F1    | F2   | F3   | F4   | F5    | F6     | F7   | F8      | F9       | F10      |
| PD9   | PD8  |      | VSS  | VSS   | VSS    | VSS  |         | MIPI_CP  | MIPI_CN  |
| G1    | G2   | G3   | G4   | G5    | G6     | G7   | G8      | G9       | G10      |
| PD7   | PD6  |      | VSS  | VSS   | VSS    | VSS  |         | MIPI_D1P | MIPI_D1N |
| H1    | H2   | H3   | H4   | H5    | H6     | H7   | H8      | H9       | H10      |
| VDDIO | VSS  |      |      |       |        |      |         | VSS      | VDD_MIPI |
| J1    | J2   | J3   | J4   | J5    | J6     | J7   | J8      | J9       | J10      |
| PD4   | PD2  | PD0  | VSS  | VSS   | PCLK   | DE   | CS      | MIPI_D0P | MIPI_D0N |
| K1    | K2   | K3   | K4   | K5    | K6     | K7   | K8      | K9       | K10      |
| PD5   | PD3  | PD1  | VDDC | VDDIO | REFCLK | VSYN | HSYN    | VDDIO    | VSS      |

Figure 3.2 TC358778XBG 80-Pin Layout (Top View)

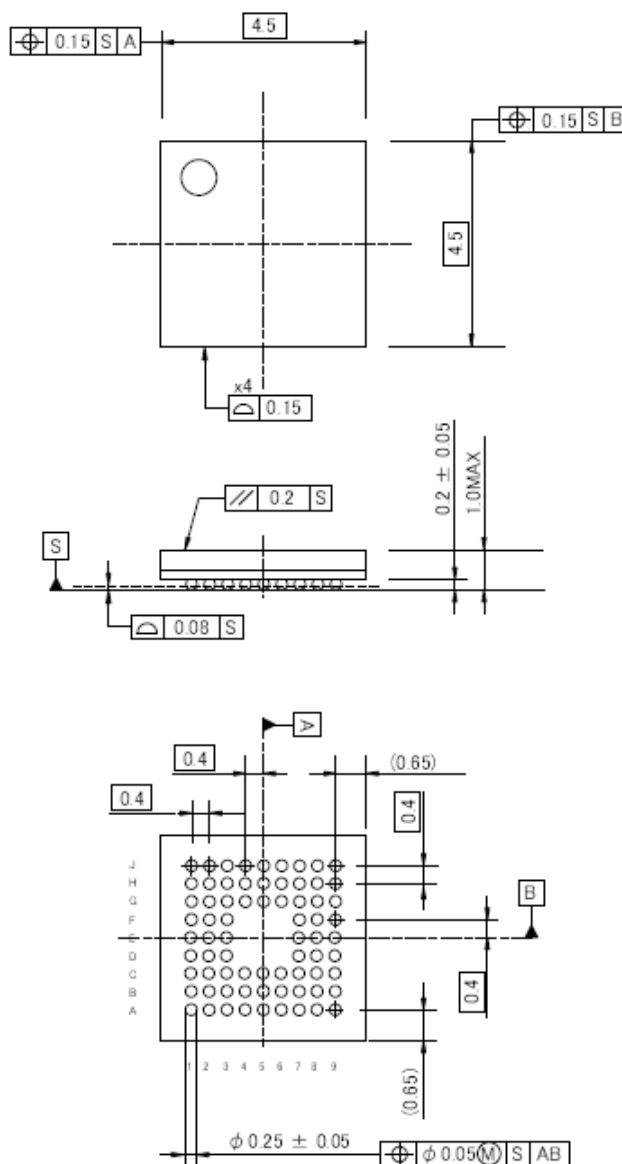
## 4. Package

### 4.1. TC358768AXBG Package

The packages for TC358768AXBG is described in the figure below.

P-VFBGA72-0505-0.40-001

"Unit:mm"



Weight: 32.0 mg (Typ.)

Figure 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 package

Table 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 Mechanical Dimension

| Dimension          | Min     | Typ.                      | Max     |
|--------------------|---------|---------------------------|---------|
| Solder ball pitch  | -       | 0.4 mm                    | -       |
| Solder ball height | 0.15 mm | 0.2 mm                    | 0.25 mm |
| Package dimension  | -       | 4.5 × 4.5 mm <sup>2</sup> | -       |
| Package height     | -       | -                         | 1.0 mm  |

## 4.2. TC358778XBG Package

The package for TC358778XBG is described in the figure below.

P-VFBGA80-0707-0.65-001

"Unit:mm"

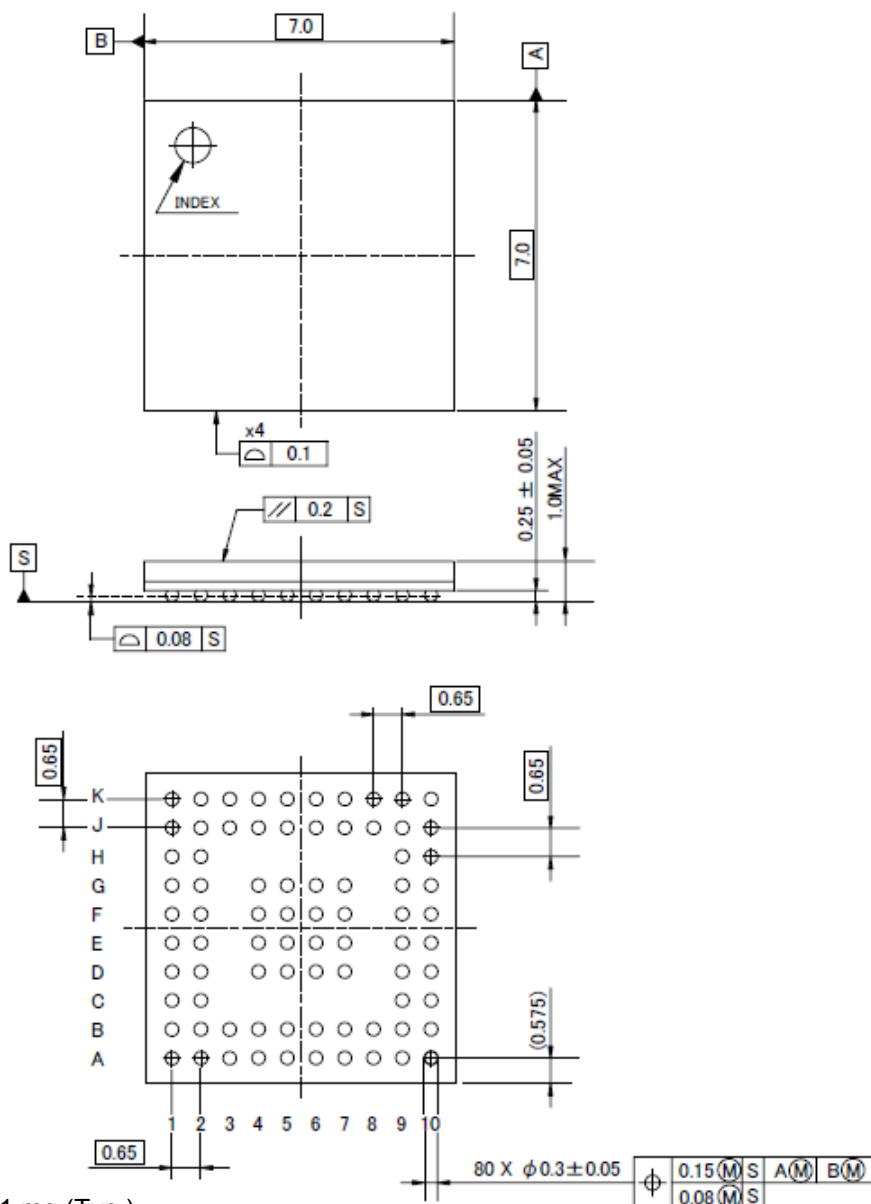


Figure 4.2 TC358778XB P-VFBGA80-0707-0.65-001 package

Table 4.2 P-VFBGA80-0707-0.65-001 Mechanical Dimension

| Dimension          | Min     | Typ.                      | Max     |
|--------------------|---------|---------------------------|---------|
| Solder ball pitch  | -       | 0.65 mm                   | -       |
| Solder ball height | 0.20 mm | 0.25 mm                   | 0.30 mm |
| Package dimension  | -       | 7.0 × 7.0 mm <sup>2</sup> | -       |
| Package height     | -       | -                         | 1.0 mm  |

## 5. Electrical Characteristics

### 5.1. Absolute Maximum Ratings

VSS= 0V reference

| Parameter                            | Symbol               | Rating               | Unit |
|--------------------------------------|----------------------|----------------------|------|
| Supply voltage (1.8V - Digital IO)   | VDDIO                | -0.3 to +3.9         | V    |
| Supply voltage (1.2V - Digital Core) | VDDC                 | -0.3 to +1.8         | V    |
| Supply voltage (1.2V - MIPI PHY)     | VDD_MIPI             | -0.3 to +1.8         | V    |
| Input voltage (DSI IO)               | V <sub>IN_DSI</sub>  | -0.3 to VDD_MIPI+0.3 | V    |
| Output voltage (DSI IO)              | V <sub>OUT_DSI</sub> | -0.3 to VDD_MIPI+0.3 | V    |
| Input voltage (Digital IO)           | V <sub>IN_IO</sub>   | -0.3 to VDDIO+0.3    | V    |
| Output voltage (Digital IO)          | V <sub>OUT_IO</sub>  | -0.3 to VDDIO+0.3    | V    |
| Junction temperature                 | T <sub>j</sub>       | 125                  | °C   |
| Storage temperature                  | T <sub>stg</sub>     | -40 to +125          | °C   |

### 5.2. Operating Condition

VSS= 0 V reference

| Parameter                                                        | Symbol          | Min  | Typ. | Max  | Unit             |
|------------------------------------------------------------------|-----------------|------|------|------|------------------|
| Supply voltage (1.8V - Digital IO)                               | VDDIO           | 1.65 | 1.8  | 1.95 | V                |
| Supply voltage (3.3V - Digital IO)                               | VDDIO           | 3.0  | 3.3  | 3.6  | V                |
| Supply voltage (1.2V - Digital Core)                             | VDDC            | 1.1  | 1.2  | 1.3  | V                |
| Supply voltage (1.2V - MIPI PHY)                                 | VDD_MIPI        | 1.1  | 1.2  | 1.3  | V                |
| Operating temperature (ambient temperature with voltage applied) | T <sub>a</sub>  | -30  | +25  | +85  | °C               |
| Supply Noise Voltage                                             | V <sub>SN</sub> | -    | -    | 100  | mV <sub>pp</sub> |

### 5.3. DC Electrical Specification

| Parameter                                                                                                     | Symbol                      | Min       | Typ. | Max       | Unit    |
|---------------------------------------------------------------------------------------------------------------|-----------------------------|-----------|------|-----------|---------|
| Input voltage, High level input <sup>Note1</sup>                                                              | $V_{IH}$                    | 0.7 VDDIO | -    | VDDIO     | V       |
| Input voltage, Low level input <sup>Note1</sup>                                                               | $V_{IL}$                    | 0         | -    | 0.3 VDDIO | V       |
| Input voltage High level<br>CMOS Schmitt Trigger <sup>Note1,2</sup>                                           | $V_{IHS}$                   | 0.7 VDDIO | -    | VDDIO     | V       |
| Input voltage Low level<br>CMOS Schmitt Trigger <sup>Note1,2</sup>                                            | $V_{ILS}$                   | 0         | -    | 0.3 VDDIO | V       |
| Output voltage High level <sup>Note1, Note2</sup><br>(Condition: $I_{OH} = -0.4$ mA)                          | $V_{OH}$                    | 0.8 VDDIO | -    | VDDIO     | V       |
| Output voltage Low level <sup>Note1, Note2</sup><br>(Condition: $I_{OL} = 2$ mA)                              | $V_{OL}$                    | 0         | -    | 0.2 VDDIO | V       |
| Input leak current, High level (Normal IO or<br>Pull-up IO)<br>(Condition: $V_{IN} = +VDDIO$ , VDDIO = 3.6 V) | $I_{ILH1}$ <sup>Note3</sup> | -10       | -    | 10        | $\mu A$ |
| Input leak current, High level (Pull-down<br>IO)<br>(Condition: $V_{IN} = +VDDIO$ , VDDIO = 3.6 V)            | $I_{ILH2}$ <sup>Note3</sup> | -         | -    | 100       | $\mu A$ |
| Input leak current, Low level (Normal IO or<br>Pull-down IO)<br>(Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)    | $I_{ILL1}$ <sup>Note4</sup> | -10       | -    | 10        | $\mu A$ |
| Input leak current, Low level (Pull-up IO)<br>(Condition: $V_{IN} = 0$ V, VDDIO = 3.6 V)                      | $I_{ILL2}$ <sup>Note4</sup> | -         | -    | 200       | $\mu A$ |

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to  $V_{in}$  (input voltage)

Note 4: Normal pin or Pull-down IO pin applied VSSIO (0V) to  $V_{in}$  (input voltage)

## 6. Revision History

Table 6.1 Revision History

| Revision | Date       | Description    |
|----------|------------|----------------|
| 1.11     | 2014-05-28 | Newly released |

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