STi7101

Low-cost HDTV set-top box decoder for H.264

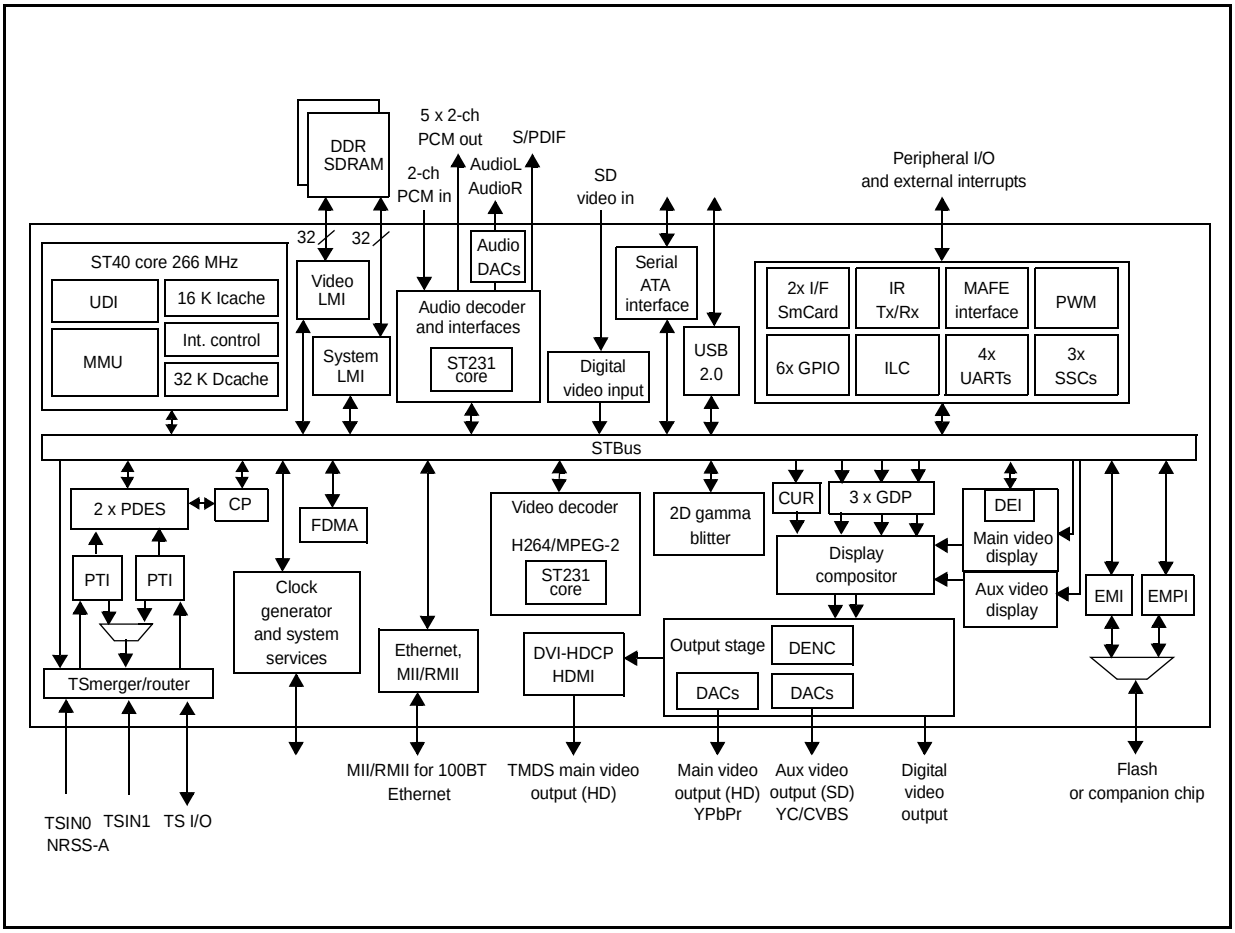
Data Brief

Features

- H.264 support
- Linux®, Windows® CE and OS21 compatible ST40 CPU core: 266 MHz
- Transport filtering and descrambling
- Video decoder: H.264 (MPEG-4 part 10) and MPEG-2
- SVP compliant
- Windows Media™ DRM support

Description

The STi7101 is a new generation, high-definition set-top box / DVD decoder chip, that provides very high performance for low-cost HD systems. The STi7101 includes both MPEG2 and H.264 video decoders.



1 Full feature list

- H.264 support
- Linux®, Windows® CE and OS21 compatible ST40 CPU core: 266 MHz
- Transport filtering and descrambling
- Video decoder: H.264 (MPEG-4 part 10) and MPEG-2
- SVP compliant
- Windows Media™ DRM support
- Graphics engine and dual display: standard and high-definition
- Audio decoder: including Windows Media™ Audio 9 (WMA-9) and WMA-9 Pro
- DVD data retrieval and decryption

1.1 Embedded interfaces

- USB 2.0 host controller/PHY interface
- DVI/HDMI™ output
- Digital audio and video auxiliary inputs
- Low-cost modem
- 100BT Ethernet controller with integrated MAC and MII/RMII interface for external PHY
- Serial ATA (SATA)

1.2 Processor subsystem

- ST40 32-bit superscaler RISC CPU
  - 266 MHz, 2-way set associative 16 Kbyte ICache, 32 Kbyte DCache, MMU
  - Five-stage pipeline, delayed branch support
  - Floating point unit, matrix operation support
  - Debug port, interrupt controller

1.3 Transport subsystem

- TS merger/router
  - Two serial/parallel inputs
  - One bidirectional interface
  - Merging of three external transport streams
  - Transport streams from memory support
  - NRSS-A module interface
  - TS routing for DVB-CI and CableCARD™ modules

- Programmable transport interfaces (PTIs)
  - Two programmable transport interfaces
  - Two transport stream demultiplexers: DVB, DIRECTV®, ATSC, ARIB, OpenCable, DCII
  - Integrated DES, AES, DVB and Multi2 descramblers
  - NDS random access scrambled stream protocol (RASP) compliant
  - NDS ICAM CA
  - Support for VGS, Passage and DVS042 residue handling

1.4 Video/graphics subsystem

- H.264(MPEG-4 part 10) main and high profile level 4.1/MPEG-2 MP@HL video decoder
  - Advanced error concealment and trick mode support
  - Dual MPEG-2 MP@HL decode
- SD digital video input
- Displays
  - One HD display multi format capable (1080I, 720P, 480P/576P, 480I/576I)
    - Analog HD output RGB or YPbPr
    - HDMI encoded output
  - One standard-definition display: Analog SD output: YPbPr or YC and CVBS
- Gamma 2D graphics processor
  - Triple-source, 2D gamma blitter engine
  - Alpha blending and logical operations
  - Color space and format conversion
  - Fast color fill
  - Arbitrary resizing with high quality filters
  - Acceleration of direct drawing by CPU
- Gamma compositor and video processor
  - 7-channel mixer for high definition output
  - Independent 2-channel mixer for SD output
  - Three graphic display planes
  - High quality video scaler
  - Motion and detail adaptive deinterlacer
  - Linear resizing and format conversions
  - Horizontal and vertical filtering
- Copy protection
  - HDMI/HDCP copy protection hardware
  - SVP compliant
  - Macrovision® copy protection for 480I, 480P, 576I, 576P outputs
  - DTCP-IP
  - AWG-based DCS analog copy protection

1.5 Audio subsystem

- Digital audio decoder
  - Support for all the most popular audio standards including WMA-9, WMA-9 Pro, MPEG-1 layer I/II, MPEG-2 layer II, MPEG-2 AAC, MPEG-4 AAC LC 2-channel/5.1 channel, MPEG-4 AAC+SBR 2-channel/5.1 channel, Dolby® Digital EX, Pro Logic® II, MLP™ and DTS®
  - PCM mixing with internal or external source, and sample rate conversion
  - 6- to 2-channel downmixing
  - PCM audio input
  - Independent, multichannel, PCM output, S/PDIF output and analog output
- Stereo 24-bit audio DAC for analog output
- IEC958/IEC1937 digital audio output interface (S/PDIF)
- CSS/CPxM copy protection hardware

1.6 Interfaces

- External memory interface (EMI)
  - 16-bit interface supporting ROM, Flash, SFlash, SRAM, peripherals
  - Access in five banks
  - High speed synchronous mode for interconnecting two STi7101 devices
- External microprocessor interface (EMPI)
  - 32-bit MPX satellite, target-only interface
  - Synchronous operation at MPX clock speed, capable of 100 MHz
- Dual local memory interface (LMI)
  - Dual interface (2 x 32-bit) for DDR1 200-MHz (DDR400) memories, supports 128-, 256-, 512-Mbit, and 1-Gbit devices
- USB 2.0 host controller/PHY interface
- Serial ATA hard-disk drive support
  - Record and playback with trick modes
  - Pause and time shifting, watch and record
- 100BT Ethernet controller, MAC and MII/RMII
- On-chip peripherals
  - Four ASCs (UARTs) with Tx and Rx FIFOS, two of which can be used in smartcard interfaces
  - Two smartcard interfaces and clock generators (improved to reduce external circuitry)
  - Three SSCs for I²C/SPI master slaves interfaces
  - Serial communications interface (SCIF)
  - Two PWM outputs
  - Teletext serializer and DMA module
  - Six banks of general purpose I/O, 3.3 V tolerant
  - SiLabs line-side (DAA) interface
  - Modem analog front end (MAFE) interface

- Infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes
- UHF remote receiver input interface
- Interrupt level controller and external interrupts, 3.3 V tolerant
- Low power/RTC/watchdog controller
- Integrated VCXO
- DiSEqC 2.0 interface
- PWM capture/compare functions
- Flexible multi-channel DMA (FDMA)

1.7 Services and package

- JTAG/TAP interface, ST40 toolset support, ST231 toolset support
- Package: 35 x 35 PBGA, 580 + 100 balls (ECOPACK® package).

2 Applications overview

Figure 1. Low-cost satellite HD set-top box

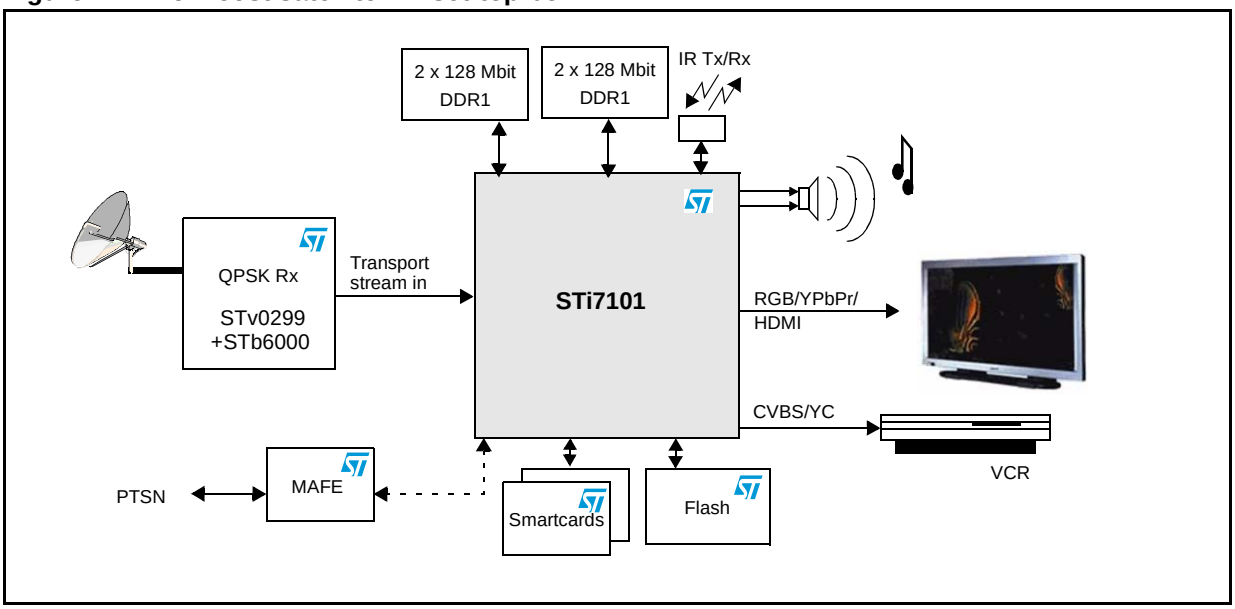


Figure 2. Low-cost cable HD set-top box with return channel

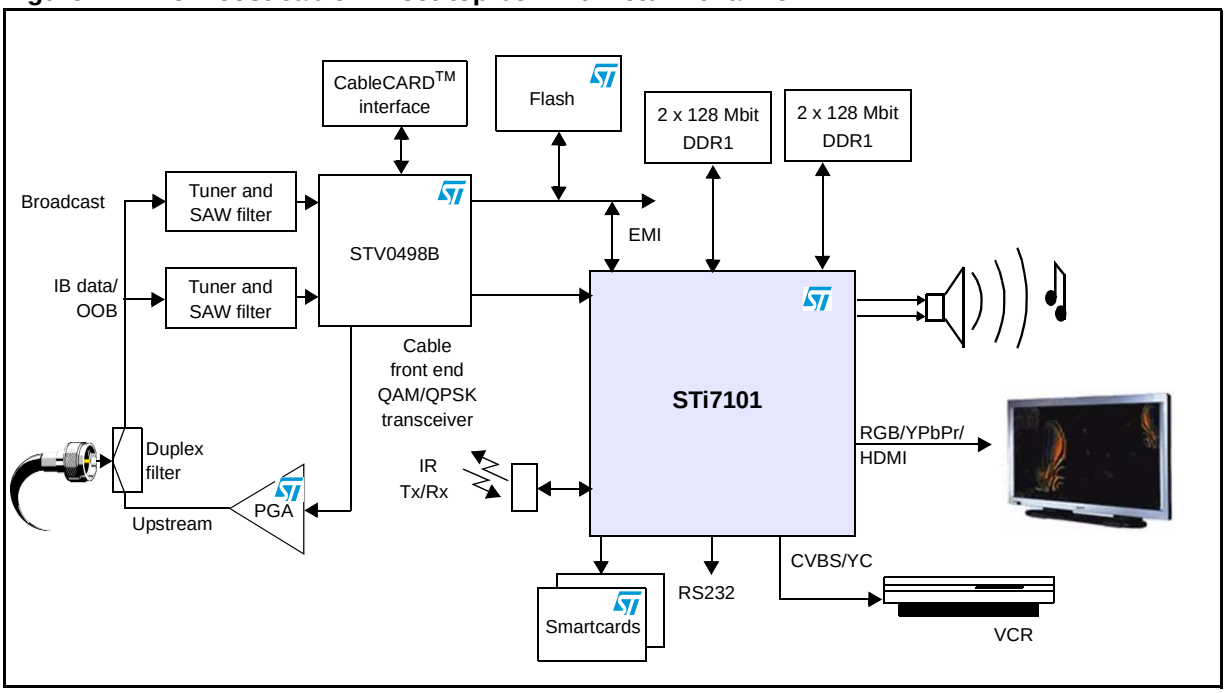


Figure 3. Low-cost dual satellite and terrestrial HD set-top box with HDD and DVD

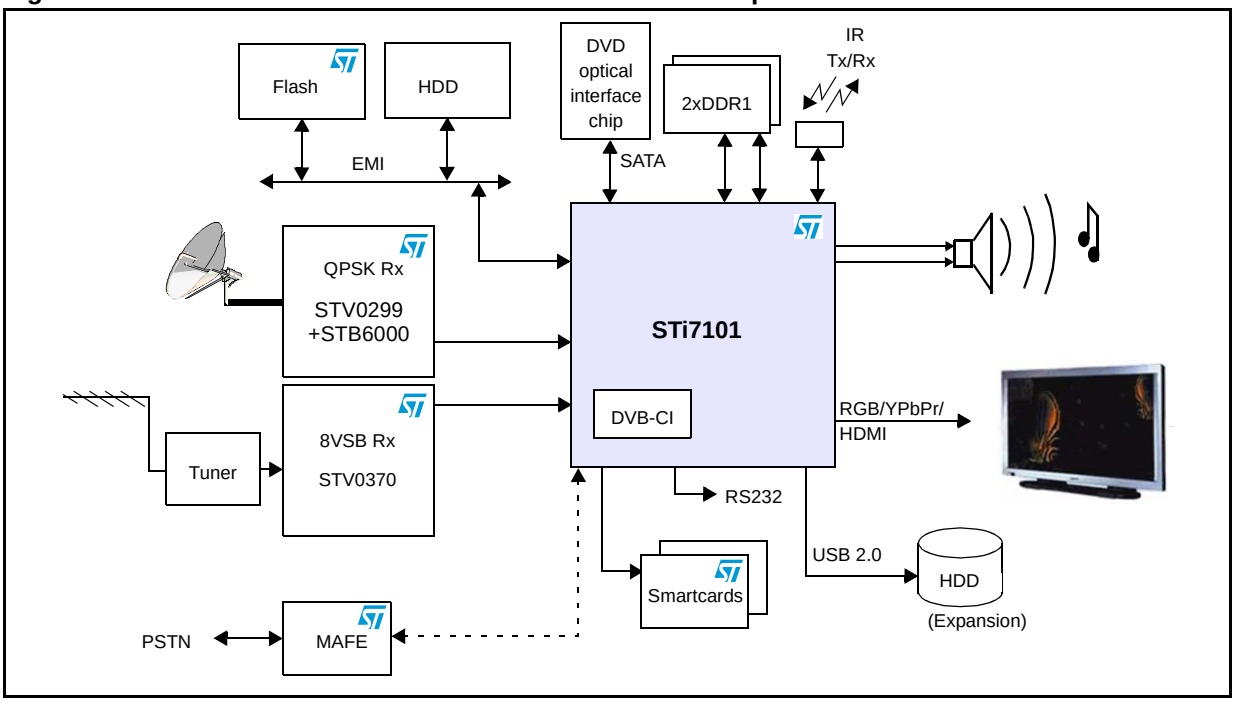
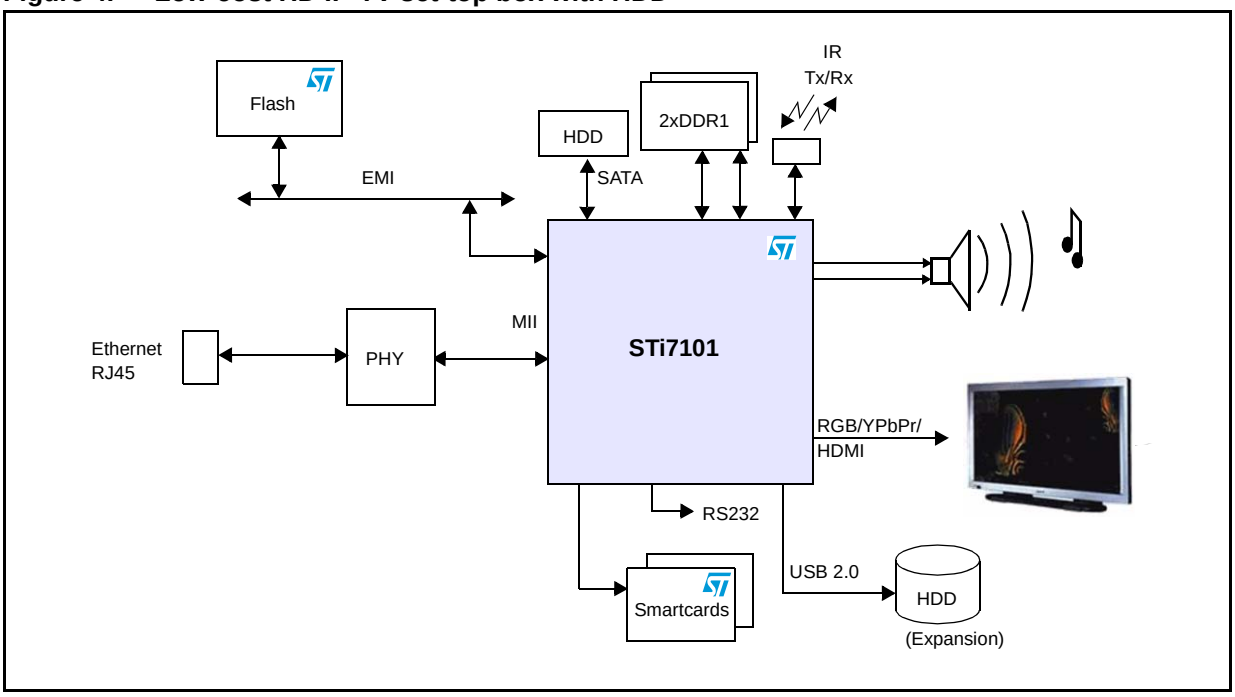


Figure 4. Low-cost HD IP-TV set-top box with HDD



3 Revision history

Table 1. Document revision history

Date	Revision	Changes
02-Sep-2008	1	Initial release
11-Sept-2008	2	Change on package

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