

ALM-11336

1850 MHz – 1980 MHz

Low Noise, High Linearity Amplifier Module
with Fail-Safe Bypass Feature



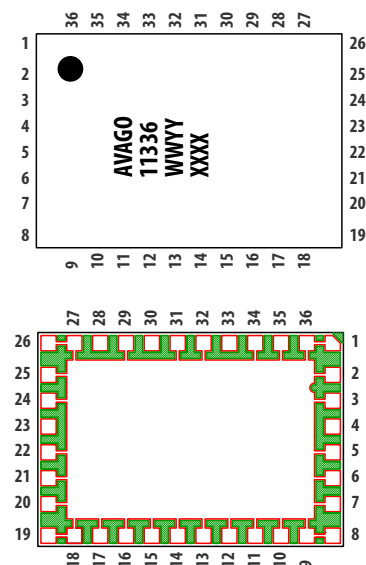
Data Sheet

Description

Avago Technologies' ALM-11336 is an easy-to-use GaAs MMIC Tower Mount Amplifier (TMA) LNA Module with low IL bypass path. The module has low noise and high linearity achieved through the use of Avago Technologies' proprietary 0.25 μm GaAs Enhancement-mode pHEMT process. All matching components are fully integrated within the module and the 50 ohm RF input and output pins are already internally AC-coupled. This makes the ALM-11336 extremely easy to use as the only external parts are DC supply bypass capacitors. For optimum performance at other bands, ALM-11036 (776-870 MHz), ALM-11136 (870-915 MHz) and ALM-11236 (1710-1850) are recommended. All ALM-11x36 share the same package and pin out configuration.

Pin Configuration and Package Marking

7.0 x 10.0 x 1.5 mm³ 36-lead MCOB



Pin	Connection
4	RF_IN
23	RF_OUT
28	EXT_P2
30	EXT_P1
33	Vdd
Others	GND

Note:
Package marking provides orientation and identification
"11336" = Device Part Number
"WWYY" = Work week and Year of manufacture
"XXXX" = Last 4 digit of Lot number

Features

- Very Low Noise Figure
- Low Bypass IL
- Good Return Loss
- Fail-safe Bypass mode
- High linearity performance
- High isolation @LNA mode
- Flat gain
- GaAs E-pHEMT Technology
- Single 5 V power supply
- Compact MCOB package 7.0 x 10.0 x 1.5 mm³
- MSL2a

Specifications

1980 MHz; 5 V, 100 mA (Typical)

- 15.3 dB Gain
- ≥ 18 dB RL
- 0.72 dB Noise Figure
- 17.9 dBm IIP3
- 3.8 dBm Input Power at 1dB gain compression
- 0.78 dB Bypass IL
- ≥ 18 dB Bypass RL
- ≥ 50 dB isolation @LNA mode

Applications

- Tower Mount Amplifier (TMA)
- Cellular Infrastructure



Attention: Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model = 300 V

ESD Human Body Model = 2000 V

Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

Absolute Maximum Rating ^[1] $T_A = 25^\circ\text{C}$

Symbol	Parameter	Units	Absolute Max.
V_{dd}	Device Voltage, RF output to ground	V	5.5
$P_{in,max}$	CW RF Input Power ($V_{dd} = 5.0\text{ V}$, $I_{dd} = 100\text{ mA}$)	dBm	+15
P_{diss}	Total Power Dissipation ^[3]	W	0.715
T_j	Junction Temperature	$^\circ\text{C}$	150
T_{STG}	Storage Temperature	$^\circ\text{C}$	-65 to 150

Thermal Resistance ^[2]

($V_{dd} = 5.0\text{ V}$, $I_{dd} = 100\text{ mA}$) $\theta_{jc} = 56.2^\circ\text{C/W}$

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. Power dissipation with unit turned on. Board temperature T_c is 25°C . Derate at $17.8\text{ mW}/^\circ\text{C}$ for $T_c > 109.8^\circ\text{C}$.

Electrical Specifications^[1, 4]

RF performance at $T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{ V}$, 1980 MHz, measured on demo board in Figure 1 with component listed in Table 1 for DC bypass.

Symbol	Parameter and Test Condition	Frequency (MHz)	Units	Min.	Typ.	Max.
I_{dd}	Drain Current		mA	81	100	117
Gain	Gain	1850 1910 1980	dB	– – 13.8	15.6 15.4 15.3	– – 16.8
IRL	Input Return Loss, 50 Ω source		dB	–	23	–
ORL	Output Return Loss, 50 Ω load		dB	–	28	–
NF ^[2]	Noise Figure	1850 1910 1980	dB	– – –	0.72 0.72 0.72	– – 0.9
IIP3 ^[3]	Input Third Order Intercept Point		dBm	14	17.9	–
IP1dB	Input Power at 1 dB Gain Compression		dBm	2.85	3.8	–
Bypass IL	Bypass Insertion Loss, 50 Ω load $V_{dd} = 0\text{ V}$	1980	dB	–	0.78	1.1
Bypass IRL	Input Return Loss, 50 Ω source $V_{dd} = 0\text{ V}$		dB	–	23	–
Bypass ORL	Output Return Loss, 50 Ω load $V_{dd} = 0\text{ V}$		dB	–	23	–
ISOL	Bypass Isolation @LNA ON $V_{dd} = 5\text{ V}$		dB	–	65	–

Notes:

1. Measurements at 1980 MHz obtained using demo board described in Figure 1.
2. For NF data, board losses of the input have not been de-embedded.
3. IIP3 test condition: $F_{RF1} = 1980\text{ MHz}$, $F_{RF2} = 1981\text{ MHz}$ with input power of -15 dBm per tone.
4. Use proper bias, heatsink and derating to ensure maximum channel temperature is not exceeded. See absolute maximum ratings and application note for more details.

Product Consistency Distribution Charts^[1, 2]

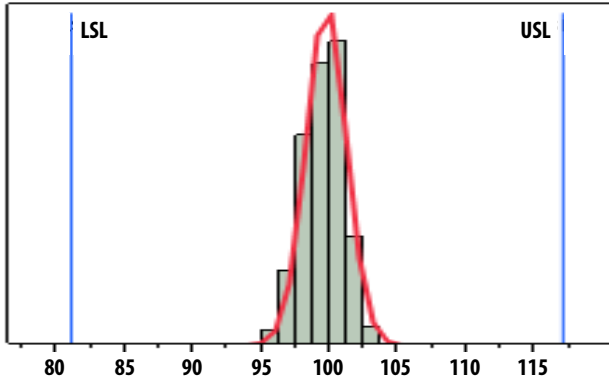


Figure 1. Idd, LSL = 81 mA, nominal = 100 mA, USL = 117 mA

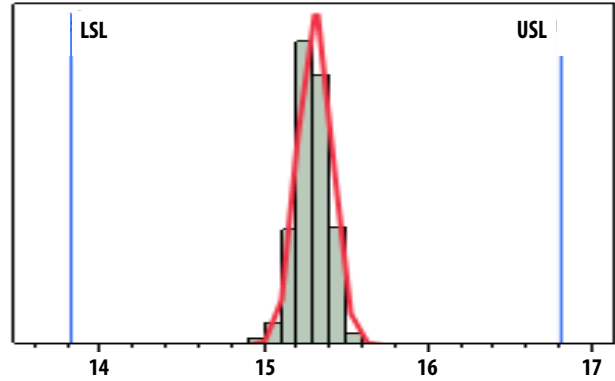


Figure 2. Gain, LSL = 13.8 dB, nominal = 15.3 dB, USL = 16.8 dB

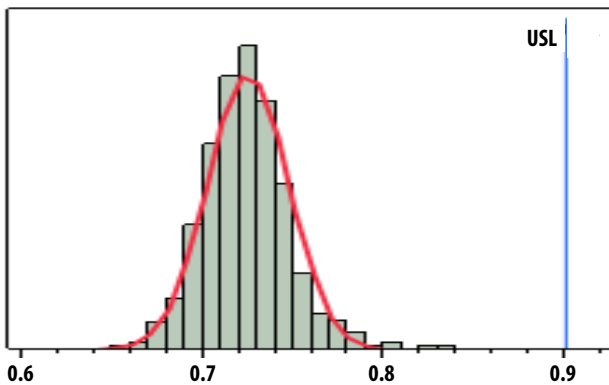


Figure 3. NF, nominal = 0.72 dB, USL = 0.9 dB

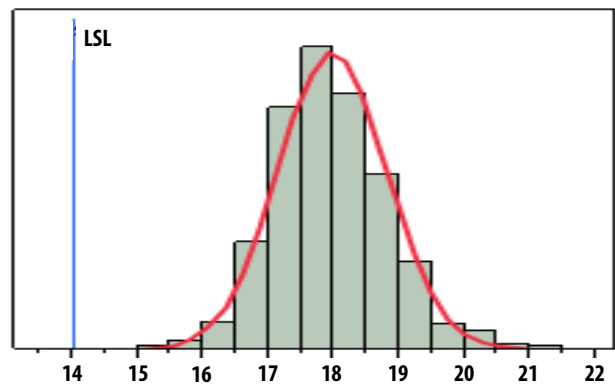


Figure 4. IIP3, LSL = 14 dBm, nominal = 17.9 dBm

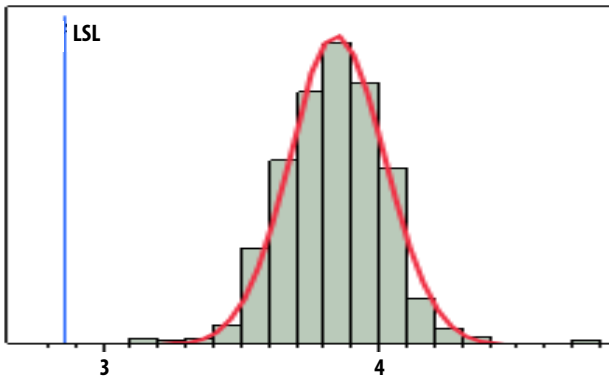


Figure 5. IP1dB, LSL = 2.85 dBm, nominal = 3.8 dBm

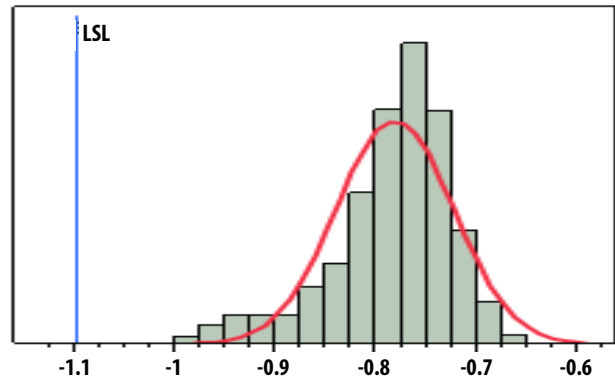


Figure 6. Bypass IL, LSL = 1.1 dB, nominal = 0.78 dB

Notes:

1. Distribution data sample size is 1500 samples taken from 3 different wafer lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
2. Circuit trace losses have not been de-embedded from measurements above.

Demo Board Layout

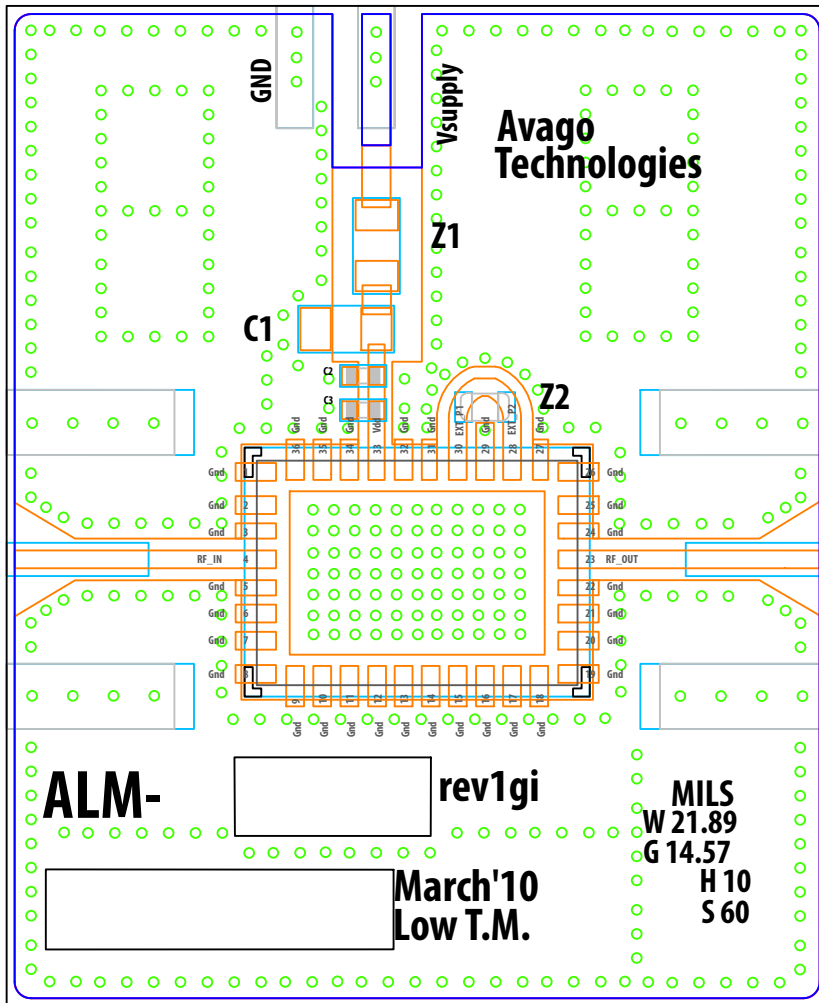
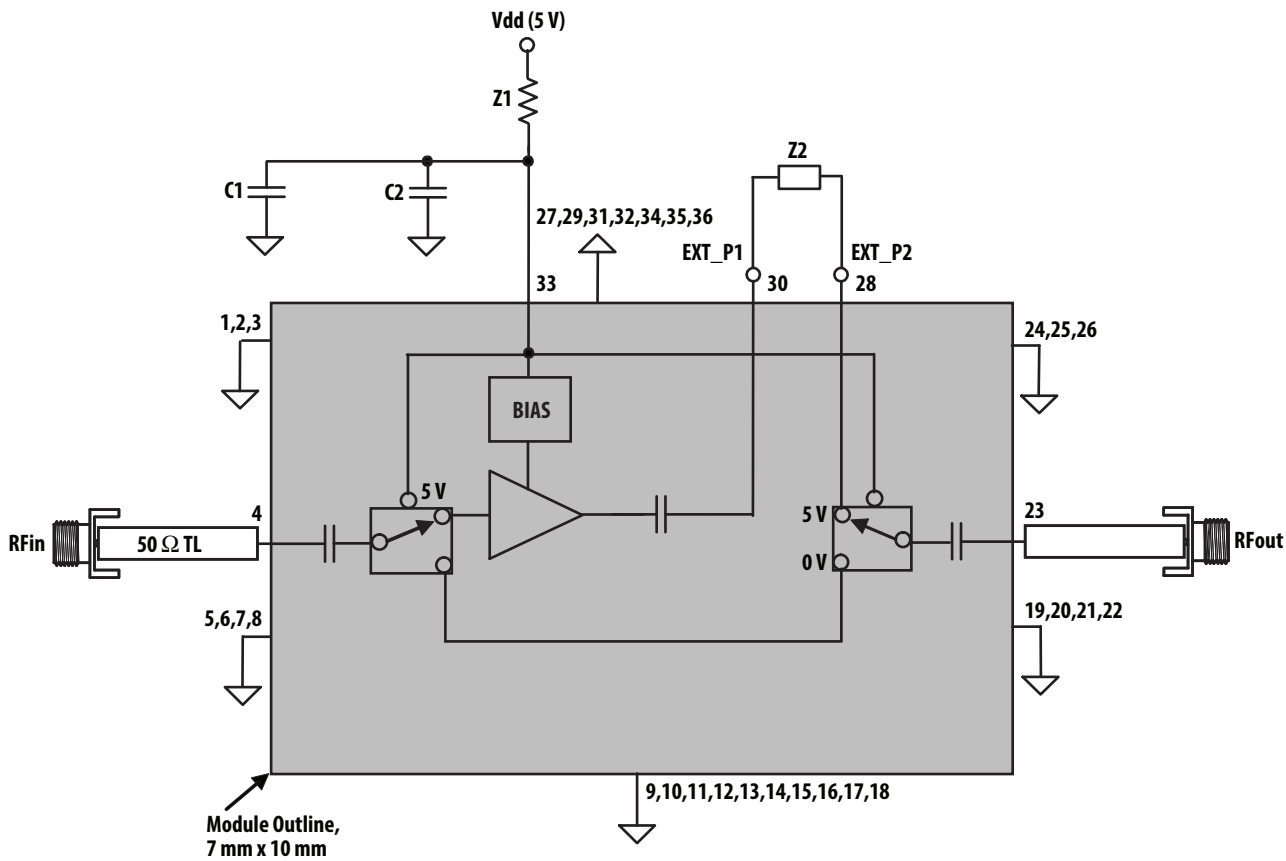


Figure 7. Demo Board Layout Diagram

- Recommended PCB material is 10 mils Rogers RO4350.
- Suggested component values may vary according to layout and PCB material.
- Copper trace between the 2 pads is removed before Z2 0(ohm) is placed.

Demo Board Schematic



Truth Table

	Vdd (V)
LNA Mode	5
Bypass Mode	0
Fail-safe Mode	NC

Bypass and Fail-safe mode have similar performance

Figure 8. Demo Board Schematic Diagram

Table 1. DC component list for 1850-1980 MHz

Part	Size	Value	Detail Part Number
C1	0805	2.2 μ F (Murata)	GRM21BR61E225KA12L
C2	0402	NU	NU
Z1	0805	0 Ω (Kamaya)	RMC1/8-JPTP
Z2	0603	0 Ω (Kamaya)	RMC1/16-JPTP

Notes:
 C1 is a DC bypass capacitor.
 Z1 is 0 Ω resistor or fuse.
 Z2 is a 0 Ω resistor if an external function block is not used.

Typical Performance

RF performance at $T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{ V}$ for LNA mode, $V_{dd} = 0\text{ V}$ for Bypass mode, measured on demo board in Figure 7. Signal = CW unless stated otherwise. Application Test Circuit is shown in Figure 8 and Table 1. IIP3 test condition: $F_{RF1}-F_{RF2} = 1\text{ MHz}$ with input power of -15 dBm per tone.

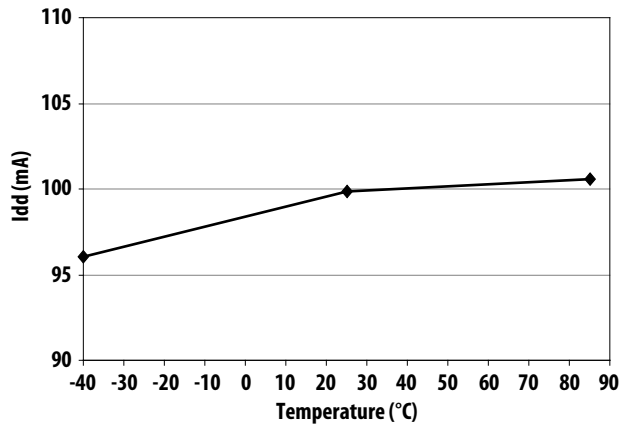


Figure 9. I_{dd} vs Temperature

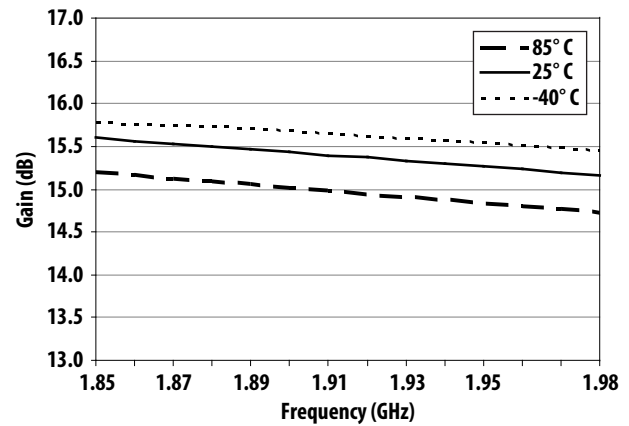


Figure 10. Gain vs Frequency

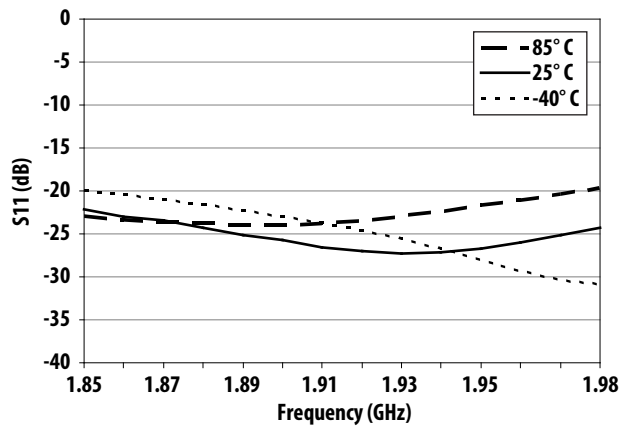


Figure 11. S₁₁ vs Frequency

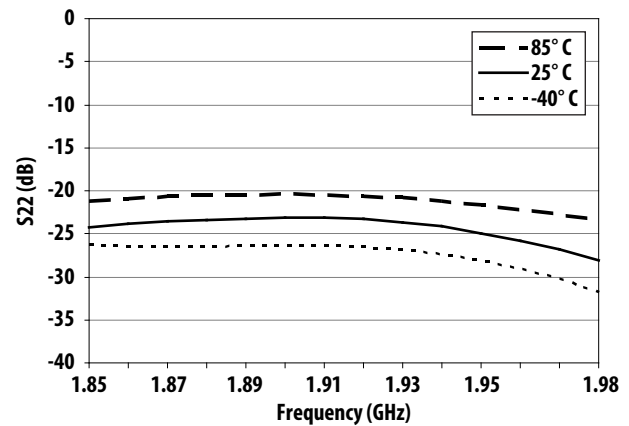


Figure 12. S₂₂ vs Frequency

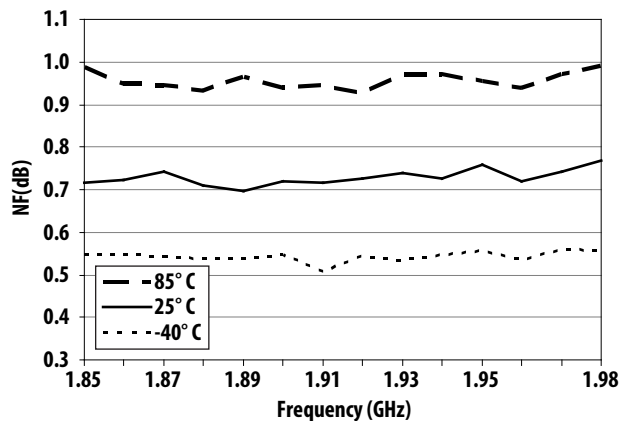


Figure 13. NF vs Frequency

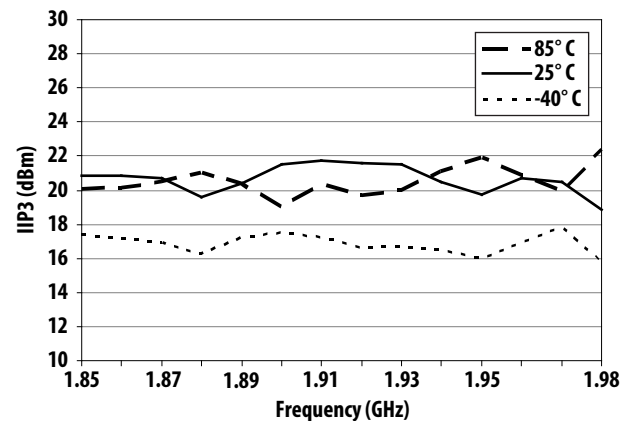


Figure 14. IIP3 vs Frequency

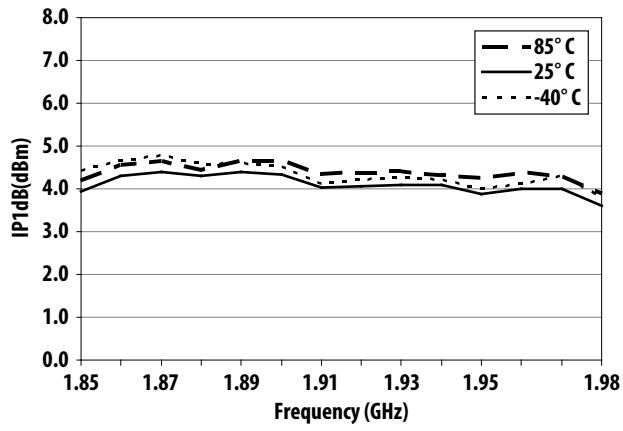


Figure 15. IP1dB vs Frequency

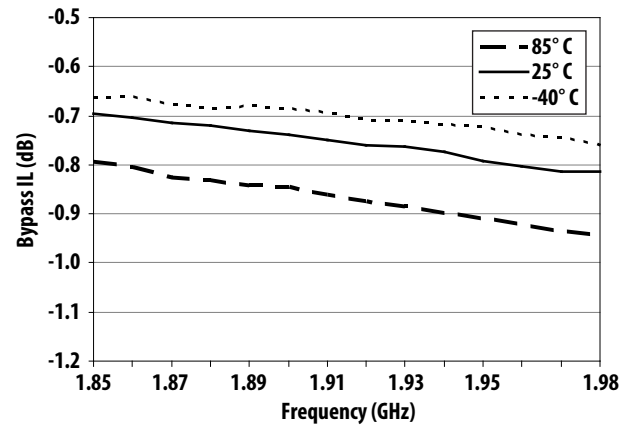


Figure 16. Bypass IL vs Frequency

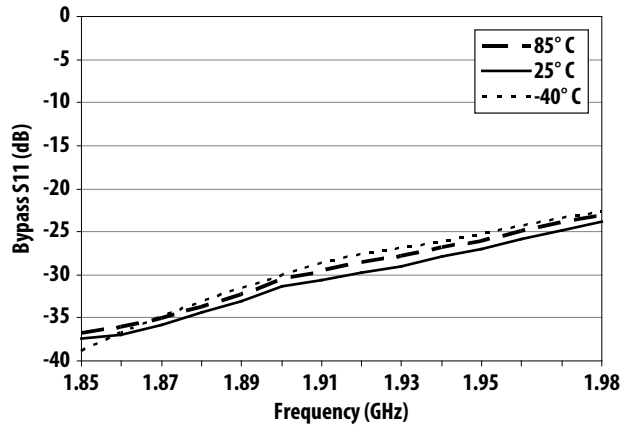


Figure 17. Bypass S11 vs Frequency

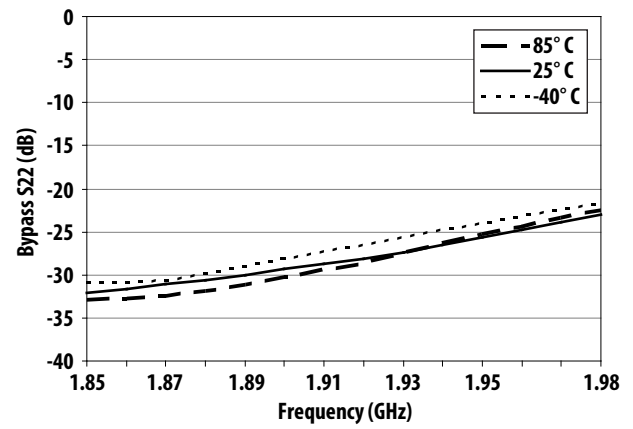


Figure 18. Bypass S22 vs Frequency

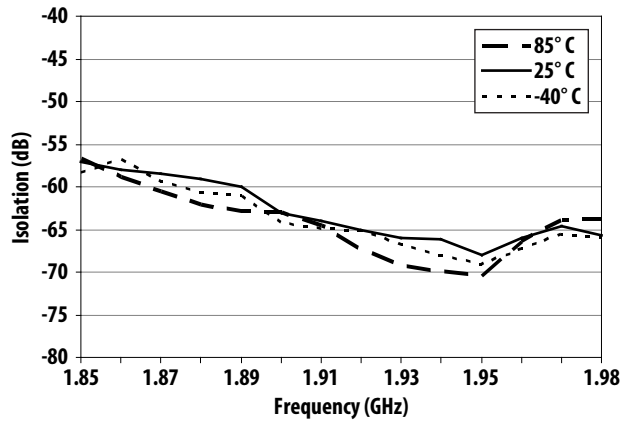
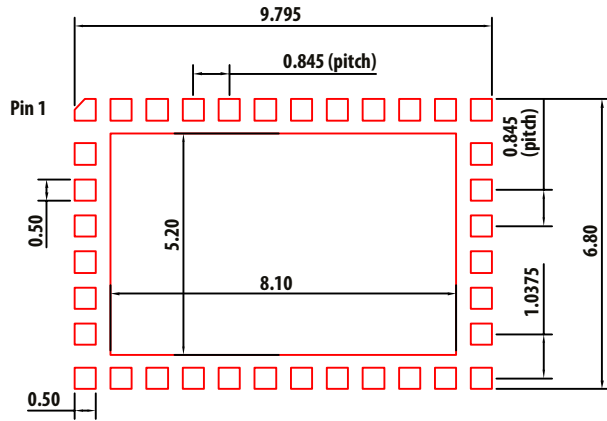


Figure 19. Bypass isolation vs Frequency (LNA mode)

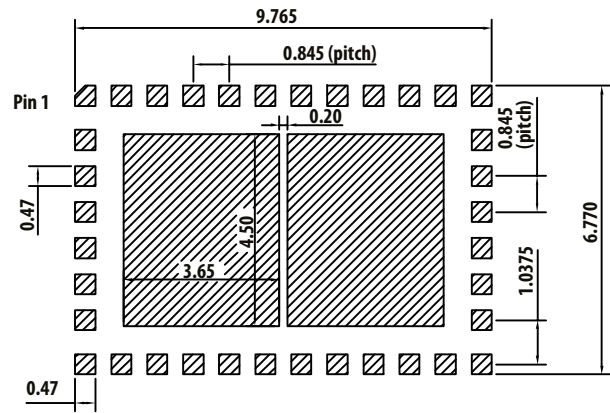
Typical Scattering Parameters, Vdd = 5 V, Idd = 100 mA
LNA SPAR (100 MHz – 20 GHz)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.1	-3.36	-108.50	-23.04	-80.03	-22.64	-84.81	-1.46	-64.90
0.5	-2.40	-164.91	-11.83	-64.20	-11.17	-60.28	-4.06	-161.07
1	-2.36	145.60	-14.83	-138.93	-14.38	-137.98	-2.59	118.69
1.5	-9.89	68.09	12.25	-27.95	-32.20	-20.18	-11.53	150.63
1.6	-13.06	91.80	14.92	-119.17	-35.67	-114.92	-18.97	97.76
1.7	-15.03	92.38	15.56	171.38	-32.38	164.10	-17.97	104.13
1.72	-15.73	92.85	15.59	159.16	-31.85	153.02	-18.69	99.44
1.74	-16.45	94.26	15.60	147.43	-31.42	142.55	-19.91	96.06
1.76	-17.19	96.86	15.60	136.02	-31.09	132.52	-21.61	95.73
1.78	-17.91	100.55	15.58	124.91	-30.79	123.04	-23.73	102.56
1.80	-18.56	104.80	15.55	114.12	-30.57	113.98	-25.46	118.95
1.82	-19.09	109.14	15.51	103.58	-30.39	104.94	-25.38	140.38
1.84	-19.48	113.47	15.46	93.27	-30.27	96.22	-23.48	153.89
1.86	-19.84	118.06	15.40	83.23	-30.20	87.62	-21.44	158.25
1.88	-20.21	122.91	15.34	73.36	-30.11	79.11	-19.69	157.32
1.90	-20.66	127.79	15.27	63.66	-30.04	70.53	-18.39	153.88
1.92	-21.17	132.84	15.21	54.09	-30.00	62.12	-17.57	148.82
1.94	-21.67	138.71	15.14	44.63	-29.97	53.65	-17.17	142.76
1.96	-21.97	145.74	15.08	35.23	-29.93	45.05	-17.08	135.45
1.98	-21.92	154.87	15.01	25.86	-29.90	36.39	-17.31	127.15
2	-21.51	164.95	14.93	16.50	-29.87	27.79	-17.91	118.35
2.5	-15.63	154.41	5.90	167.34	-34.32	-150.75	-3.57	114.23
3	-11.67	-146.42	-9.82	28.05	-40.12	157.08	-2.66	-81.73
3.5	-6.97	-157.37	-24.10	-45.15	-43.00	125.05	-1.37	-158.55
4	-5.31	-170.08	-33.47	-103.08	-47.50	107.94	-1.71	151.19
4.5	-4.92	177.82	-34.47	-160.53	-40.57	172.02	-2.58	100.65
5	-5.40	166.36	-32.66	88.15	-31.84	70.31	-2.99	52.03
5.5	-6.23	155.24	-30.02	30.25	-28.83	24.44	-3.11	-13.54
6	-7.98	156.73	-21.53	-44.30	-20.79	-42.71	-4.32	-102.68
7	-1.34	153.73	-24.35	84.91	-23.17	77.85	-2.17	143.13
8	-0.69	113.60	-49.59	86.65	-42.84	-60.98	-1.36	87.71
9	-1.20	93.89	-41.25	-74.07	-43.86	-87.39	-1.28	26.21
10	-2.77	62.12	-33.78	-32.79	-31.78	-28.12	-1.91	-18.49
11	-4.77	79.80	-25.78	-158.91	-26.08	-172.49	-3.00	-42.36
12	-5.33	26.84	-32.28	94.76	-32.68	89.98	-1.71	-71.96
13	-4.88	5.79	-23.67	-27.91	-23.18	-24.37	-2.23	-92.69
14	-4.96	-41.03	-28.30	-147.95	-27.25	-144.58	-2.58	-130.39
15	-15.26	42.07	-28.94	151.12	-28.13	155.24	-4.56	-178.30
16	-7.11	23.78	-25.23	-0.14	-25.47	6.67	-9.42	34.20
17	-4.84	-21.56	-33.02	1.60	-30.14	0.54	-7.87	-98.67
18	-7.91	-74.97	-31.08	-108.99	-29.84	-109.28	-7.40	-120.15
19	-4.05	-55.62	-27.15	133.81	-26.58	135.83	-9.04	-154.20
20	-4.15	-73.35	-38.65	-117.77	-40.08	-112.87	-7.77	-79.81

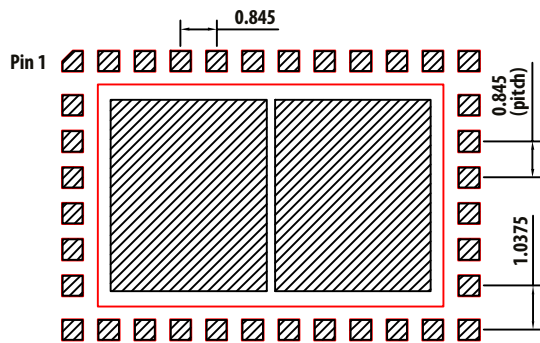
PCB Layout and Stencil Design



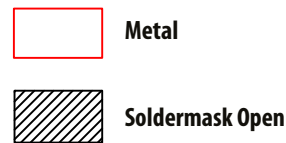
Land Pattern



Stencil Opening



Combination of Land Pattern and Stencil Opening



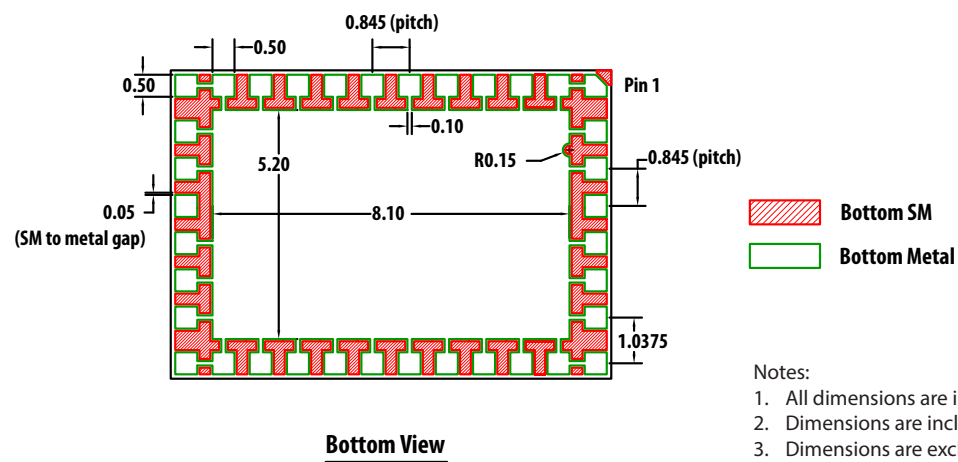
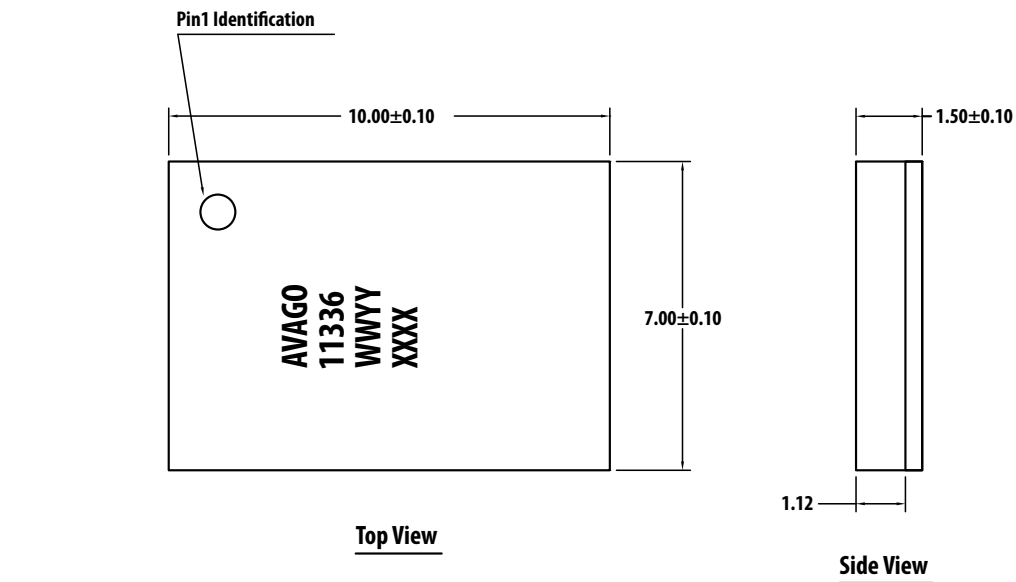
Note :

1. Recommended Land Pattern & Stencil Opening.
2. Stencil thickness is 0.1 mm (4 mils)
3. All dimension are in MM unless otherwise specified

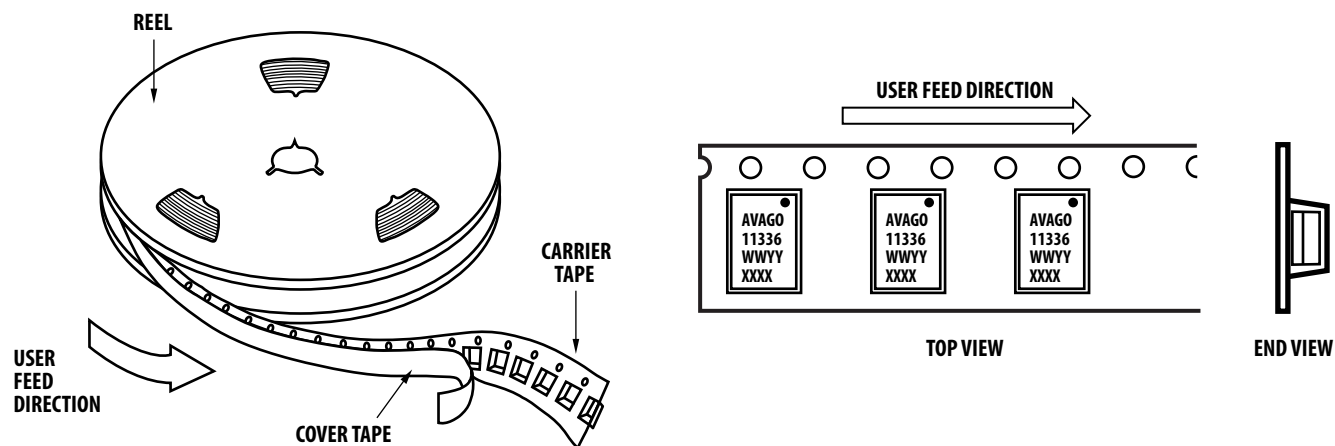
Part Number Ordering Information

Part Number	No. of Devices	Container
ALM-11336-TR1G	1000	13" Reel
ALM-11336-BLKG	100	antistatic bag

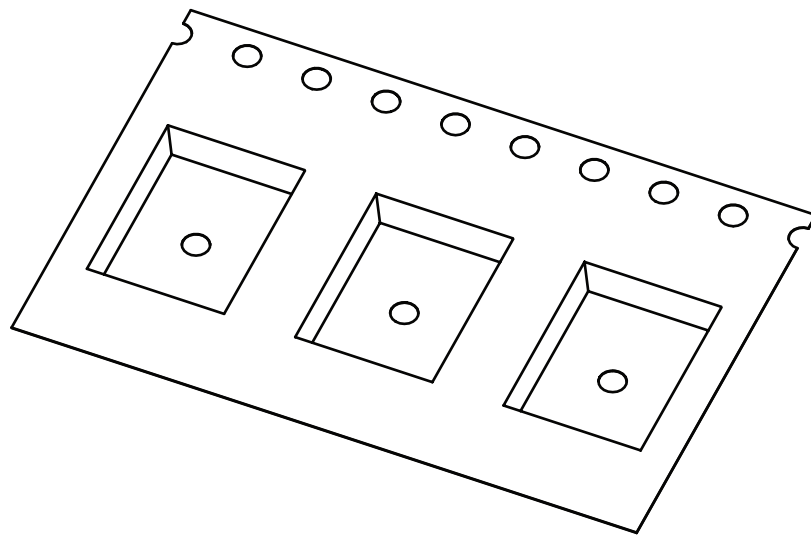
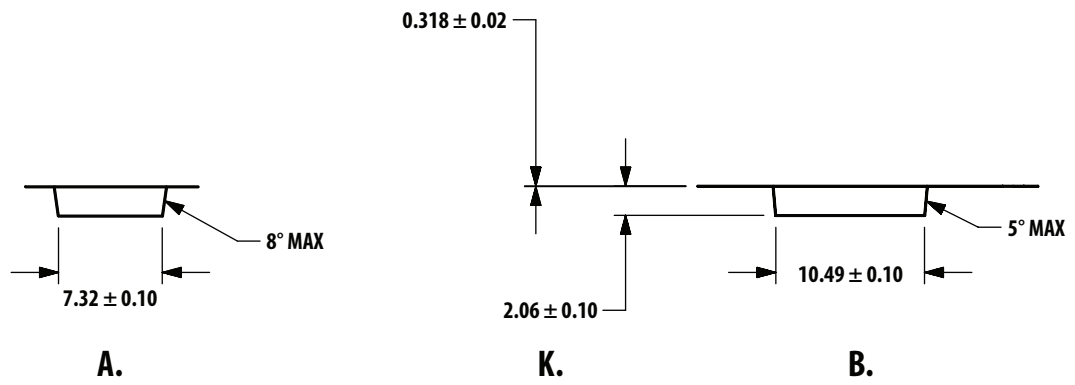
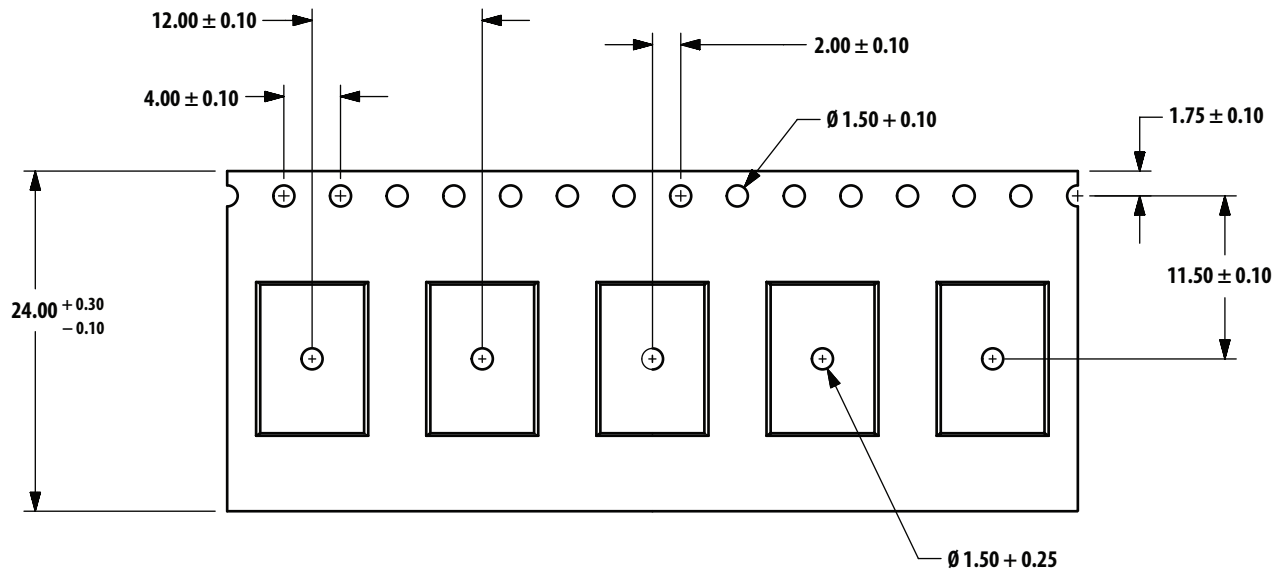
MCOB 7 x 10 Package Dimensions



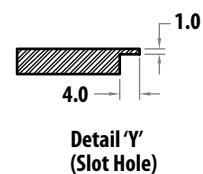
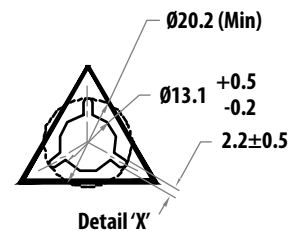
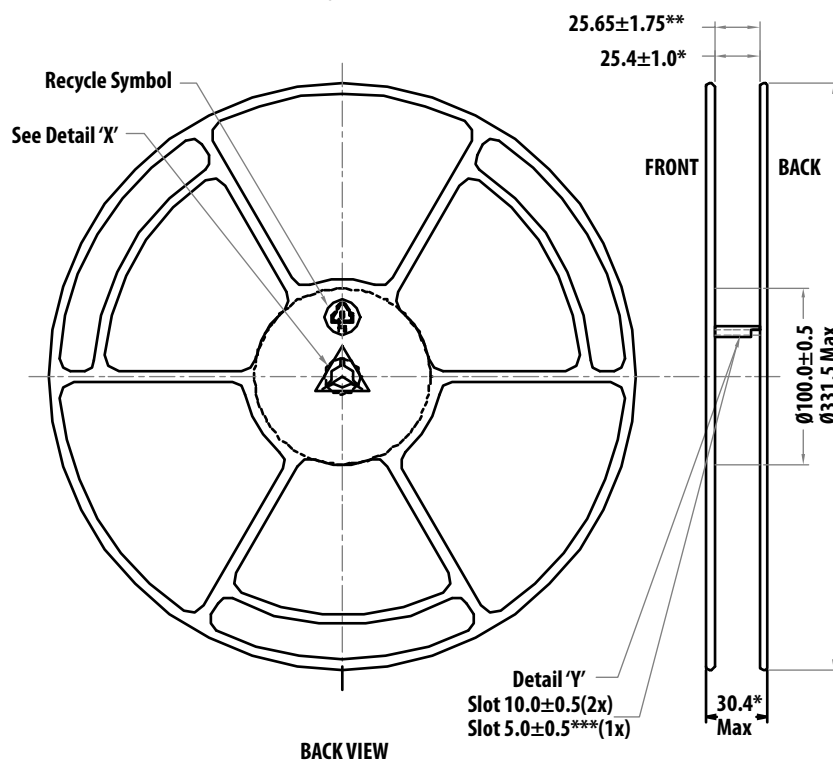
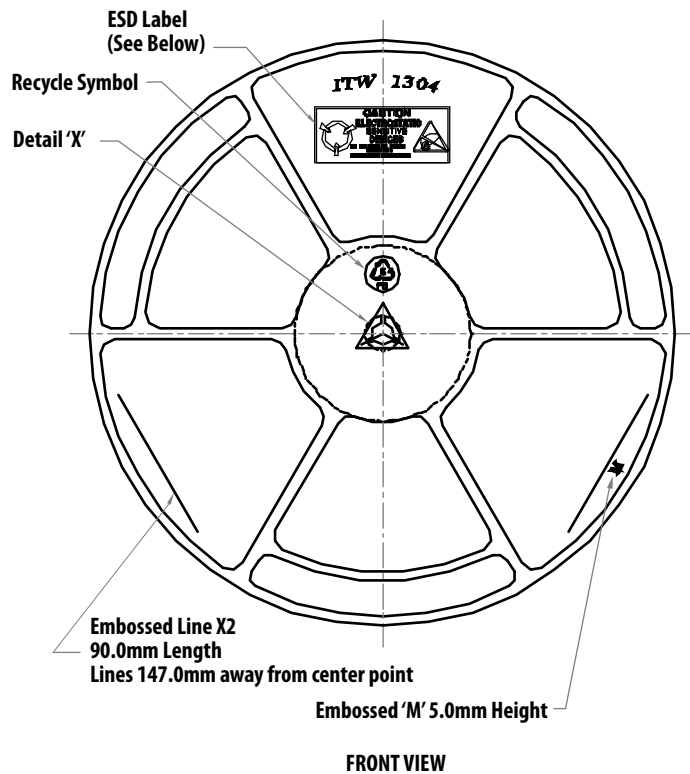
Device Orientation



Tape Dimensions



Reel Dimensions - 13" Reel



For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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