ISP1568A

Hi-Speed USB PCI host controller

Rev. 03 — 5 January 2010 Product data sheet

1. General description

The ISP1568A is a Peripheral Component Interconnect (PCI)-based, single-chip Universal Serial Bus (USB) host controller. It integrates one Original USB Open Host Controller Interface (OHCI) core, one Hi-Speed USB Enhanced Host Controller Interface (EHCI) core, and two transceivers that are compliant with Hi-Speed USB and Original USB. The functional parts of the ISP1568A are fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *Open Host Controller Interface Specification for USB Rev. 1.0a*, *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*, *PCI Local Bus Specification Rev. 2.2*, and *PCI Bus Power Management Interface Specification Rev. 1.1*.

The ISP1568A is pin-to-pin and function compatible with ST-Ericsson's ISP1562 and ISP1564, subject to the structure of the software.

Integrated high performance USB transceivers allow the ISP1568A to handle all Hi-Speed USB transfer speed modes: high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s). The ISP1568A provides two downstream ports, allowing simultaneous connection of USB devices at different speeds.

The ISP1568A is fully compatible with various operating system drivers, such as Microsoft Windows standard OHCI and EHCI drivers that are present in Windows XP, Windows 2000, and Red Hat Linux.

The ISP1568A directly interfaces to any 32-bit, 33 MHz PCI bus. Its PCI pins can source 3.3 V.

The ISP1568A is ideally suited for use in Hi-Speed USB mobile applications and embedded solutions.

2. Features

- Compliant with *Universal Serial Bus Specification Rev. 2.0*
- Compliant with *PCI Local Bus Specification Rev. 2.2*
- Supports data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s)
- One Original USB OHCI core is compliant with *Open Host Controller Interface Specification for USB Rev. 1.0a*
- One Hi-Speed USB EHCI core is compliant with *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*
- Supports PCI 32-bit, 33 MHz interface compliant with *PCI Local Bus Specification Rev. 2.2*, with support for $D3_{cold}$ standby and wake-up modes; all I/O pins are 3.3 V standard

- Compliant with *PCI Bus Power Management Interface Specification Rev. 1.1* for all hosts (EHCI and OHCI), and supports all power states: D0, D1, D2, $D3_{hot}$, and $D3_{cold}$
- CLKRUN support for mobile applications, such as internal notebook design
- Configurable subsystem ID and subsystem vendor ID through external EEPROM
- External EEPROM can be programmed using the external PCI interface; refer to Appendix I of *PCI Local Bus Specification Rev. 2.2*
- Digital and analog power separation for better ElectroMagnetic Interference (EMI) and ElectroStatic Discharge (ESD) protection
- Supports hot Plug and Play, and remote wake-up of peripherals
- Supports individual power switching and individual overcurrent protection for downstream ports
- Supports partial dynamic port-routing capability for downstream ports that allows sharing of the same physical downstream ports between the Original USB host controller and the Hi-Speed USB host controller
- Uses 12 MHz crystal oscillator to reduce system cost and EMI emissions
- Supports dual power supply: PCI $V_{aux(3V3)}$ and V_{CC}
- Operates at +3.3 V power supply input
- Low power consumption
- Full industrial operating temperature range from −40 °C to +85 °C
- Available in LQFP100 and TFBGA100 Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free packages

3. Applications

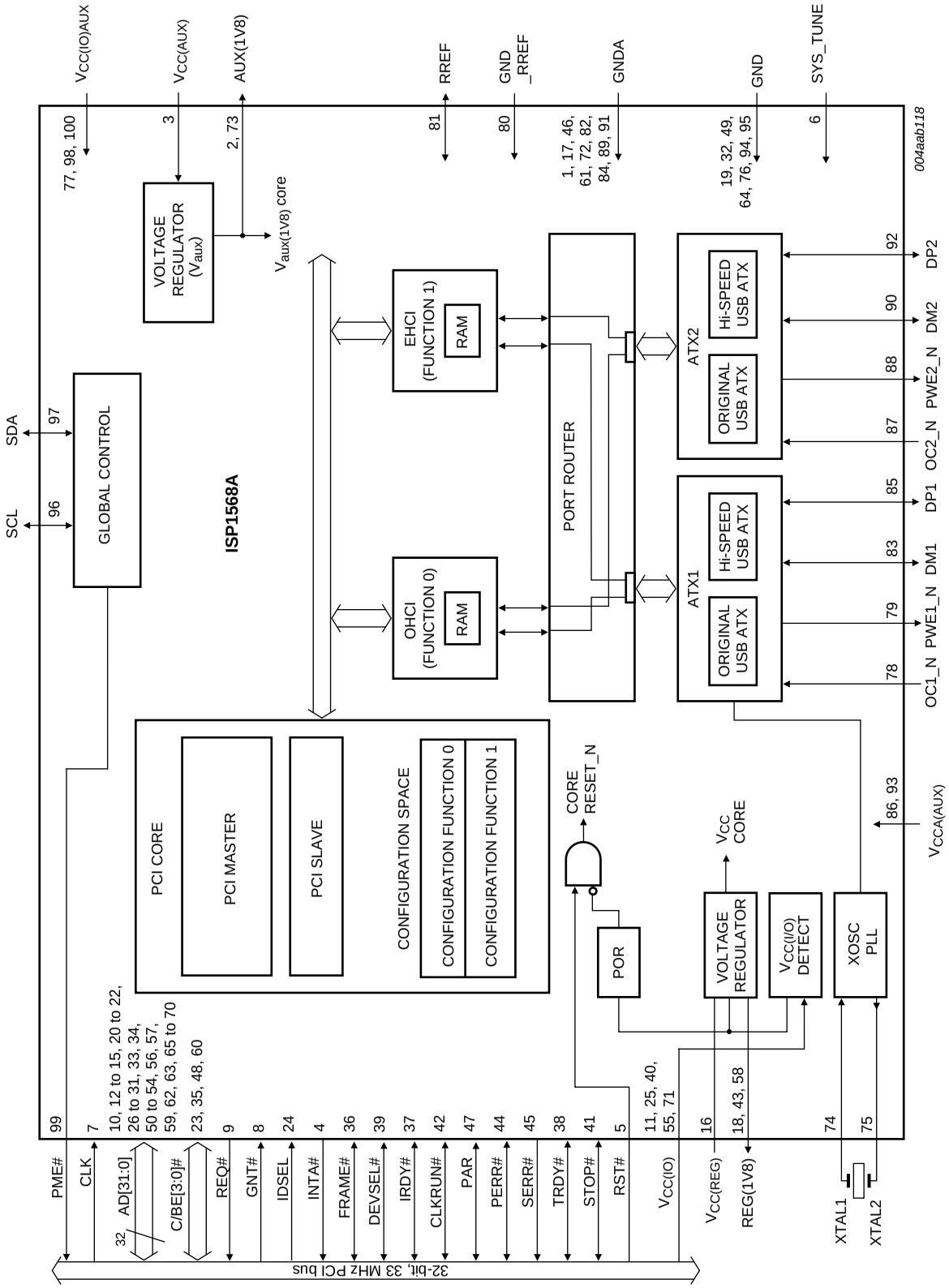
- Digital consumer appliances:
  - Portable consumer
  - Home entertainment
- Notebook
- PCI add-on card
- PC motherboard

4. Ordering information

Table 1. Ordering information

Commercial product code	Package description	Packing	Pitch	Minimum sellable quantity
ISP1568AHLUM	LQFP100; 100 leads; body 14 × 14 × 1.4 (mm)	13 inch tape and reel dry pack	0.5 mm	1000 pieces
ISP1568AETUM	TFBGA100; 100 balls; body 9 × 9 × 0.7 (mm)	13 inch tape and reel dry pack	0.8 mm	1000 pieces

5. Block diagram



Remark: The figure shows the LQFP pinout. For the TFBGA ballout, see Table 2.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

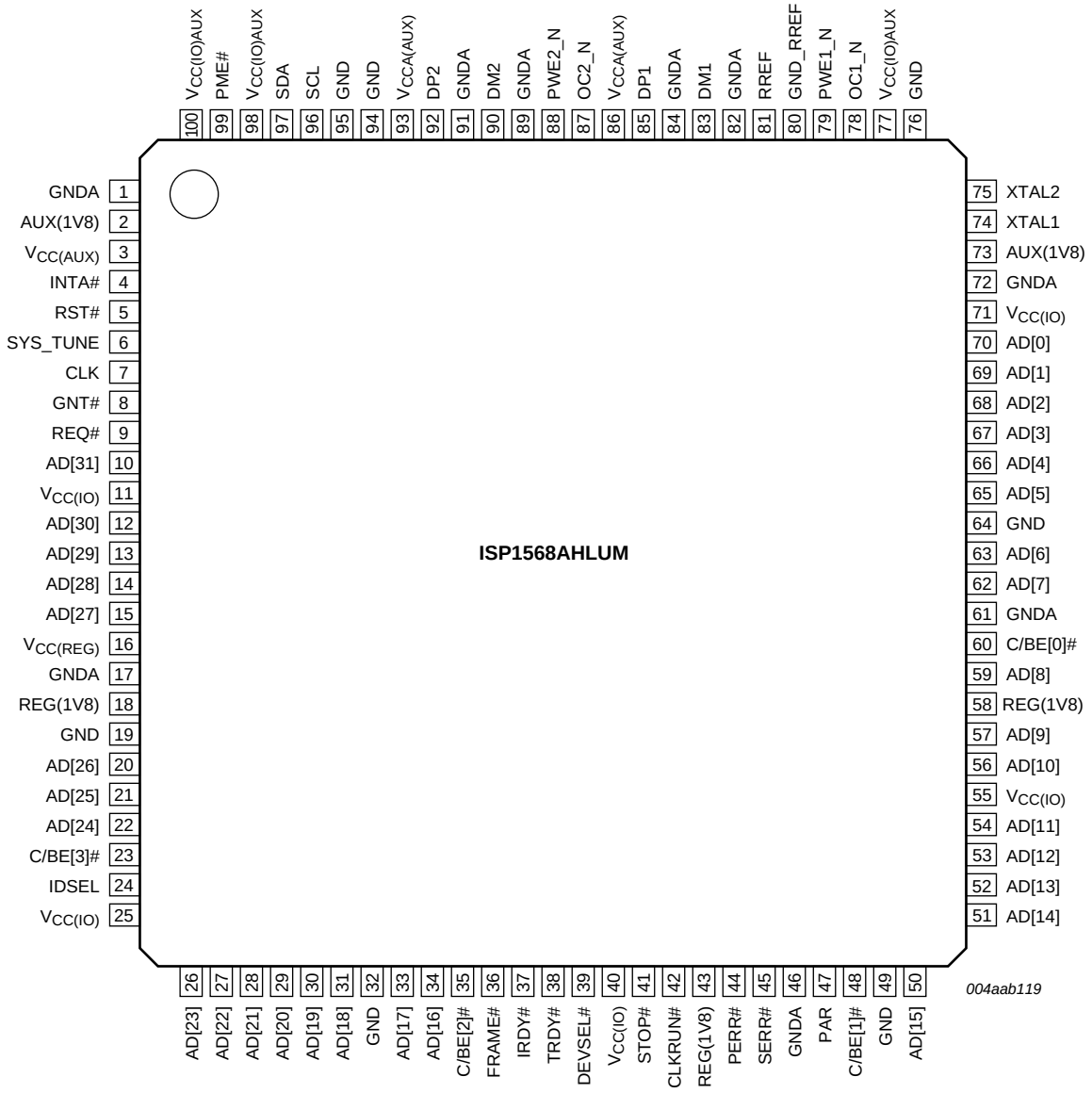


Fig 2. Pin configuration LQFP100 (top view)

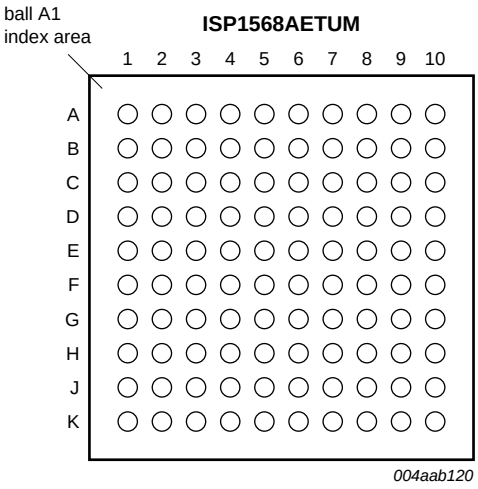


Fig 3. Pin configuration TFBGA100 (top view)

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin		Type[2]	Description
	LQFP100	TFBGA100		
GNDA	1	B1	-	analog ground
AUX(1V8)	2	C2	-	1.8 V auxiliary output voltage; only for voltage conditioning; cannot be used to supply power to external components; see Section 7.8
$V_{CC(AUX)}$[3]	3	C1	-	auxiliary supply voltage; see Section 7.8
INTA#	4	D1	O	PCI interrupt PCI pad; 3.3 V signaling; open-drain
RST#	5	C3	I	PCI reset; used to bring PCI-specific registers, sequencers, and signals to a consistent state 3.3 V input pad; CMOS
SYS_TUNE	6	C6	I	used for system tuning; for connection details, see Table 13, Section 11.4, and Table 118
CLK	7	D2	I	PCI system clock; see Table 127 PCI pad; 3.3 V signaling
GNT#	8	D3	I	PCI grant; indicates to the agent that access to the bus is granted PCI pad; 3.3 V signaling
REQ#	9	D4	O	PCI request; indicates to the arbitrator that the agent wants to use the bus PCI pad; 3.3 V signaling
AD[31]	10	E1	I/O	bit 31 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(IO)}$	11	E2	-	I/O pads supply voltage; see Section 7.8
AD[30]	12	E3	I/O	bit 30 of multiplexed PCI address and data PCI pad; 3.3 V signaling

Table 2. Pin description *...continued*

Symbol[1]	Pin		Type[2]	Description
	LQFP100	TFBGA100		
AD[29]	13	E4	I/O	bit 29 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[28]	14	E5	I/O	bit 28 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[27]	15	F3	I/O	bit 27 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(REG)}$	16	F1	-	regulator supply voltage; see Section 7.8
GNDA	17	G1	-	analog ground
REG(1V8)	18	G2	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; see Section 7.8
GND	19	F4	-	ground
AD[26]	20	F2	I/O	bit 26 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[25]	21	G3	I/O	bit 25 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[24]	22	H1	I/O	bit 24 of multiplexed PCI address and data PCI pad; 3.3 V signaling
C/BE[3]#	23	H2	I/O	byte 3 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
IDSEL	24	J1	I	PCI initialization device select; used as a chip select during configuration read and write transactions PCI pad; 3.3 V signaling
$V_{CC(IO)}$	25	J2	-	I/O pads supply voltage; see Section 7.8
AD[23]	26	K1	I/O	bit 23 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[22]	27	K2	I/O	bit 22 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[21]	28	H3	I/O	bit 21 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[20]	29	J3	I/O	bit 20 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[19]	30	K3	I/O	bit 19 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[18]	31	G4	I/O	bit 18 of multiplexed PCI address and data PCI pad; 3.3 V signaling
GND	32	H4	-	ground
AD[17]	33	J4	I/O	bit 17 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[16]	34	K4	I/O	bit 16 of multiplexed PCI address and data PCI pad; 3.3 V signaling

Table 2. Pin description *...continued*

Symbol[1]	Pin		Type[2]	Description
	LQFP100	TFBGA100		
C/BE[2]#	35	F5	I/O	byte 2 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
FRAME#	36	G5	I/O	PCI cycle frame; driven by the master to indicate the beginning and duration of an access PCI pad; 3.3 V signaling
IRDY#	37	H5	I/O	PCI initiator ready; indicates the ability of the initiating agent to complete the current data phase of a transaction PCI pad; 3.3 V signaling
TRDY#	38	J5	I/O	PCI target ready; indicates the ability of the target agent to complete the current data phase of a transaction PCI pad; 3.3 V signaling
DEVSEL#	39	H6	I/O	PCI device select; indicates if any device is selected on the bus PCI pad; 3.3 V signaling
$V_{CC(IO)}$	40	K5	-	I/O pads supply voltage; see Section 7.8
STOP#	41	G6	I/O	PCI stop; indicates that the current target is requesting the master to stop the current transaction PCI pad; 3.3 V signaling
CLKRUN#	42	K6	I/O	PCI CLKRUN signal; pull down to ground through a 10 kΩ resistor PCI pad; 3.3 V signaling; open-drain
REG(1V8)	43	J6	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; see Section 7.8
PERR#	44	J7	I/O	PCI parity error; used to report data parity errors during all PCI transactions, except a special cycle PCI pad; 3.3 V signaling
SERR#	45	J8	O	PCI system error; used to report address parity errors and data parity errors on the Special Cycle command, or any other system error in which the result will be catastrophic PCI pad; 3.3 V signaling; open-drain
GNDA	46	K7	-	analog ground
PAR	47	K8	I/O	PCI parity PCI pad; 3.3 V signaling
C/BE[1]#	48	K9	I/O	byte 1 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
GND	49	H7	-	ground
AD[15]	50	K10	I/O	bit 15 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[14]	51	J10	I/O	bit 14 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[13]	52	H10	I/O	bit 13 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[12]	53	H9	I/O	bit 12 of multiplexed PCI address and data PCI pad; 3.3 V signaling

Table 2. Pin description *...continued*

Symbol[1]	Pin		Type[2]	Description
	LQFP100	TFBGA100		
AD[11]	54	H8	I/O	bit 11 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(IO)}$	55	J9	-	I/O pads supply voltage; see Section 7.8
AD[10]	56	G7	I/O	bit 10 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[9]	57	G8	I/O	bit 9 of multiplexed PCI address and data PCI pad; 3.3 V signaling
REG(1V8)	58	G9	-	1.8 V regulator output voltage; only for voltage conditioning; cannot be used to supply power to external components; see Section 7.8
AD[8]	59	F10	I/O	bit 8 of multiplexed PCI address and data PCI pad; 3.3 V signaling
C/BE[0]#	60	F6	I/O	byte 0 of multiplexed PCI bus command and byte enable PCI pad; 3.3 V signaling
GNDA	61	G10	-	analog ground
AD[7]	62	F9	I/O	bit 7 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[6]	63	F8	I/O	bit 6 of multiplexed PCI address and data PCI pad; 3.3 V signaling
GND	64	F7	-	ground
AD[5]	65	E7	I/O	bit 5 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[4]	66	E8	I/O	bit 4 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[3]	67	E10	I/O	bit 3 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[2]	68	D10	I/O	bit 2 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[1]	69	D9	I/O	bit 1 of multiplexed PCI address and data PCI pad; 3.3 V signaling
AD[0]	70	D8	I/O	bit 0 of multiplexed PCI address and data PCI pad; 3.3 V signaling
$V_{CC(IO)}$	71	E9	-	I/O pads supply voltage; see Section 7.8
GNDA	72	C10	-	analog ground
AUX(1V8)	73	B9	-	1.8 V auxiliary output voltage; only for voltage conditioning; cannot be used to supply power to external components; see Section 7.8
XTAL1	74	B10	AI	crystal oscillator input; this can also be a 12 MHz clock input at 1.8 V
XTAL2	75	A10	AO	crystal oscillator output (12 MHz); leave open when clock is used
GND	76	C8	-	ground
$V_{CC(IO)AUX}$	77	A9	-	I/O pads auxiliary supply voltage; see Section 7.8
OC1_N	78	C9	I	overcurrent sense input for the USB downstream port 1 (digital); when not in use, connect this pin to 3.3 V 3.3 V input pad; CMOS

Table 2. Pin description *...continued*

Symbol[1]	Pin		Type[2]	Description
	LQFP100	TFBGA100		
PWE1_N	79	D7	O	power enable for the USB downstream port 1 3.3 V output pad; 3 ns slew rate control; CMOS; open-drain
GND_RREF	80	A8	-	ground for external resistor on pin RREF
RREF	81	B8	AI/O	analog connection for the external resistor (12 kΩ ± 1 %)
GNDA	82	C7	-	analog ground
DM1	83	A7	AI/O	D–; analog connection for the USB downstream port 1; pull down to ground through a 15 kΩ resistor, even when the port is not used
GNDA	84	B7	-	analog ground
DP1	85	A6	AI/O	D+; analog connection for the USB downstream port 1; pull down to ground through a 15 kΩ resistor, even when the port is not used
$V_{CCA(AUX)}$	86	B6	-	auxiliary analog supply voltage; see Section 7.8
OC2_N	87	E6	I	overcurrent sense input for the USB downstream port 2 (digital); when not in use, connect this pin to 3.3 V 3.3 V input pad; CMOS
PWE2_N	88	D6	O	power enable for the USB downstream port 2 3.3 V output pad; 3 ns slew rate control; CMOS; open-drain
GNDA	89	C5	-	analog ground
DM2	90	A5	AI/O	D–; analog connection for the USB downstream port 2; pull down to ground through a 15 kΩ resistor, even when the port is not used
GNDA	91	B5	-	analog ground
DP2	92	A4	AI/O	D+; analog connection for the USB downstream port 2; pull down to ground through a 15 kΩ resistor, even when the port is not used
$V_{CCA(AUX)}$	93	B4	-	auxiliary analog supply voltage; see Section 7.8
GND	94	B2	-	ground
GND	95	D5	-	ground
SCL	96	B3	I/O	I^2C-bus clock; pull up to 3.3 V through a 10 kΩ resistor[4] I^2C-bus pad; clock signal
SDA	97	A3	I/O	I^2C-bus data; pull up to 3.3 V through a 10 kΩ resistor[4] I^2C-bus pad; data signal
$V_{CC(IO)AUX}$	98	A2	-	I/O pads auxiliary supply voltage; see Section 7.8
PME#	99	A1	O	PCI Power Management Event; used by a device to request a change in the device or system power state PCI pad; 3.3 V signaling; open-drain
$V_{CC(IO)AUX}$	100	C4	-	I/O pads auxiliary supply voltage; see Section 7.8

[1] Symbol names ending with # represent active-LOW signals for PCI pins, for example: NAME#. Symbol names ending with underscore N represent active-LOW signals for USB pins, for example: NAME_N.

[2] I = input; O = output; I/O = input/output; AI/O = analog input/output; AI = analog input; AO = analog output.

[3] $V_{CC(AUX)}$ should come up not later than $V_{CC(IO)}$ and $V_{CC(REG)}$.

[4] Connect to ground if I^2C-bus is not used.

7. Functional description

7.1 OHCI host controller

An OHCI host controller per port transfers data to devices at the Original USB defined bit rate of 12 Mbit/s or 1.5 Mbit/s.

7.2 EHCI host controller

The EHCI host controller transfers data to a Hi-Speed USB compliant device at the Hi-Speed USB defined bit rate of 480 Mbit/s. When the EHCI host controller has the ownership of a port, OHCI host controllers are not allowed to modify the port register. All additional port bit definitions required for the enhanced host controller are not visible to the OHCI host controller.

7.3 Dynamic port-routing logic

The port-routing feature allows sharing of the same physical downstream ports between the Original USB host controller and the Hi-Speed USB host controller. This requirement of *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0* provides ports that are multiplexed with the ports of the OHCI.

The EHCI is responsible for the port-routing switching mechanism. Two register bits are used for ownership switching. During power-on and system reset, the default ownership of all downstream ports is the OHCI. The enhanced Host Controller Driver (HCD) controls the ownership during normal functionality.

7.4 Hi-Speed USB analog transceivers

Hi-Speed USB analog transceivers directly interface to USB cables through integrated termination resistors. These transceivers can transmit and receive serial data at all data rates: high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s).

7.5 Power management

The ISP1568A provides an advanced power management capability interface that is compliant with *PCI Bus Power Management Interface Specification Rev. 1.1*. Power is controlled and managed by the interaction between drivers and PCI registers.

For a detailed description on power management, see Section 10.

7.6 Phase-Locked Loop (PLL)

A 12 MHz-to-30 MHz and 48 MHz clock multiplier PLL is integrated on-chip. This allows the use of a low-cost 12 MHz crystal, which also minimizes EMI.

7.7 Power-On Reset (POR)

Figure 4 shows a possible curve of AUX(1V8) and REG(1V8) with dips at t2 to t3 and t4 to t5. At t0, POR will start with 1. At t1, the detector passes through the trip level. Another delay will be added before POR drops to 0 to ensure that the length of the generated detector pulse, POR, is large enough to reset asynchronous flip-flops. If the dip is too short (t4 to t5 < 11 μs), POR will not react and will stay LOW.

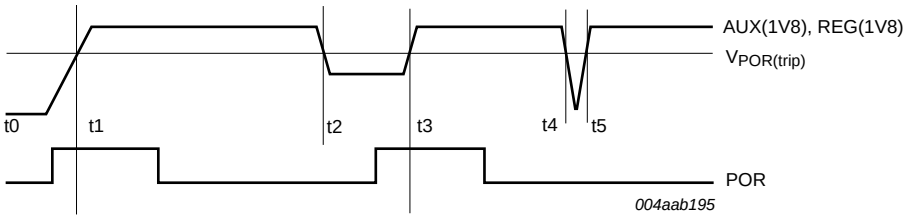
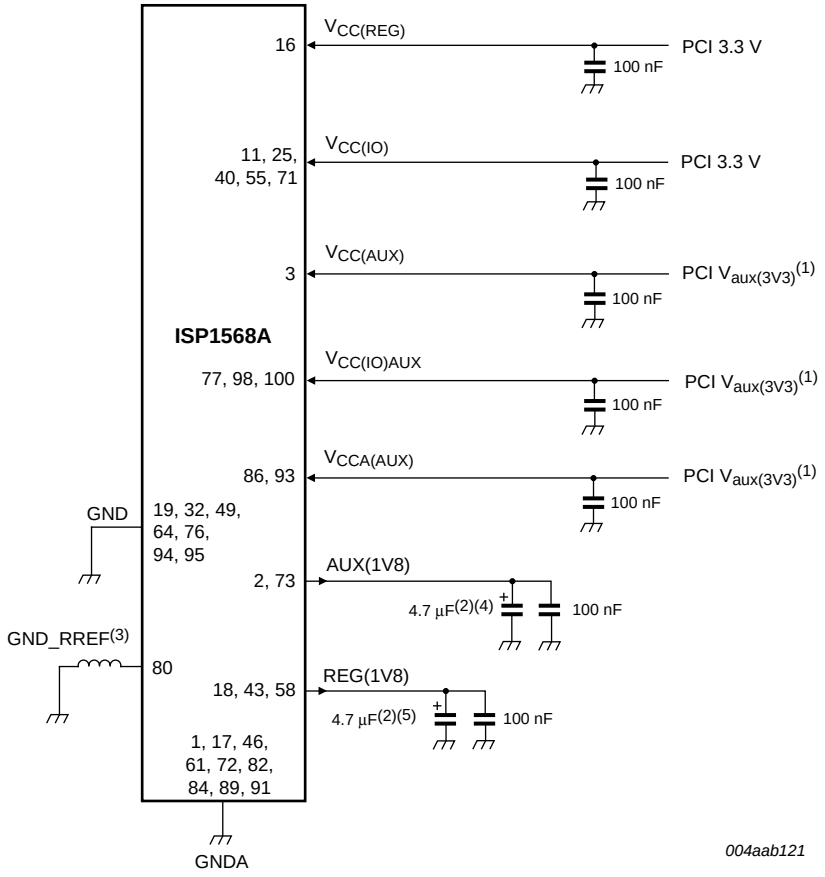


Fig 4. Power-on reset

7.8 Power supply

Figure 5 shows the ISP1568A power supply connection.



Remark: The 100 nF capacitor is needed on each individual pin, and is not shared among the listed pins.

Remark: The figure shows the LQFP pinout. For the TFBGA ballout, see Table 2.

(1) If $V_{aux(3V3)}$ is not present on PCI, the pin must be connected to PCI 3.3 V.

(2) This electrolytic or tantalum capacitor must be of LOW ESR type (0.2 Ω to 2 Ω).

(3) The use of ferrite bead is optional. Can be directly connected to ground.

(4) This electrolytic or tantalum capacitor is needed only on pin 2.

(5) This electrolytic or tantalum capacitor is needed only on pin 18.

Fig 5. Power supply connection

7.9 PCI reset at power up

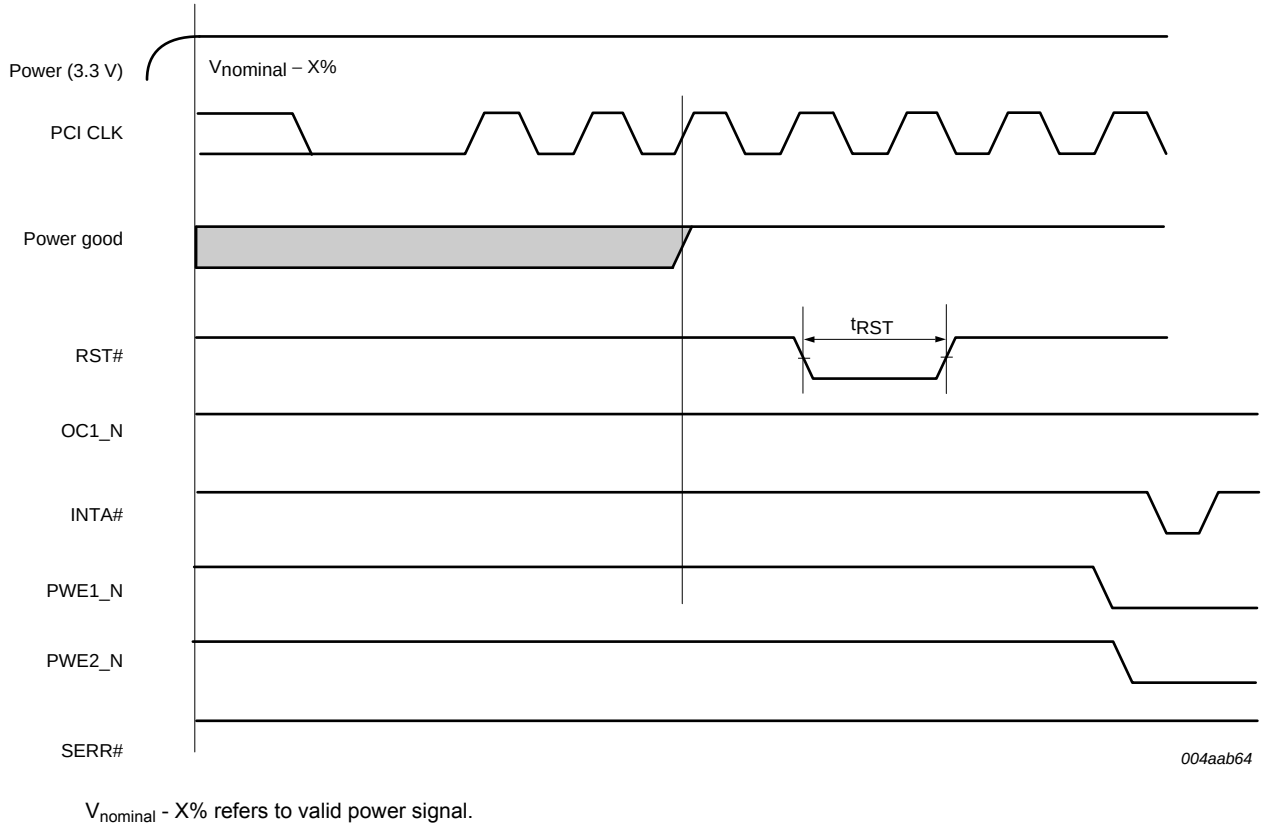
An embedded system may have multiple power rails, such as V_{CC} and $V_{CC(I/O)}$. If the ISP1568A is powered up by different power rails, V_{CC} and $V_{CC(I/O)}$ may start at different times. In such cases, signal such as OCn_N and PWEn_N may start to toggle because of powering up of power rails at different times. Therefore, it is required to wait until all the power rails for the ISP1568A are stable before asserting the PCI reset.

The PCI reset pin of the ISP1568A, RST#, is an active-LOW signal. It must be kept high with a pull-up resistor connected to 3.3 V and asserted only when the following conditions are met.

- Power and clock are stable.
- Critical signals, such as OC1_N, INTA#, PWE1_N, PWE2_N, and SERR# are in inactive state.

This is to avoid any uncertainties or race condition that can cause toggling of critical signals during the PCI reset assertion. RST# can be immediately asserted after the stable clock and stable power supply (No waiting time). The minimum time for reset active after stable power is 1 ms (t_{rst}).

Figure 6 shows the recommendation for RST# with respect to critical signals.



$V_{nominal}$ - X% refers to valid power signal.

Fig 6. Recommendation for RST# assertion

In summary, it is recommended that you keep RST# at HIGH during power on to prevent the ISP1568A from entering into undefined behavior.

8. PCI

8.1 PCI interface

The PCI interface has two functions. Function #0 is for the OHCI host controller and function #1 is for the EHCI host controller. These functions support both master and target accesses, and share the same PCI interrupt signal INTA#. These functions provide memory-mapped, addressable operational registers as required in *Open Host Controller Interface Specification for USB Rev. 1.0a* and *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.

Each function has its own configuration space. The PCI enumerator must allocate the memory address space for each of these functions. Power management is implemented in each PCI function and all power states are provided. This allows the system to achieve low power consumption by switching off the functions that are not required.

8.1.1 PCI configuration space

PCI Local Bus Specification Rev. 2.2 requires that each of the two PCI functions of the ISP1568A provides its own PCI configuration registers, which can vary in size. In addition to the basic PCI configuration header registers, these functions implement capability registers to support power management.

The registers of each of these functions are accessed by the respective driver. Section 8.2 provides a detailed description of various PCI configuration registers.

8.1.2 PCI initiator and target

A PCI initiator initiates PCI transactions to the PCI bus. A PCI target responds to PCI transactions as a slave. In the ISP1568A, the open host controller and the enhanced host controller function as both initiators or targets of PCI transactions issued by the host CPU.

All USB host controllers have their own operational registers that can be accessed by the system driver software. Drivers use these registers to configure the host controller hardware system, issue commands to it, and monitor the status of the current hardware operation. The host controller plays the role of a PCI target. All operational registers of the host controllers are the PCI transaction targets of the CPU.

Normal USB transfers require the host controller to access system memory fields, which are allocated by USB HCDs and PCI drivers. The host controller hardware interacts with the HCD by accessing these buffers. The host controller works as an initiator in this case and becomes a PCI master.

8.2 PCI configuration registers

OHCI USB host controllers and the EHCI USB host controller contain two sets of software-accessible hardware registers: PCI configuration registers and memory-mapped host controller registers.

A set of configuration registers is implemented for each of the two PCI functions of the ISP1568A, see Table 3.

Remark: In addition to the normal PCI header, from offset index 00h to 3Fh, implementation-specific registers are defined to support power management and function-specific features.

The HCD does not usually interact with the PCI configuration space. The configuration space is used only by the PCI enumerator to identify the USB host controller and assign appropriate system resources by reading the Vendor ID (VID) and the Device ID (DID).

Table 3. PCI configuration space registers of OHCI and EHCI

Address	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0	Reset value[1]	
					Func0 OHCI	Func1 EHCI
PCI configuration header registers						
00h	Device ID[15:0]		Vendor ID[15:0]		1561 1131h	1562 1131h
04h	Status[15:0]		Command[15:0]		0210 **0000**h	0210 **0000**h
08h	Class Code[23:0]			Revision ID[7:0]	0C03 1030h	0C03 2030h
0Ch	reserved	Header Type[7:0]	Latency Timer[7:0]	CacheLine Size[7:0]	0080 **0000**h	0080 **0000**h
10h	Base Address 0[31:0]				**0000 0**000h	**0000 00**00h
14h	reserved				0000 0000h	0000 0000h
18h						
1Ch						
20h						
24h						
28h						
2Ch	Subsystem ID[15:0]		Subsystem Vendor ID[15:0]		1561 1131h	1562 1131h
30h	reserved				0000 0000h	0000 0000h
34h	reserved			Capabilities Pointer[7:0]	0000 00DCh	0000 00DCh
38h	reserved				0000 0000h	0000 0000h
3Ch	Max_Lat[7:0]	Min_Gnt[7:0]	Interrupt Pin[7:0]	Interrupt Line[7:0]	**2A01 0100**h	**1002 0100**h
40h	reserved		Retry Timeout	TRDY Timeout	0000 **0000**h	0000 **0000**h
Enhanced host controller-specific PCI registers						
60h	PORTWAKECAP[15:0]		FLADJ[7:0]	SBRN[7:0]	-	**0007 20**20h
Power management registers						
DCh	PMC[15:0]		Next_Item_Ptr [7:0]	Cap_ID[7:0]	D282 0001h	FE82 E401h
E0h	Data[7:0]	PMCSR_BSE [7:0]	PMCSR[15:0]		0000 **XX00**h[2]	0000 **XX00**h[2]
VPD specific registers						
E4h	VPD_Addr[15:0]		VPD_Next_Item_Ptr[7:0]	VPD_Cap_ID [7:0]	-	0000 0003h
E8h	VPD_Data[31:0]				-	0000 0000h

[1] Reset values that are highlighted (for example, **0**) indicate read and write accesses; and reset values that are not highlighted (for example, 0) indicate read-only.

[2] See Section 8.2.3.4.

8.2.1 PCI configuration header registers

The enhanced host controller implements normal PCI header register values, except the values for the memory-mapping base address register, serial bus number, and device ID.

8.2.1.1 Vendor ID register

This read-only register identifies the manufacturer of the device. PCI Special Interest Group (PCI-SIG) assigns valid vendor identifiers to ensure the uniqueness of the identifier. The bit description is shown in Table 4.

Table 4. VID - Vendor ID register (address 00h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	VID[15:0]	R	1131h*	**Vendor ID**: This read-only register value is assigned to ST-Ericsson by PCI-SIG as 1131h.

8.2.1.2 Device ID register

This is a 2-byte read-only register that identifies a particular device. The identifier is allocated by ST-Ericsson. Table 5 shows the bit description of the register.

Table 5. DID - Device ID register (address 02h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	DID[15:0]	R	156Xh*[1]	**Device ID**: This register value is defined by ST-Ericsson to identify the USB host controller IC product.

[1] X is 1h for OHCI; X is 2h for EHCI.

8.2.1.3 Command register

This is a 2-byte register that provides coarse control over the ability of a device to generate and respond to PCI cycles. The bit allocation of the Command register is given in Table 6. When logic 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses, except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not support this base level of functionality.

Table 6. Command register (address 04h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							SERRE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SCTRL	PER	VGAPS	MWIE	SC	BM	MS	reserved[1]
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R	R/W	R	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 7. Command register (address 04h) bit description

Bit	Symbol	Description
15 to 9	reserved	-
8	SERRE	**SERR# Enable**: This bit is an enable bit for the SERR# driver. All devices that have an SERR# pin must implement this bit. Address parity errors are reported only if this bit and the PER bit are logic 1. **0 —** Disable the SERR# driver. **1 —** Enable the SERR# driver.
7	SCTRL	**Stepping Control**: This bit controls whether a device does address and data stepping. Devices that never do stepping must clear this bit. Devices that always do stepping must set this bit. Devices that can do either, must make this bit read or write, and initialize it to logic 1 after RST#.
6	PER	**Parity Error Response**: This bit controls the response of a device to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is logic 0, the device sets DPE (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation. The state of this bit after RST# is logic 0. Devices that check parity must implement this bit. Devices are required to generate parity, even if parity checking is disabled.
5	VGAPS	**VGA Palette Snoop**: This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. **0 —** The device must treat palette write accesses like all other accesses. **1 —** Palette snooping is enabled, that is, the device does not respond to palette register writes and snoops data. VGA compatible devices must implement this bit.
4	MWIE	**Memory Write and Invalidate Enable**: This is an enable bit for using the Memory Write and Invalidate command. **0 —** Memory writes must be used instead. State after RST# is logic 0. **1 —** Masters may generate the command. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
3	SC	**Special Cycles**: Controls the action of a device on special cycle operations. **0 —** Causes the device to ignore all special cycle operations. State after RST# is logic 0. **1 —** Allows the device to monitor special cycle operations.
2	BM	**Bus Master**: Controls the ability of a device to act as a master on the PCI bus. **0 —** Disables the device from generating PCI accesses. State after RST# is logic 0. **1 —** Allows the device to behave as a bus master.
1	MS	**Memory Space**: Controls the response of a device to memory space accesses. **0 —** Disables the device response. State after RST# is logic 0. **1 —** Allows the device to respond to memory space accesses.
0	reserved	-

8.2.1.4 Status register

The Status register is a 2-byte read-only register used to record status information on PCI bus-related events. For bit allocation, see Table 8.

Table 8. Status register (address 06h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	DPE	SSE	RMA	RTA	STA	DEVSELT[1:0]		MDPE
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FBBC	reserved	66MC	CL	reserved			
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 9. Status register (address 06h) bit description

Bit	Symbol	Description
15	DPE	**Detected Parity Error**: This bit must be set by the device whenever it detects a parity error, even if the parity error handling is disabled.
14	SSE	**Signaled System Error**: This bit must be set whenever the device asserts SERR#. Devices that never assert SERR# do not need to implement this bit.
13	RMA	**Received Master Abort**: This bit must be set by a master device whenever its transaction, except for special cycle, is terminated with master abort. All master devices must implement this bit.
12	RTA	**Received Target Abort**: This bit must be set by a master device whenever its transaction is terminated with target abort. All master devices must implement this bit.
11	STA	**Signaled Target Abort**: This bit must be set by a target device whenever it terminates a transaction with target abort. Devices that never signal target abort do not need to implement this bit.
10 to 9	DEVSELT [1:0]	**DEVSEL Timing**: These bits encode the timing of DEVSEL#. There are three allowable timing to assert DEVSEL#: **00b —** Fast **01b —** Medium **10b —** Slow **11b —** Reserved These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command, except Configuration Read and Configuration Write.
8	MDPE	**Master Data Parity Error**: This bit is implemented by bus masters. It is set when the following three conditions are met: • The bus agent asserted PERR# itself, on a read; or observed PERR# asserted, on a write. • The agent setting the bit acted as the bus master for the operation in which error occurred. • PER (bit 6 in the Command register) is set.
7	FBBC	**Fast Back-to-Back Capable**: This read-only bit indicates whether the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. Reading this bit will always return 0, meaning that the ISP1568A does not support fast back-to-back transactions.
6	reserved	-
5	66MC	**66 MHz Capable**: This read-only bit indicates whether this device is capable of running at 66 MHz. **0 —** 33 MHz **1 —** 66 MHz
4	CL	**Capabilities List**: This read-only bit indicates whether this device implements the pointer for a new capabilities linked list at offset 34h. **0 —** No new capabilities linked list is available. **1 —** The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities.
3 to 0	reserved	-

8.2.1.5 Revision ID register

This 1-byte read-only register indicates a device-specific revision identifier. The value is chosen by the vendor. This field is a vendor-defined extension of the device ID. The Revision ID register bit description is given in Table 10.

Table 10. REVID - Revision ID register (address 08h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	REVID[7:0]	R	30h*	**Revision ID**: This byte specifies the design revision number of functions.

8.2.1.6 Class Code register

Class Code is a 24-bit read-only register used to identify the generic function of the device, and in some cases, a specific register-level programming interface. Table 11 shows the bit allocation of the register.

The Class Code register is divided into three byte-size fields. The upper byte is a base class code that broadly classifies the type of function the device performs. The middle byte is a sub-class code that identifies more specifically the function of the device. The lower byte identifies a specific register-level programming interface, if any, so that device-independent software can interact with the device.

Table 11. Class Code register (address 09h) bit allocation

Bit	23	22	21	20	19	18	17	16
Symbol	BCC[7:0]							
Reset	0Ch							
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	SCC[7:0]							
Reset	03h							
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RLPI[7:0]							
Reset	X0h[1]							
Access	R	R	R	R	R	R	R	R

[1] X is 1h for OHCI; X is 2h for EHCI.

Table 12. Class Code register (address 09h) bit description

Bit	Symbol	Description
23 to 16	BCC[7:0]	**Base Class Code**: 0Ch is the base class code assigned to this byte. It implies a serial bus controller.
15 to 8	SCC[7:0]	**Sub-Class Code**: 03h is the sub-class code assigned to this byte. It implies the USB host controller.
7 to 0	RLPI[7:0]	**Register-Level Programming Interface**: 10h is the programming interface code assigned to OHCI, which is USB 1.1 specification compliant. 20h is the programming interface code assigned to EHCI, which is USB 2.0 specification compliant.

8.2.1.7 CacheLine Size register

The CacheLine Size register is a read and write single-byte register that specifies the system CacheLine size in units of DWORDs. This register must be implemented by master devices that can generate the Memory Write and Invalidate command. The value in this register is also used by master devices to determine whether to use the Read, Read Line, or Read Multiple command to access the memory.

Slave devices that want to allow memory bursting using CacheLine-wrap addressing mode must implement this register to know when a burst sequence wraps to the beginning of the CacheLine.

This field must be initialized to logic 0 on activation of RST#. Table 13 shows the bit description of the CacheLine Size register.

Table 13. CLS - CacheLine Size register (address 0Ch) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CLS[7:0]	R/W	00h*	**CacheLine Size**: This byte identifies the system CacheLine size. **Remark:** If the SYS_TUNE pin is connected to GND, then the value in this register is disregarded by the ISP1568A and always treated as 01h.

8.2.1.8 Latency Timer register

This register specifies, in units of PCI bus clocks, the value of the latency timer for the PCI bus master. Table 14 shows the bit description of the Latency Timer register.

Table 14. LT - Latency Timer register (address 0Dh) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	LT[7:0]	R/W	00h*	**Latency Timer**: This byte identifies the latency timer.

Remark: It is recommended that you to set the value of the Latency Timer register to 20h.

8.2.1.9 Header Type register

The Header Type register identifies the layout of the second part of the predefined header, beginning at byte 10h in configuration space. It also identifies whether the device contains multiple functions. For bit allocation, see Table 15.

Table 15. Header Type register (address 0Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MFD	HT[6:0]						
Reset	1	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 16. Header Type register (address 0Eh) bit description

Bit	Symbol	Description
7	MFD	**Multi-Function Device**: This bit identifies a multifunction device. **0 —** The device has a single function. **1 —** The device has multiple functions.
6 to 0	HT[6:0]	**Header Type**: These bits identify the layout of the part of the predefined header, beginning at byte 10h in configuration space.

8.2.1.10 Base Address register 0

Power-up software must build a consistent address map before booting the machine to an operating system. This means it must determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, power-up software can map the I/O controllers into reasonable locations and proceed with system boot. To do this mapping in a device-independent manner, base registers for this mapping are placed in the predefined header portion of configuration space.

Bit 0 in all Base Address registers is read-only and used to determine whether the register maps into memory or I/O space. Base Address registers that map to memory space must return logic 0 in bit 0. Base Address registers that map to I/O space must return logic 1 in bit 0.

The bit description of the BAR0 register is given in Table 17.

Table 17. BAR0 - Base Address register 0 (address 10h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	BAR0[31:0]	R/W	0000 0000h*	**Base Address to Memory-Mapped Host Controller Register Space**: The memory size required by OHCI and EHCI are 4 kB and 256 bytes, respectively. Therefore, BAR0[31:12] is assigned to the OHCI port, and BAR0[31:8] is assigned to the EHCI port.

8.2.1.11 Subsystem Vendor ID register

The Subsystem Vendor ID register is used to uniquely identify the expansion board or subsystem where the PCI device resides. This register allows expansion board vendors to distinguish their boards, even though the boards may have the same vendor ID and device ID.

Subsystem vendor IDs are assigned by PCI-SIG to maintain uniqueness. The bit description of the Subsystem Vendor ID register is given in Table 18.

Table 18. SVID - Subsystem Vendor ID register (address 2Ch) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	SVID[15:0]	R	1131h*	**Subsystem Vendor ID**: 1131h is the subsystem vendor ID assigned to ST-Ericsson.

8.2.1.12 Subsystem ID register

Subsystem ID values are vendor specific. The bit description of the Subsystem ID register is given in Table 19.

Table 19. SID - Subsystem ID register (address 2Eh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	SID[15:0]	R	156Xh*[1]	**Subsystem ID**: For the ISP1568A, ST-Ericsson has defined OHCI functions as 1561h, and the EHCI function as 1562h.

[1] X is 1h for OHCI; X is 2h for EHCI.

8.2.1.13 Capabilities Pointer register

This register is used to point to a linked list of new capabilities implemented by the device. This register is only valid if CL (bit 4 in the Status register) is set. If implemented, bit 1 and bit 0 are reserved, and must be set to 00b. Software must mask these bits off before using this register as a pointer in configuration space to the first entry of a linked list of new capabilities. The bit description of the register is given in Table 20.

Table 20. CP - Capabilities Pointer register (address 34h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CP[7:0]	R	DCh*	**Capabilities Pointer**: EHCI efficiently manages power using this register. This Power Management register is allocated at offset DCh. Only one host controller is needed to manage power in the ISP1568A.

8.2.1.14 Interrupt Line register

This is a 1-byte register used to communicate interrupt line routing information. This register must be implemented by any device or device function that uses an interrupt pin. The interrupt allocation is done by the BIOS. The POST software needs to write the routing information to this register because it initializes and configures the system.

The value in this register specifies which input of the system interrupt controller(s) the interrupt pin of the device is connected. This value is used by device drivers and operating systems to determine priority and vector information. Values in this register are system architecture specific. The bit description of the register is given in Table 21.

Table 21. IL - Interrupt Line register (address 3Ch) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	IL[7:0]	R/W	00h*	**Interrupt Line**: Indicates which IRQ is used to report interrupt from the ISP1568A.

8.2.1.15 Interrupt Pin register

This 1-byte register is use to specify which interrupt pin the device or device function uses.

A value of 1h corresponds to INTA#, 2h corresponds to INTB#, 3h corresponds to INTC#, and 4h corresponds to INTD#. Devices or functions that do not use the interrupt pin must set this register to logic 0. The bit description is given in Table 22.

Table 22. IP - Interrupt Pin register (address 3Dh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	IP[7:0]	R	01h*	**Interrupt Pin**: INTA# is the default interrupt pin used by the ISP1568A.

8.2.1.16 Min_Gnt and Max_Lat registers

The Minimum Grant (Min_Gnt) and Maximum Latency (Max_Lat) registers are used to specify the desired settings of the device for latency timer values. For both registers, the value specifies a period of time in units of 250 ns. Logic 0 indicates that the device has no major requirements for setting latency timers.

The Min_Gnt register bit description is given in Table 23.

Table 23. Min_Gnt - Minimum Grant register (address 3Eh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	MIN_GNT[7:0]	R	0Xh*[1]	**Min_Gnt**: It is used to specify how long a burst period the device needs, assuming a clock rate of 33 MHz.

[1] X is 1h for OHCI; X is 2h for EHCI.

The Max_Lat register bit description is given in Table 24.

Table 24. Max_Lat - Maximum Latency register (address 3Fh) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	MAX_LAT[7:0]	R	XXh*[1]	**Max_Lat**: It is used to specify how often the device needs to gain access to the PCI bus.

[1] XX is 2Ah for OHCI; XX is 10h for EHCI.

8.2.1.17 TRDY Timeout register

This is a read and write register at address 40h. The default and recommended value is 00h, TRDY time-out disabled. This value can, however, be modified. It is an implementation-specific register, and not a standard PCI configuration register.

The TRDY timer is 13 bits: the lower 5 bits are fixed as logic 0, and the upper 8 bits are determined by the TRDY Timeout register value. The time-out is calculated by multiplying the 13-bit timer with the PCI CLK cycle time.

This register determines the maximum TRDY delay, without asserting the UE (Unrecoverable Error) bit. If TRDY is longer than the delay determined by this register value, then the UE bit will be set.

8.2.1.18 Retry Timeout register

The default value of this read and write register is 00h, and is located at address 41h. This value can, however, be modified. Programming this register as 00h means that retry time-out is disabled. This is an implementation-specific register, and not a standard PCI configuration register.

The time-out is determined by multiplying the register value with the PCI CLK cycle time. This register determines the maximum number of PCI retires before the UE bit is set. If the number of retries is longer than the delay determined by this register value, then the UE bit will be set.

8.2.2 Enhanced host controller-specific PCI registers

In addition to PCI configuration header registers, EHCI needs some additional PCI configuration space registers to indicate the serial bus release number, downstream port wake-up event capability, and adjust the USB bus frame length for Start-Of-Frame (SOF). The EHCI-specific PCI registers are given in Table 25.

Table 25. EHCI-specific PCI registers

Offset	Register
60h	Serial Bus Release Number (SBRN)
61h	Frame Length Adjustment (FLADJ)
62h to 63h	Port Wake Capability (PORTWAKECAP)

8.2.2.1 SBRN register

The Serial Bus Release Number (SBRN) register is a 1-byte register, and the bit description is given in Table 26. This register contains the release number of the USB specification with which this USB host controller module is compliant.

Table 26. SBRN - Serial Bus Release Number register (address 60h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	SBRN[7:0]	R	20h*	**Serial Bus Specification Release Number**: This register value is to identify *Universal Serial Bus Specification Rev. 2.0*. All other combinations are reserved.

8.2.2.2 FLADJ register

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written to these six bits, the length of the frame is adjusted. The bit allocation of the Frame Length Adjustment (FLADJ) register is given in Table 27.

Table 27. FLADJ - Frame Length Adjustment register (address 61h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]		FLADJ[5:0]					
Reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 28. FLADJ - Frame Length Adjustment register (address 61h) bit description

Bit	Symbol	Description
7 to 6	reserved	-
5 to 0	FLADJ[5:0]	**Frame Length Timing Value**: Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time, number of SOF counter clock periods to generate a SOF microframe length, is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives an SOF cycle time of 60000. See Table 29.

Table 29. FLADJ value vs. SOF cycle time

FLADJ value	SOF cycle time (480 MHz)
0 (00h)	59488
1 (01h)	59504
2 (02h)	59520
:	:
31 (1Fh)	59984
32 (20h)	60000
:	:
62 (3Eh)	60480
63 (3Fh)	60496

8.2.2.3 PORTWAKECAP register

Port Wake Capability (PORTWAKECAP) is a 2-byte register used to establish a policy about which ports are for wake events; see Table 30. Bit positions 15 to 1 in the mask correspond to a physical port implemented on the current EHCI controller. Logic 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect or connect, or overcurrent events as wake-up events. This is an information only mask register. The bits in this register do not affect the actual operation of the EHCI host controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. The system software uses the information in this register when enabling devices and ports for remote wake-up.

Table 30. PORTWAKECAP - Port Wake Capability register (address 62h) bit description
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	PORTWAKECAP[15:0]	R/W	0007h*	**Port Wake-Up Capability Mask**: EHCI does not implement this feature.

8.2.3 Power management registers

Table 31. Power Management registers

Offset	Register
Value read from address 34h + 0h	Capability Identifier (Cap_ID)
Value read from address 34h + 1h	Next Item Pointer (Next_Item_Ptr)
Value read from address 34h + 2h	Power Management Capabilities (PMC)
Value read from address 34h + 4h	Power Management Control/Status (PMCSR)
Value read from address 34h + 6h	Power Management Control/Status PCI-to-PCI Bridge Support Extensions (PMCSR_BSE)
Value read from address 34h + 7h	Data

8.2.3.1 Cap_ID register

The Capability Identifier (Cap_ID) register when read by the system software as 01h indicates that the data structure currently being pointed to is the PCI power management data structure. Each function of a PCI device may have only one item in its capability list with Cap_ID set to 01h. The bit description of the register is given in Table 32.

Table 32. Cap_ID - Capability Identifier register bit description
Address: Value read from address 34h + 0h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CAP_ID[7:0]	R	01h*	**ID**: This field when 01h identifies the linked list item as being PCI power management registers.

8.2.3.2 Next_Item_Ptr register

The Next Item Pointer (Next_Item_Ptr) register describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI configuration space. If the function does not implement any other capabilities defined by the PCI-SIG for inclusion in the capabilities list, or if power management is the last item in the list, then this register must be set to 00h. See Table 33.

Table 33. Next_Item_Ptr - Next Item Pointer register bit description
Address: Value read from address 34h + 1h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	NEXT_ITEM_PTR[7:0]	R	[1]*	**Next Item Pointer**: This field provides an offset into the function's PCI configuration space, pointing to the location of the next item in the function's capability list.

[1] Reset value for OHCI is 00h and for EHCI is E4h.

8.2.3.3 PMC register

The Power Management Capabilities (PMC) register is a 2-byte register, and the bit allocation is given in Table 34. This register provides information on the capabilities of the function related to power management.

Table 34. PMC - Power Management Capabilities register bit allocation
Address: Value read from address 34h + 2h

Bit	15	14	13	12	11	10	9	8
Symbol	PME_S[4:0]					D2_S	D1_S	AUX_C
Reset	1	1	X[1]	1	X[1]	X[1]	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AUX_C[1:0]		DSI	reserved	PMI	VER[2:0]		
Reset	1	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R

[1] X is 0 for OHCI; X is 1 for EHCI.

Table 35. PMC - Power Management Capabilities register bit description

Address: Value read from address 34h + 2h

Bit	Symbol	Description
15 to 11	PME_S [4:0]	**PME Support**: These bits indicate the power states in which the function may assert PME#. Logic 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. **PME_S[0] —** PME# can be asserted from D0 **PME_S[1] —** PME# can be asserted from D1 **PME_S[2] —** PME# can be asserted from D2 **PME_S[3] —** PME# can be asserted from $D3_{hot}$ **PME_S[4] —** PME# can be asserted from $D3_{cold}$
10	D2_S	**D2 Support**: If this bit is logic 1, this function supports the D2 power management state. Functions that do not support D2 must always return logic 0 for this bit.
9	D1_S	**D1 Support**: If this bit is logic 1, this function supports the D1 power management state. Functions that do not support D1 must always return logic 0 for this bit.
8 to 6	AUX_C [2:0]	**Auxiliary Current**: This three-bit field reports the $V_{aux(3V3)}$ auxiliary current requirements for the PCI function. If the Data register is implemented by this function: • A read from this field needs to return a value of 000b. • The Data register takes precedence over this field for $V_{aux(3V3)}$ current requirement reporting. If the PME# generation from $D3_{cold}$ is not supported by the function (PMC[15] = 0), this field must return a value of 000b when read. For functions that support PME# from $D3_{cold}$ and do not implement the Data register, bit assignments corresponding to the maximum current required for $V_{aux(3V3)}$ are: **111b —** 375 mA **110b —** 320 mA **101b —** 270 mA **100b —** 220 mA **011b —** 160 mA **010b —** 100 mA **001b —** 55 mA **000b —** 0 (self powered)
5	DSI	**Device Specific Initialization**: This bit indicates whether special initialization of this function is required, beyond the standard PCI configuration header, before the generic class device driver can use it. This bit is not used by some operating systems. For example, Microsoft Windows and Windows NT do not use this bit to determine whether to use D3. Instead, it is determined using the capabilities of the driver. Logic 1 indicates that the function requires a device-specific initialization sequence, following transition to D0 un-initialized state.
4	reserved	-
3	PMI	**PME Clock**: **0 —** Indicates that no PCI clock is required for the function to generate PME#. **1 —** Indicates that the function relies on the presence of the PCI clock for the PME# operation. Functions that do not support the PME# generation in any state must return logic 0 for this field.
2 to 0	VER[2:0]	**Version**: A value of 010b indicates that this function complies with *PCI Bus Power Management Interface Specification Rev. 1.1*.

8.2.3.4 PMCSR register

The Power Management Control/Status (PMCSR) register is a 2-byte register used to manage the power management state of the PCI function, as well as to allow and monitor Power Management Events (PMEs). The bit allocation of the register is given in Table 36.

Table 36. PMCSR - Power Management Control/Status register bit allocation

Address: Value read from address 34h + 4h

Bit	15	14	13	12	11	10	9	8
Symbol	PMES	DS[1:0]		D_S[3:0]				PMEE
Reset	X[1]	0	0	0	0	0	0	X[1]
Access	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[2]						PS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] Sticky bit, if the function supports PME# from $D3_{cold}$, then X is indeterminate at the time of initial operating system boot; X is 0 if the function does not support PME# from $D3_{cold}$.

[2] The reserved bits must always be written with the reset value.

Table 37. PMCSR - Power Management Control/Status register bit description

Address: Value read from address 34h + 4h

Bit	Symbol	Description
15	PMES	**PME Status**: This bit is set when the function normally asserts the PME# signal independent of the state of the PMEE bit. Writing logic 1 to this bit clears it and causes the function to stop asserting PME#, if enabled. Writing logic 0 has no effect. This bit defaults to logic 0, if the function does not support the PME# generation from $D3_{cold}$. If the function supports the PME# generation from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
14 to 13	DS[1:0]	**Data Scale**: This two-bit read-only field indicates the scaling factor when interpreting the value of the Data register. The value and meaning of this field vary, depending on which data value is selected by the D_S field. This field is a required component of the Data register (offset 7) and must be implemented, if the Data register is implemented. If the Data register is not implemented, this field must return 00b when PMCSR is read.
12 to 9	D_S [3:0]	**Data Select**: This four-bit field selects the data that is reported through the Data register and the D_S field. This field is a required component of the Data register (offset 7) and must be implemented, if the Data register is implemented. If the Data register is not implemented, this field must return 00b when PMCSR is read.

Table 37. PMCSR - Power Management Control/Status register bit description *...continued*
Address: Value read from address 34h + 4h

Bit	Symbol	Description
8	PMEE	**PME Enabled**: Logic 1 allows the function to assert PME#. When it is logic 0, PME# assertion is disabled. This bit defaults to logic 0, if the function does not support the PME# generation from $D3_{cold}$. If the function supports PME# from $D3_{cold}$, then this bit is sticky and must explicitly be cleared by the operating system each time the operating system is initially loaded.
7 to 2	reserved	-
1 to 0	PS[1:0]	**Power State**: This two-bit field is used to determine the current power state of the EHCI function and to set the function into a new power state. The definition of the field values is given as: **00b —** D0 **01b —** D1 **10b —** D2 **11b —** $D3_{hot}$ If the software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, data is discarded and no status change occurs.

8.2.3.5 PMCSR_BSE register

The PMCSR PCI-to-PCI Bridge Support Extensions (PMCSR_BSE) register supports PCI bridge-specific functionality and is required for all PCI-to-PCI bridges. The bit allocation of this register is given in Table 38.

Table 38. PMCSR_BSE - PMCSR PCI-to-PCI Bridge Support Extensions register bit allocation
Address: Value read from address 34h + 6h

Bit	7	6	5	4	3	2	1	0
Symbol	BPCC_EN	B2_B3#	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 39. PMCSR_BSE - PMCSR PCI-to-PCI Bridge Support Extensions register bit description
Address: Value read from address 34h + 6h

Bit	Symbol	Description
7	BPCC_EN	**Bus Power or Clock Control Enable**: **1 —** Indicates that the bus power or clock control mechanism as defined in Table 40 is enabled. **0 —** Indicates that the bus power or control policies as defined in Table 40 are disabled. When the bus power or clock control mechanism is disabled, the bridge's PMCSR Power State (PS) field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6	B2_B3#	**B2 or B3 support for $D3_{hot}$**: The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. **1 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus's PCI clock will be stopped (B2). **0 —** Indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus will have its power removed (B3). This bit is only meaningful if bit 7 (BPCC_EN) is logic 1.
5 to 0	reserved	-

Table 40. PCI bus power and clock control

Originating device's bridge PM state	Secondary bus PM state	Resultant actions by bridge (either direct or indirect)
D0	B0	none
D1	B1	none
D2	B2	clock stopped on secondary bus
$D3_{hot}$	B2, B3	clock stopped and PCI V_{CC} removed from secondary bus (B3 only); for definition of B2_B3#, see Table 39.
$D3_{cold}$	B3	none

8.2.3.6 Data register

The Data register is an optional, 1-byte register that provides a mechanism for the function to report state dependent operating data, such as power consumed or heat dissipated. Table 41 shows the bit description of the register.

Table 41. Data register bit description
Address: Value read from address 34h + 7h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	DATA[7:0]	R	00h*	**DATA**: This register is used to report the state dependent data requested by the D_S field of the PMCSR register. The value of this register is scaled by the value reported by the DS field of the PMCSR register.

8.2.4 VPD register

Table 42. VPD specific registers

Offset	Register
Value read from address 34h + 8h	Vital Product Data Capability Identifier (VPD_Cap_ID)
Value read from address 34h + 9h	Vital Product Data Next Item Pointer (VPD_Next_Item_Ptr)
Value read from address 34h + Ah	Vital Product Data Address (VPD_Addr)
Value read from address 34h + Ch	Vital Product Data Data (VPD_Data)

8.2.4.1 VPD_Cap_ID register

The Capability Identifier (Cap_ID) register when read by the system software as 03h indicates that the data structure currently being pointed to is the VPD_Data structure. The bit description of the register is given in Table 43.

Table 43. VPD_Cap_ID - Vital Product Data Capability Identifier register bit description
Address: Value read from address 34h + 8h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VPD_CAP_ID[7:0]	R	03h*	**VPD Capability ID**: Capability structure ID; for details, refer to Appendix I of *PCI Local Bus Specification Rev. 2.2*

8.2.4.2 VPD_Next_Item_Ptr register

The Next Item Pointer (Next_Item_Ptr) register describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI configuration space. If the function does not implement any other capabilities defined by the PCI-SIG for inclusion in the capabilities list, or if the power management is the last item in the list, then this register must be set to 00h. See Table 44.

Table 44. VPD_Next_Item_Ptr - Vital Product Data Next Item Pointer register bit description
Address: Value read from address 34h + 9h
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VPD_NEXT_ITEM_PTR[7:0]	R	00h*	**VPD Next Item Pointer**: Pointer to the next capability structure, or 00h if this is the last structure in the capability list; for details, refer to Appendix I of *PCI Local Bus Specification Rev. 2.2*

8.2.4.3 VPD_Addr register

The DWORD-aligned byte address of the VPD to be accessed. This is a R/W register, and the initial value at power-up is indeterminate. The bit description of the register is given in Table 45.

Table 45. VPD_Addr - Vital Product Data Address register bit allocation
Address: Value read from address 34h + 9Ah

Bit	7	6	5	4	3	2	1	0
Symbol	F	VPD_ADDR[6:0]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 46. VPD_Addr - Vital Product Data Address register bit description
Address: Value read from address 34h + 9h

Bit	Symbol	Description[1]
7	F	**Flag**: A flag used to indicate when the transfer of data between the VPD Data register and the storage component is completed.
6 to 0	VPD_ADDR[6:0]	**VPD Address**: DWORD-aligned byte address of the VPD to be accessed.

[1] For details on this bits, refer to Appendix I, *PCI Local Bus Specification Rev. 2.2*.

8.2.4.4 VPD_Data register

VPD data can be read or written through this register. The bit description of the register is given in Table 47.

Table 47. VPD_Data - Vital Product Data Data bit description
Address: Value read from address 34h + Ch
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
31 to 0	VPD_DATA[7:0]	R/W	00h*	**VPD Data**: VPD data can be read through this register; for details, refer to Appendix I of *PCI Local Bus Specification Rev. 2.2*

9. I²C-bus interface

A simple I²C-bus interface is provided in the ISP1568A to read customized vendor ID, product ID, and some other configuration bits from an external EEPROM.

The I²C-bus interface is for bidirectional communication between ICs using two serial bus wires: SDA (data) and SCL (clock). Both lines are driven by open-drain circuits and must be connected to the positive supply voltage through pull-up resistors when in use; otherwise, they must be connected to ground.

9.1 Protocol

The I²C-bus protocol defines the following conditions:

- **Bus free**: both SDA and SCL are HIGH
- **START**: a HIGH-to-LOW transition on SDA, while SCL is HIGH
- **STOP**: a LOW-to-HIGH transition on SDA, while SCL is HIGH
- **Data valid**: after a START condition, data on SDA is stable during the HIGH period of SCL; data on SDA may only change while SCL is LOW

Each device on the I²C-bus has a unique slave address, which the master uses to select a device for access.

The master starts a data transfer using a START condition and ends it by generating a STOP condition. Transfers can only be initiated when the bus is free. The receiver must acknowledge each byte by using a LOW level on SDA during the ninth clock pulse on SCL.

For detailed information, refer to *The I²C-bus Specification Version 2.1*.

9.2 Hardware connections

The ISP1568A can be connected to an external EEPROM through the I²C-bus interface. The hardware connections are shown in Figure 7.

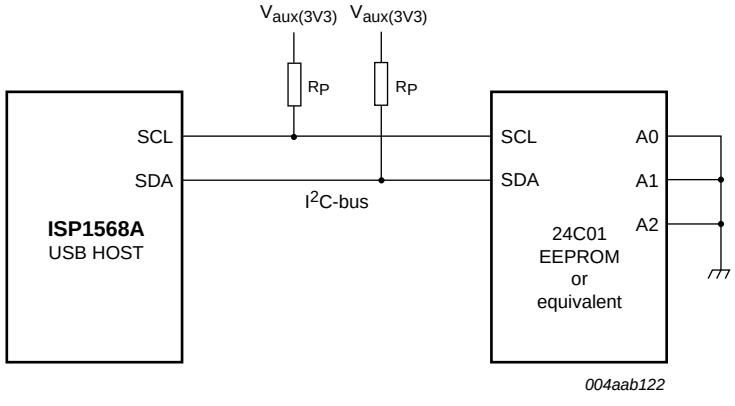
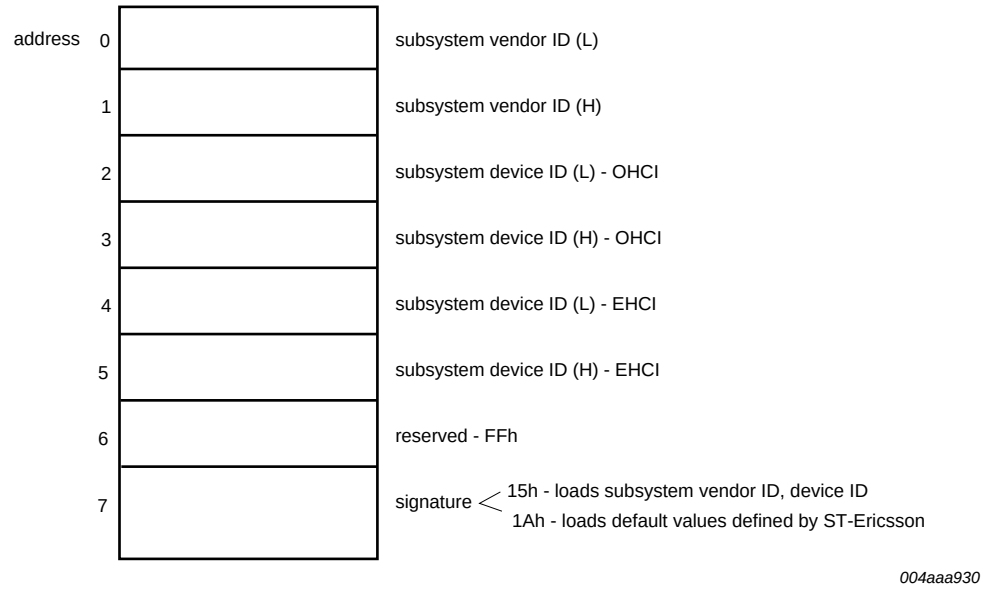


Fig 7. EEPROM connection

The slave address that the ISP1568A uses to access the EEPROM is 101 0000b. Page mode addressing is not supported. Therefore, pins A0, A1, and A2 of the EEPROM must be connected to ground (logic 0).

9.3 Information loading from EEPROM

Figure 8 shows the content of the EEPROM memory. If the EEPROM is not present, the default values of device ID, vendor ID, subsystem VID, and subsystem DID assigned to ST-Ericsson by PCI-SIG will be loaded. For default values, see Table 3.



L = LOW; H = HIGH.

Fig 8. Information loading from EEPROM

9.4 EEPROM programming

To simplify the manufacturing of products based on the ISP1568A, which requires changing of subsystem DID and VID, information can be written in-circuit to the EEPROM through the PCI bus. Reading and writing of the EEPROM is achieved by the mechanism described in Appendix I of *PCI Local Bus Specification Rev. 2.2*.

Remark: The VPD data structure described in Appendix I of *PCI Local Bus Specification Rev. 2.2* is not adopted and only the read write mechanism is adopted in the ISP1568A.

10. Power management

10.1 PCI bus power states

The PCI bus can be characterized by one of the four power management states: B0, B1, B2, and B3.

B0 state (PCI clock = 33 MHz, PCI bus power = on) — This corresponds to the bus being fully operational.

B1 state (PCI clock = intermittent clock operation mode, PCI bus power = on) — When a PCI bus is in B1, PCI V_{CC} is still applied to all devices on the bus. No bus transactions, however, are allowed to take place on the bus. The B1 state indicates a perpetual idle state on the PCI bus.

B2 state (PCI clock = stop, PCI bus power = on) — PCI V_{CC} is still applied on the bus, but the clock is stopped and held in the LOW state.

B3 state (PCI clock = stop, PCI bus power = off) — PCI V_{CC} is removed from all devices on the PCI bus segment.

10.2 USB bus states

Reset state — When the USB bus is in the reset state, the USB system is stopped.

Operational state — When the USB bus is in the active state, the USB system is operating normally.

Suspend state — When the USB bus is in the suspend state, the USB system is stopped.

Resume state — When the USB bus is in the resume state, the USB system is operating normally.

11. USB host controller registers

Each host controller contains a set of on-chip operational registers that are mapped to un-cached memory of the system addressable space. This memory space must begin on a DWORD (32-bit) boundary. The size of the allocated space is defined by the initial value in the Base Address register 0. HCDs must interact with these registers to implement USB functionality.

After the PCI enumeration driver finishes the PCI device configuration, the new base address of these memory-mapped operational registers is defined in BAR0. The HCD can access these registers by using the address of base address value + offset.

Table 48 contains a list of host controller registers.

For the OHCI host controller, there are only operational registers for the USB operation.

For the enhanced host controller, there are two types of registers: one set of read-only capability registers, and one set of read and write operational registers.

Table 48. USB host controller registers

Address	OHCI register	Reset value func0 OHCI[1]	EHCI register	Reset value func1 EHCI[1]
00h	HcRevision	0000 0**010**h	CAPLENGTH/HCIVERSION[2]	**0100 0020**h
04h	HcControl	0000 0000h	HCSPARAMS	**0000 1292**h
08h	HcCommandStatus	0000 0000h	HCCPARAMS	**0000 0012**h
0Ch	HcInterruptStatus	0000 0000h	HCSP-PORTROUTE1[31:0]	**0000 1010**h
10h	HcInterruptEnable	0000 0000h	HCSP-PORTROUTE2[59:32]	**0000 0000**h
14h	HcInterruptDisable	0000 0000h	reserved	-
18h	HcHCCA	0000 0000h	reserved	-
1Ch	HcPeriodCurrentED	0000 0000h	reserved	-
20h	HcControlHeadED	0000 0000h	USBCMD	0008 0000h
24h	HcControlCurrentED	0000 0000h	USBSTS	0000 1000h
28h	HcBulkHeadED	0000 0000h	USBINTR	0000 0000h
2Ch	HcBulkCurrentED	0000 0000h	FRINDEX	0000 0000h
30h	HcDoneHead	0000 0000h	reserved	-
34h	HcFmInterval	0000 2EDFh	PERIODICLISTBASE	0000 0000h
38h	HcFmRemaining	0000 0000h	ASYNCLISTADDR	0000 0000h
3Ch	HcFmNumber	0000 0000h	reserved	-
40h	HcPeriodicStart	0000 0000h	reserved	-
44h	HcLSThreshold	0000 0628h	reserved	-
48h	HcRhDescriptorA	**FF00 0902**h	reserved	-
4Ch	HcRhDescriptorB	0006 0000h	reserved	-
50h	HcRhStatus	0000 0000h	reserved	-
54h	HcRhPortStatus[1]	0000 0000h	reserved	-
58h	HcRhPortStatus[2]	0000 0000h	reserved	-
5Ch	reserved	-	reserved	-
60h	reserved	-	CONFIGFLAG	0000 0000h

Table 48. USB host controller registers *...continued*

Address	OHCI register	Reset value func0 OHCI[1]	EHCI register	Reset value func1 EHCI[1]
64h	reserved	-	PORTSC1	0000 0000h
68h	reserved	-	PORTSC2	0000 0000h
6Ch	reserved	-	System Tuning	0000 0003h
70h	reserved	-	reserved	-

[1] Reset values that are highlighted, for example, **0**, are the ISP1568A implementation-specific reset values; and reset values that are not highlighted, for example, 0, are compliant with the OHCI and EHCI specifications.

[2] HCIVERSION is 0100h when subsystem ID and subsystem vendor ID are configured through the external EEPROM or when SCL is pulled down. Otherwise, it is 0095h.

11.1 OHCI USB host controller operational registers

OHCI HCDs must communicate with these registers to implement USB data transfers. Based on their functions, these registers are classified into four partitions:

- Control and status
- Memory pointer
- Frame counter
- Root hub

11.1.1 HcRevision register

Table 49. HcRevision - Host Controller Revision register bit allocation
Address: Content of the base address register + 00h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	REV[7:0]							
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 50. HcRevision - Host Controller Revision register bit description
Address: Content of the base address register + 00h

Bit	Symbol	Description
31 to 8	reserved	-
7 to 0	REV[7:0]	**Revision**: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this host controller. For example, a value of 11h corresponds to version 1.1. All of the host controller implementations that are compliant with this specification must have a value of 10h.

11.1.2 HcControl register

This register defines the operating modes for the host controller. All the fields in this register, except HCFS and RWC, are modified only by the HCD. The bit allocation is given in Table 51.

Table 51. HcControl - Host Controller Control register bit allocation
Address: Content of the base address register + 04h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]					RWE	RWC	IR
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	HCFS[1:0]		BLE	CLE	IE	PLE	CBSR[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 52. HcControl - Host Controller Control register bit description

Address: Content of the base address register + 04h

Bit	Symbol	Description
31 to 11	reserved	-
10	RWE	**Remote Wake-up Enable**: This bit is used by the HCD to enable or disable the remote wake-up feature on detecting upstream resume signaling. When this bit and RD (bit 3) in the HcInterruptStatus register are set, a remote wake-up is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	RWC	**Remote Wake-up Connected**: This bit indicates whether the host controller supports remote wake-up signaling. If remote wake-up is supported and used by the system, it is the responsibility of the system firmware to set this bit during POST. The host controller clears the bit on a hardware reset but does not alter it on a software reset. Remote wake-up signaling of the host system is host-bus-specific and is not described in this specification.
8	IR	**Interrupt Routing**: This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the system management interrupt. The HCD clears this bit on a hardware reset, but it does not alter this bit on a software reset. The HCD uses this bit as a tag to indicate the ownership of the host controller.
7 to 6	HCFS [1:0]	**Host Controller Functional State** for USB: **00b —** USBRESET **01b —** USBRESUME **10b —** USBOPERATIONAL **11b —** USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. The HCD may determine whether the host controller has begun sending SOFs by reading SF (bit 2) in HcInterruptStatus. This field may be changed by the host controller only when in the USBSUSPEND state. The host controller may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. The host controller enters USBSUSPEND after a software reset; it enters USBRESET after a hardware reset. The latter also resets the root hub and asserts subsequent reset signaling to downstream ports.
5	BLE	**Bulk List Enable**: This bit is set to enable the processing of the bulk list in the next frame. If cleared by the HCD, processing of the bulk list does not occur after the next SOF. The host controller checks this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcBulkCurrentED is pointing to an Endpoint Descriptor (ED) to be removed, the HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

Table 52. HcControl - Host Controller Control register bit description *…continued*
Address: Content of the base address register + 04h

Bit	Symbol	Description
4	CLE	**Control List Enable**: This bit is set to enable the processing of the control list in the next frame. If cleared by the HCD, processing of the control list does not occur after the next SOF. The host controller must check this bit whenever it wants to process the list. When disabled, the HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, the HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	IE	**Isochronous Enable**: This bit is used by the HCD to enable or disable processing of isochronous EDs. While processing the periodic list in a frame, the host controller checks the status of this bit when it finds an isochronous ED (F = 1). If set (enabled), the host controller continues processing EDs. If cleared (disabled), the host controller halts processing of the periodic list, which now contains only isochronous EDs, and begins processing bulk or control lists. Setting this bit is guaranteed to take effect in the next frame and not the current frame.
2	PLE	**Periodic List Enable**: This bit is set to enable the processing of the periodic list in the next frame. If cleared by the HCD, processing of the periodic list does not occur after the next SOF. The host controller must check this bit before it starts processing the list.
1 to 0	CBSR [1:0]	**Control Bulk Service Ratio**: This specifies the service ratio of control EDs over bulk EDs. Before processing any of the nonperiodic lists, the host controller must compare the ratio specified with its internal count on how many nonempty control EDs are processed, in determining whether to continue serving another control ED or switching to bulk EDs. The internal count must be retained when crossing the frame boundary. After a reset, the HCD is responsible to restore this value. **00b —** 1 : 1 **01b —** 2 : 1 **10b —** 3 : 1 **11b —** 4 : 1

11.1.3 HcCommandStatus register

The HcCommandStatus register is used by the host controller to receive commands issued by the HCD. It also reflects the current status of the host controller. To the HCD, it appears as a ‘write to set’ register. The host controller must ensure that bits written as logic 1 become set in the register while bits written as logic 0 remain unchanged in the register. The HCD may issue multiple distinct commands to the host controller without concern for corrupting previously issued commands. The HCD has normal read access to all bits.

The SOC[1:0] field (bits 17 and 16 in the HcCommandStatus register) indicates the number of frames with which the host controller has detected the scheduling overrun error. This occurs when the periodic list does not complete before EOF. When a scheduling overrun error is detected, the host controller increments the counter and sets SO (bit 0 in the HcInterruptStatus register).

Table 53 shows the bit allocation of the HcCommandStatus register.

Table 53. HcCommandStatus - Host Controller Command Status register bit allocation
Address: Content of the base address register + 08h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]						SOC[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]				OCR	BLF	CLF	HCR
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 54. HcCommandStatus - Host Controller Command Status register bit description
Address: Content of the base address register + 08h

Bit	Symbol	Description
31 to 18	reserved	-
17 to 16	SOC[1:0]	**Scheduling Overrun Count**: The bit is incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. It must be incremented when a scheduling overrun is detected, even if SO (bit 0 in HcInterruptStatus) is already set. This is used by the HCD to monitor any persistent scheduling problems.
15 to 4	reserved	-
3	OCR	**Ownership Change Request**: This bit is set by an OS HCD to request a change of control of the host controller. When set, the host controller must set OC (bit 30 in HcInterruptStatus). After the changeover, this bit is cleared and remains so until the next request from the OS HCD.

Table 54. HcCommandStatus - Host Controller Command Status register bit description *...continued*

Address: Content of the base address register + 08h

Bit	Symbol	Description
2	BLF	**Bulk List Filled**: This bit is used to indicate whether there are any Transfer Descriptors (TDs) on the bulk list. It is set by the HCD whenever it adds a TD to an ED in the bulk list. When the host controller begins to process the head of the bulk list, it checks Bulk-Filled (BF). If BLF is logic 0, the host controller does not need to process the bulk list. If BLF is logic 1, the host controller must start processing the bulk list and set BF to logic 0. If the host controller finds a TD on the list, then the host controller must set BLF to logic 1, causing the bulk list processing to continue. If no TD is found on the bulk list, and if the HCD does not set BLF, then BLF is still logic 0 when the host controller completes processing the bulk list and the bulk list processing stops.
1	CLF	**Control List Filled**: This bit is used to indicate whether there are any TDs on the control list. It is set by the HCD whenever it adds a TD to an ED in the control list. When the host controller begins to process the head of the control list, it checks CLF. If CLF is logic 0, the host controller does not need to process the control list. If Control-Filled (CF) is logic 1, the host controller needs to start processing the control list and set CLF to logic 0. If the host controller finds a TD on the list, then the host controller must set CLF to logic 1, causing the control list processing to continue. If no TD is found on the control list, and if the HCD does not set CLF, then CLF is still logic 0 when the host controller completes processing the control list and the control list processing stops.
0	HCR	**Host Controller Reset**: This bit is set by the HCD to initiate a software reset of the host controller. Regardless of the functional state of the host controller, it moves to the USBSUSPEND state in which most of the operational registers are reset, except those stated otherwise; for example, IR (bit 8) in the HcControl register, and no host bus accesses are allowed. This bit is cleared by the host controller on completing the reset operation. The reset operation must be completed within 10 μs. This bit, when set, must not cause a reset to the root hub and no subsequent reset signaling must be asserted to its downstream ports.

11.1.4 HcInterruptStatus register

This is a 4-byte register that provides the status of the events that cause hardware interrupts. The bit allocation of the register is given in Table 55. When an event occurs, the host controller sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated, if the interrupt is enabled in the HcInterruptEnable register (see Table 57) and the MIE (Master Interrupt Enable) bit is set. The HCD may clear specific bits in this register by writing logic 1 to the bit positions to be cleared. The HCD may not set any of these bits. The host controller does not clear the bit.

Table 55. HcInterruptStatus - Host Controller Interrupt Status register bit allocation

Address: Content of the base address register + 0Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 56. HcInterruptStatus - Host Controller Interrupt Status register bit description
Address: Content of the base address register + 0Ch

Bit	Symbol	Description
31	reserved	-
30	OC	**Ownership Change**: This bit is set by the host controller when HCD sets OCR (bit 3) in the HcCommandStatus register. This event, when unmasked, will always immediately generate a System Management Interrupt (SMI). This bit is forced to logic 0 when the SMI# pin is not implemented.
29 to 7	reserved	-
6	RHSC	**Root Hub Status Change**: This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	FNO	**Frame Number Overflow**: This bit is set when the Most Significant Bit (MSB) of HcFmNumber (bit 15) changes value, or after HccaFrameNumber is updated.
4	UE	**Unrecoverable Error**: This bit is set when the host controller detects a system error not related to USB. The host controller must not proceed with any processing or signaling before the system error is corrected. The HCD clears this bit after the host controller is reset.
3	RD	**Resume Detected**: This bit is set when the host controller detects that a device on the USB is asserting resume signaling. This bit is set by the transition from no resume signaling to resume signaling. This bit is not set when the HCD sets the USBRESUME state.
2	SF	**Start-of-Frame**: At the start of each frame, this bit is set by the host controller and an SOF token is generated at the same time.
1	WDH	**Write-back Done Head**: This bit is immediately set after the host controller has written HcDoneHead to HccaDoneHead. Further, updates of HccaDoneHead occur only after this bit is cleared. The HCD must only clear this bit after it has saved the content of HccaDoneHead.
0	SO	**Scheduling Overrun**: This bit is set when USB schedules for current frame overruns and after the update of HccaFrameNumber. A scheduling overrun increments the SOC[1:0] field (bits 17 to 16 of HcCommandStatus).

11.1.5 HcInterruptEnable register

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt. A hardware interrupt is requested on the host bus if the following conditions occur:

- A bit is set in the HcInterruptStatus register.
- The corresponding bit in the HcInterruptEnable register is set.
- The MIE (Master Interrupt Enable) bit is set.

Writing logic 1 to a bit in this register sets the corresponding bit, whereas writing logic 0 to a bit in this register leaves the corresponding bit unchanged. On a read, the current value of this register is returned. The bit allocation is given in Table 57.

Table 57. HcInterruptEnable - Host Controller Interrupt Enable register bit allocation
Address: Content of the base address register + 10h

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 58. HcInterruptEnable - Host Controller Interrupt Enable register bit description
Address: Content of the base address register + 10h

Bit	Symbol	Description
31	MIE	**Master Interrupt Enable**: **0 —** Ignore **1 —** Enables interrupt generation by events specified in other bits of this register.
30	OC	**Ownership Change**: **0 —** Ignore **1 —** Enables interrupt generation because of ownership change.
29 to 7	reserved	-
6	RHSC	**Root Hub Status Change**: **0 —** Ignore **1 —** Enables interrupt generation because of root hub status change.
5	FNO	**Frame Number Overflow**: **0 —** Ignore **1 —** Enables interrupt generation because of frame number overflow.
4	UE	**Unrecoverable Error**: **0 —** Ignore **1 —** Enables interrupt generation because of unrecoverable error.
3	RD	**Resume Detect**: **0 —** Ignore **1 —** Enables interrupt generation because of resume detect.

Table 58. HcInterruptEnable - Host Controller Interrupt Enable register bit description *...continued*
Address: Content of the base address register + 10h

Bit	Symbol	Description
2	SF	**Start-of-Frame**: **0 —** Ignore **1 —** Enables interrupt generation because of Start-of-Frame.
1	WDH	**HcDoneHead Write-back**: **0 —** Ignore **1 —** Enables interrupt generation because of HcDoneHead write-back.
0	SO	**Scheduling Overrun**: **0 —** Ignore **1 —** Enables interrupt generation because of scheduling overrun.

11.1.6 HcInterruptDisable register

Each disable bit in the HcInterruptDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Therefore, writing logic 1 to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing logic 0 to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On a read, the current value of the HcInterruptEnable register is returned.

The register contains 4 bytes, and the bit allocation is given in Table 59.

Table 59. HcInterruptDisable - Host Controller Interrupt Disable register bit allocation
Address: Content of the base address register + 14h

Bit	31	30	29	28	27	26	25	24
Symbol	MIE	OC	reserved[1]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]	RHSC	FNO	UE	RD	SF	WDH	SO
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 60. HcInterruptDisable - Host Controller Interrupt Disable register bit description
Address: Content of the base address register + 14h

Bit	Symbol	Description
31	MIE	**Master Interrupt Enable**: **0 —** Ignore **1 —** Disables interrupt generation because of events specified in other bits of this register. This field is set after a hardware or software reset. Interrupts are disabled.
30	OC	**Ownership Change**: **0 —** Ignore **1 —** Disables interrupt generation because of ownership change.
29 to 7	reserved	-
6	RHSC	**Root Hub Status Change**: **0 —** Ignore **1 —** Disables interrupt generation because of root hub status change.
5	FNO	**Frame Number Overflow**: **0 —** Ignore **1 —** Disables interrupt generation because of frame number overflow.
4	UE	**Unrecoverable Error**: **0 —** Ignore **1 —** Disables interrupt generation because of unrecoverable error.
3	RD	**Resume Detect**: **0 —** Ignore **1 —** Disables interrupt generation because of resume detect.
2	SF	**Start-of-Frame**: **0 —** Ignore **1 —** Disables interrupt generation because of Start-of-Frame.
1	WDH	**HcDoneHead Write-back**: **0 —** Ignore **1 —** Disables interrupt generation because of HcDoneHead write-back.
0	SO	**Scheduling Overrun**: **0 —** Ignore **1 —** Disables interrupt generation because of scheduling overrun.

11.1.7 HcHCCA register

The HcHCCA register contains the physical address of Host Controller Communication Area (HCCA). The bit allocation is given in Table 61. The HCD determines alignment restrictions by writing all 1s to HcHCCA and reading the content of HcHCCA. The alignment is evaluated by examining the number of zeroes in lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 will always return logic 0 when read. This area is used to hold control structures and the interrupt table that are accessed by both the host controller and the HCD.

Table 61. HcHCCA - Host Controller Communication Area register bit allocation
Address: Content of the base address register + 18h

Bit	31	30	29	28	27	26	25	24
Symbol	HCCA[23:16]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	HCCA[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	HCCA[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 62. HcHCCA - Host Controller Communication Area register bit description
Address: Content of the base address register + 18h

Bit	Symbol	Description
31 to 8	HCCA[23:0]	**Host Controller Communication Area Base Address**: This is the base address of the HCCA.
7 to 0	reserved	-

11.1.8 HcPeriodCurrentED register

The HcPeriodCurrentED register contains the physical address of the current isochronous or interrupt ED. Table 63 shows the bit allocation of the register.

Table 63. HcPeriodCurrentED - Host Controller Period Current Endpoint Descriptor register bit allocation
Address: Content of the base address register + 1Ch

Bit	31	30	29	28	27	26	25	24
Symbol	PCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	23	22	21	20	19	18	17	16
Symbol	PCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	15	14	13	12	11	10	9	8
Symbol	PCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Symbol	PCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 64. HcPeriodCurrentED - Host Controller Period Current Endpoint Descriptor register bit description
Address: Content of the base address register + 1Ch

Bit	Symbol	Description
31 to 4	PCED[27:0]	**Period Current ED**: This is used by the host controller to point to the head of one of the periodic lists that must be processed in the current frame. The content of this register is updated by the host controller after a periodic ED is processed. The HCD may read the content in determining which ED is being processed at the time of reading.
3 to 0	reserved	-

11.1.9 HcControlHeadED register

The HcControlHeadED register contains the physical address of the first ED of the control list. The bit allocation is given in Table 65.

Table 65. HcControlHeadED - Host Controller Control Head Endpoint Descriptor register bit allocation
Address: Content of the base address register + 20h

Bit	31	30	29	28	27	26	25	24
Symbol	CHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CHED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 66. HcControlHeadED - Host Controller Control Head Endpoint Descriptor register bit description
Address: Content of the base address register + 20h

Bit	Symbol	Description
31 to 4	CHED[27:0]	**Control Head ED**: The host controller traverses the control list, starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of the host controller.
3 to 0	reserved	-

11.1.10 HcControlCurrentED register

The HcControlCurrentED register contains the physical address of the current ED of the control list. The bit allocation is given in Table 67.

Table 67. HcControlCurrentED - Host Controller Control Current Endpoint Descriptor register bit allocation
Address: Content of the base address register + 24h

Bit	31	30	29	28	27	26	25	24
Symbol	CCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	CCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	CCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CCED[3:0]				reserved			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 68. HcControlCurrentED - Host Controller Control Current Endpoint Descriptor register bit description
Address: Content of the base address register + 24h

Bit	Symbol	Description
31 to 4	CCED[27:0]	**Control Current ED**: This pointer is advanced to the next ED after serving the present. The host controller must continue processing the list from where it left in the last frame. When it reaches the end of the control list, the host controller checks CLF (bit 1 of HcCommandStatus). If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. The HCD is allowed to modify this register only when CLE (bit 4 in the HcControl register) is cleared. When set, the HCD only reads the instantaneous value of this register. Initially, this is set to logic 0 to indicate the end of the control list.
3 to 0	reserved	-

11.1.11 HcBulkHeadED register

This register (see Table 69) contains the physical address of the first ED of the bulk list.

Table 69. HcBulkHeadED - Host Controller Bulk Head Endpoint Descriptor register bit allocation
Address: Content of the base address register + 28h

Bit	31	30	29	28	27	26	25	24
Symbol	BHED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	BHED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BHED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BHED[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 70. HcBulkHeadED - Host Controller Bulk Head Endpoint Descriptor register bit description
Address: Content of the base address register + 28h

Bit	Symbol	Description
31 to 4	BHED[27:0]	**Bulk Head ED**: The host controller traverses the bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of the host controller.
3 to 0	reserved	-

11.1.12 HcBulkCurrentED register

This register contains the physical address of the current endpoint of the bulk list. The endpoints are ordered according to their insertion to the list because the bulk list must be served in a round-robin fashion.

The bit allocation is given in Table 71.

Table 71. HcBulkCurrentED - Host Controller Bulk Current Endpoint Descriptor register bit allocation
Address: Content of the base address register + 2Ch

Bit	31	30	29	28	27	26	25	24
Symbol	BCED[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	BCED[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	BCED[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	BCED[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 72. HcBulkCurrentED - Host Controller Bulk Current Endpoint Descriptor register bit description
Address: Content of the base address register + 2Ch

Bit	Symbol	Description
31 to 4	BCED[27:0]	**Bulk Current ED**: This is advanced to the next ED after the host controller has served the current ED. The host controller continues processing the list from where it left off in the last frame. When it reaches the end of the bulk list, the host controller checks CLF (bit 1 of HcCommandStatus). If the CLF bit is not set, nothing is done. If the CLF bit is set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the CLF bit. The HCD can modify this register only when BLE (bit 5 in the HcControl register) is cleared. When HcControl is set, the HCD reads the instantaneous value of this register. This is initially set to logic 0 to indicate the end of the bulk list.
3 to 0	reserved	-

11.1.13 HcDoneHead register

The HcDoneHead register contains the physical address of the last completed TD that was added to the done queue. In a normal operation, the HCD need not read this register because its content is periodically written to the HCCA. Table 73 contains the bit allocation of the register.

Table 73. HcDoneHead - Host Controller Done Head register bit allocation
Address: Content of the base address register + 30h

Bit	31	30	29	28	27	26	25	24
Symbol	DH[27:20]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	DH[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DH[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DH[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 74. HcDoneHead - Host Controller Done Head register bit description

Address: Content of the base address register + 30h

Bit	Symbol	Description
31 to 4	DH[27:0]	**Done Head**: When a TD is completed, the host controller writes the content of HcDoneHead to the NextTD field of the TD. The host controller then overwrites the content of HcDoneHead with the address of this TD. This is set to logic 0 whenever the host controller writes the content of this register to HCCA.
3 to 0	reserved	-

11.1.14 HcFmInterval register

This register contains a 14-bit value that indicates the bit time interval in a frame, that is, between two consecutive SOFs, and a 15-bit value indicating the full-speed maximum packet size that the host controller may transmit or receive, without causing a scheduling overrun. The HCD may carry out minor adjustment on FI (Frame Interval) by writing a new value over the present at each SOF. This provides the possibility for the host controller to synchronize with an external clocking resource and to adjust any unknown local clock offset. The bit allocation of the register is given in Table 75.

Table 75. HcFmInterval - Host Controller Frame Interval register bit allocation

Address: Content of the base address register + 34h

Bit	31	30	29	28	27	26	25	24
Symbol	FIT	FSMPS[14:8]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	FSMPS[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		FI[13:8]					
Reset	0	0	1	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FI[7:0]							
Reset	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 76. HcFmInterval - Host Controller Frame Interval register bit description
Address: Content of the base address register + 34h

Bit	Symbol	Description
31	FIT	**Frame Interval Toggle**: The HCD toggles this bit whenever it loads a new value to Frame Interval.
30 to 16	FSMPS[14:0]	**FS Largest Data Packet**: This field specifies the value that is loaded into the largest data packet counter at the beginning of each frame. The counter value represents the largest amount of data in bits that can be sent or received by the host controller in a single transaction at any given time, without causing a scheduling overrun. The field value is calculated by the HCD.
15 to 14	reserved	-
13 to 0	FI[13:0]	**Frame Interval**: This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to 11,999. The HCD must store the current value of this field before resetting the host controller to reset this field to its nominal value. The HCD can then restore the stored value on completing the reset sequence.

11.1.15 HcFmRemaining register

This register is a 14-bit down counter showing the bit time remaining in the current frame. Table 77 contains the bit allocation of this register.

Table 77. HcFmRemaining - Host Controller Frame Remaining register bit allocation
Address: Content of the base address register + 38h

Bit	31	30	29	28	27	26	25	24
Symbol	FRT	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		FR[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 78. HcFmRemaining - Host Controller Frame Remaining register bit description
Address: Content of the base address register + 38h

Bit	Symbol	Description
31	FRT	**Frame Remaining Toggle**: This bit is loaded from FIT (bit 31 of HcFmInterval) whenever FR[13:0] reaches 0. This bit is used by the HCD for the synchronization between FI[13:0] (bits 13 to 0 of HcFmInterval) and FR[13:0].
30 to 14	reserved	-
13 to 0	FR[13:0]	**Frame Remaining**: This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FI[13:0] value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, the host controller reloads the content with FI[13:0] of HcFmInterval and uses the updated value from the next SOF.

11.1.16 HcFmNumber register

This register is a 16-bit counter, and the bit allocation is given in Table 79. It provides a timing reference among events happening in the host controller and the HCD. The HCD may use the 16-bit value specified in this register and generate a 32-bit frame number, without requiring frequent access to the register.

Table 79. HcFmNumber - Host Controller Frame Number register bit allocation
Address: Content of the base address register + 3Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		FN[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 80. HcFmNumber - Host Controller Frame Number register bit description
Address: Content of the base address register + 3Ch

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	FN[13:0]	**Frame Number**: Incremented when HcFmRemaining is reloaded. It must be rolled over to 0h after FFFFh. Automatically incremented when entering the USBOPERATIONAL state. The content is written to HCCA after the host controller has incremented Frame Number at each frame boundary and sent an SOF but before the host controller reads the first ED in that frame. After writing to HCCA, the host controller sets SF (bit 2 in HcInterruptStatus).

11.1.17 HcPeriodicStart register

This register has a 14-bit programmable value that determines when is the earliest time for the host controller to start processing the periodic list. For bit allocation, see Table 81.

Table 81. HcPeriodicStart - Host Controller Periodic Start register bit allocation
Address: Content of the base address register + 40h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		P_S[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	P_S[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 82. HcPeriodicStart - Host Controller Periodic Start register bit description
Address: Content of the base address register + 40h

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	P_S[13:0]	**Periodic Start**: After a hardware reset, this field is cleared. It is then set by the HCD during the host controller initialization. The value is roughly calculated as 10% of HcFmInterval. A typical value is 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists have priority over control or bulk processing. The host controller, therefore, starts processing the interrupt list after completing the current control or bulk transaction that is in progress.

11.1.18 HcLSThreshold register

This register contains an 11-bit value used by the host controller to determine whether to commit to the transfer of a maximum of 8-byte low-speed packet before EOF. Neither the host controller nor the HCD can change this value. For bit allocation, see Table 83.

Table 83. HcLSThreshold - Host Controller Low-Speed Threshold register bit allocation
Address: Content of the base address register + 44h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]				LST[11:8]			
Reset	0	0	0	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LST[7:0]							
Reset	0	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 84. HcLSThreshold - Host Controller Low-Speed Threshold register bit description
Address: Content of the base address register + 44h

Bit	Symbol	Description
31 to 12	reserved	-
11 to 0	LST[11:0]	**LS Threshold**: This field contains a value that is compared to the FR[13:0] field, before initiating a low-speed transaction. The transaction is started only if FR ≥ this field. The value is calculated by the HCD, considering the transmission and set-up overhead.

11.1.19 HcRhDescriptorA register

This register is the first of two registers describing the characteristics of the root hub. Reset values are implementation-specific.

Table 85 contains the bit allocation of the HcRhDescriptorA register.

Table 85. HcRhDescriptorA - Host Controller Root Hub Descriptor A register bit allocation
Address: Content of the base address register + 48h

Bit	31	30	29	28	27	26	25	24
Symbol	POTPGT[7:0]							
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]			NOCP	OCPM	DT	NPS	PSM
Reset	0	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	NDP[7:0]							
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R

[1] The reserved bits must always be written with the reset value.

Table 86. HcRhDescriptorA - Host Controller Root Hub Descriptor A register bit description
Address: Content of the base address register + 48h

Bit	Symbol	Description
31 to 24	POTPGT [7:0]	**Power On To Power Good Time**: This byte specifies the duration the HCD must wait before accessing a powered-on port of the root hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT × 2 ms.
23 to 13	reserved	-
12	NOCP	**No Overcurrent Protection**: This bit describes how the overcurrent status for root hub ports are reported. When this bit is cleared, the OCPM bit specifies global or per-port reporting. **0 —** Overcurrent status is collectively reported for all downstream ports. **1 —** No overcurrent protection supported.
11	OCPM	**Overcurrent Protection Mode**: This bit describes how the overcurrent status for root hub ports are reported. At reset, this fields reflects the same mode as Power Switching Mode. This field is valid only if the NOCP bit is cleared. **0 —** Overcurrent status is collectively reported for all downstream ports. **1 —** Overcurrent status is reported on a per-port basis.
10	DT	**Device Type**: This bit specifies that the root hub is not a compound device. The root hub is not permitted to be a compound device. This field must always read logic 0.
9	NPS	**No Power Switching**: This bit is used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PSM bit specifies global or per-port switching. **0 —** Ports are power switched. **1 —** Ports are always powered on when the host controller is powered on.
8	PSM	**Power Switching Mode**: This bit is used to specify how the power switching of root hub ports is controlled. It is implementation-specific. This field is only valid if the NPS field is cleared. **0 —** All ports are powered at the same time. **1 —** Each port is individually powered. This mode allows port power to be controlled by either the global switch or per-port switching. If the PPCM (Port Power Control Mask) bit is set, the port responds only to port power commands (Set/Clear Port Power). If the port mask is cleared, then the port is controlled only by the global power switch (Set/Clear Global Power).
7 to 0	NDP[7:0]	**Number Downstream Ports**: These bits specify the number of downstream ports supported by the root hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OHCI is 15.

11.1.20 HcRhDescriptorB register

The HcRhDescriptorB register is the second of two registers describing the characteristics of the root hub. The bit allocation is given in Table 87. These fields are written during initialization to correspond to the system implementation. Reset values are implementation-specific.

Table 87. HcRhDescriptorB - Host Controller Root Hub Descriptor B register bit allocation
Address: Content of the base address register + 4Ch

Bit	31	30	29	28	27	26	25	24
Symbol	PPCM[15:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	PPCM[7:0]							
Reset	0	0	0	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DR[15:8]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DR[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 88. HcRhDescriptorB - Host Controller Root Hub Descriptor B register bit description
Address: Content of the base address register + 4Ch

Bit	Symbol	Description
31 to 16	PPCM[15:0]	**Port Power Control Mask**: Each bit indicates whether a port is affected by a global power control command when Power Switching Mode is set. When set, only the power state of the port is affected by per-port power control (Set/Clear Port Power). When cleared, the port is controlled by the global power switch (Set/Clear Global Power). If the device is configured to global switching mode (Power Switching Mode = 0), this field is not valid. **Bit 0 —** Reserved **Bit 1 —** Ganged-power mask on port 1 **Bit 2 —** Ganged-power mask on port 2
15 to 0	DR[15:0]	**Device Removable**: Each bit is dedicated to a port of the root hub. When cleared, the attached device is removable. When set, the attached device is not removable. **Bit 0 —** Reserved **Bit 1 —** Device attached to port 1 **Bit 2 —** Device attached to port 2

11.1.21 HcRhStatus register

This register is divided into two parts. The lower word of a DWORD represents the Hub Status field, and the upper word represents the Hub Status Change field. Reserved bits must always be written as logic 0. Table 89 shows the bit allocation of the register.

Table 89. HcRhStatus - Host Controller Root Hub Status register bit allocation
Address: Content of the base address register + 50h

Bit	31	30	29	28	27	26	25	24
Symbol	CRWE	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]						CCIC	LPSC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	DRWE	reserved[1]						
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]						OCI	LPS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	RW

[1] The reserved bits must always be written with the reset value.

Table 90. HcRhStatus - Host Controller Root Hub Status register bit description

Address: Content of the base address register + 50h

Bit	Symbol	Description
31	CRWE	On write **Clear Remote Wake-up Enable**: **0 —** No effect **1 —** Clears DRWE (Device Remote Wake-up Enable)
30 to 18	reserved	-
17	CCIC	**Overcurrent Indicator Change**: This bit is set by hardware when a change has occurred to the OCI bit of this register. **0 —** No effect **1 —** The HCD clears this bit.
16	LPSC	On read **Local Power Status Change**: The root hub does not support the local power status feature. Therefore, this bit is always logic 0. On write **Set Global Power**: In global power mode (Power Switching Mode = 0), logic 1 is written to this bit to turn on power to all ports (clear Port Power Status). In per-port power mode, it sets Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing logic 0 has no effect.
15	DRWE	On read **Device Remote Wake-up Enable**: This bit enables bit Connect Status Change (CSC) as a resume event, causing a state transition from USBSUSPEND to USBRESUME and setting the Resume Detected interrupt. **0 —** CSC is not a remote wake-up event. **1 —** CSC is a remote wake-up event. On write **Set Remote Wake-up Enable**: Writing logic 1 sets DRWE (Device Remote Wake-up Enable). Writing logic 0 has no effect.

Table 90. HcRhStatus - Host Controller Root Hub Status register bit description *...continued*
Address: Content of the base address register + 50h

Bit	Symbol	Description
14 to 2	reserved	-
1	OCI	**Overcurrent Indicator**: This bit reports overcurrent conditions when global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If the per-port overcurrent protection is implemented, this bit is always logic 0.
0	LPS	On read **Local Power Status**: The root hub does not support the local power status feature. Therefore, this bit is always read as logic 0. On write **Clear Global Power**: In global power mode (Power Switching Mode = 0), logic 1 is written to this bit to turn off power to all ports (clear Port Power Status). In per-port power mode, it clears Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing logic 0 has no effect.

11.1.22 HcRhPortStatus[2:1] register

The HcRhPortStatus[2:1] register is used to control and report port events on a per-port basis. NumberDownstreamPorts represents the number of HcRhPortStatus registers that are implemented in hardware. The lower word reflects the port status. The upper word reflects status change bits. Some status bits are implemented with special write behavior. If a transaction, token through handshake, is in progress when a write to change port status occurs, the resulting port status change is postponed until the transaction completes. Always write logic 0 to reserved bits. The bit allocation of the register is given in Table 91.

Table 91. HcRhPortStatus[2:1] - Host Controller Root Hub Port Status[2:1] register bit allocation
Address: Content of the base address register + 54h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]			PRSC	OCIC	PSSC	PESC	CSC
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]						LSDA	PPS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]			PRS	POCI	PSS	PES	CCS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 92. HcRhPortStatus[2:1] - Host Controller Root Hub Port Status[2:1] register bit description
Address: Content of the base address register + 54h

Bit	Symbol	Description
31 to 21	reserved	-
20	PRSC	**Port Reset Status Change**: This bit is set at the end of the 10 ms port reset signal. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** Port reset is not complete. **1 —** Port reset is complete.
19	OCIC	**Port Overcurrent Indicator Change**: This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when the root hub changes the POCI (Port Overcurrent Indicator) bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** No change in POCI. **1 —** POCI has changed.
18	PSSC	**Port Suspend Status Change**: This bit is set when the resume sequence is completed. This sequence includes the 20 ms resume pulse, LS EOP, and 3 ms re-synchronization delay. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. This bit is also cleared when Reset Status Change is set. **0 —** Resume is not completed. **1 —** Resume is completed.
17	PESC	**Port Enable Status Change**: This bit is set when hardware events cause the PES (Port Enable Status) bit to be cleared. Changes from the HCD writes do not set this bit. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. **0 —** No change in PES. **1 —** Change in PES.
16	CSC	**Connect Status Change**: This bit is set whenever a connect or disconnect event occurs. The HCD can write logic 1 to clear this bit. Writing logic 0 has no effect. If CCS (Current Connect Status) is cleared when a Set Port Reset, Set Port Enable, or Set Port Suspend write occurs, this bit is set to force the driver to re-evaluate the connection status because these writes must not occur if the port is disconnected. **0 —** No change in CCS. **1 —** Change in CCS. **Remark:** If the DeviceRemovable[NDP] bit is set, this bit is set only after a root hub reset to inform the system that the device is attached.
15 to 10	reserved	-
9	LSDA	On read **Low-speed Device Attached**: This bit indicates the speed of the device attached to this port. When set, a low-speed device is attached to this port. When cleared, a full-speed device is attached to this port. This field is valid only when CCS is set. **0 —** Port is not suspended. **1 —** Port is suspended. On write **Clear Port Power**: The HCD can clear the PPS (Port Power Status) bit by writing logic 1 to this bit. Writing logic 0 has no effect.

Table 92. HcRhPortStatus[2:1] - Host Controller Root Hub Port Status[2:1] register bit description *…continued*
Address: Content of the base address register + 54h

Bit	Symbol	Description
8	PPS	On read **Port Power Status**: This bit reflects the port power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. The HCD can set this bit by writing Set Port Power or Set Global Power. The HCD can clear this bit by writing Clear Port Power or Clear Global Power. Power Switching Mode and PortPowerControlMask[NDP] determine that power control switches are enabled. In Global Switching mode (Power Switching Mode = 0), only Set/Clear Global Power controls this bit. In the per-port power switching (Power Switching Mode = 1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/Clear Port Power commands are enabled. If the mask is not set, only Set/Clear Global Power commands are enabled. When port power is disabled, bits CCS (Current Connect Status), PES (Port Enable Status), PSS (Port Suspend Status), and PRS (Port Reset Status) must be reset. **0 —** Port power is off. **1 —** Port power is on. On write **Set Port Power**: The HCD can write logic 1 to set the PPS (Port Power Status) bit. Writing logic 0 has no effect. **Remark:** This bit always reads logic 1 if power switching is not supported.
7 to 5	reserved	-
4	PRS	On read **Port Reset Status**: When this bit is set by a write to Set Port Reset, port reset signaling is asserted. When reset is completed and PRSC is set, this bit is cleared. **0 —** Port reset signal is inactive. **1 —** Port reset signal is active. On write **Set Port Reset**: The HCD can set the port reset signaling by writing logic 1 to this bit. Writing logic 0 has no effect. If CCS is cleared, this write does not set PRS (Port Reset Status) but instead sets CCS. This informs the driver that it attempted to reset a disconnected port.
3	POCI	On read **Port Overcurrent Indicator**: This bit is valid only when the root hub is configured to show overcurrent conditions are reported on a per-port basis. If the per-port overcurrent reporting is not supported, this bit is set to logic 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. **0 —** No overcurrent condition. **1 —** Overcurrent condition detected. On write **Clear Suspend Status**: The HCD can write logic 1 to initiate a resume. Writing logic 0 has no effect. A resume is initiated only if PSS (Port Suspend Status) is set.

Table 92. HcRhPortStatus[2:1] - Host Controller Root Hub Port Status[2:1] register bit description *...continued*

Address: Content of the base address register + 54h

Bit	Symbol	Description
2	PSS	On read **Port Suspend Status**: This bit indicates whether the port is suspended or is in the resume sequence. It is set by a Set Suspend State write and cleared when PSSC (Port Suspend Status Change) is set at the end of the resume interval. This bit is not set if CCS (Current Connect Status) is cleared. This bit is also cleared when PRSC is set at the end of the port reset or when the host controller is placed in the USBRESUME state. If an upstream resume is in progress, it will propagate to the host controller. **0 —** Port is not suspended. **1 —** Port is suspended. On write **Set Port Suspend**: The HCD can set the PSS (Port Suspend Status) bit by writing logic 1 to this bit. Writing logic 0 has no effect. If CCS is cleared, this write does not set PSS; instead it sets CSS. This informs the driver that it attempted to suspend a disconnected port.
1	PES	On read **Port Enable Status**: This bit indicates whether the port is enabled or disabled. The root hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error is detected. This change also causes Port Enabled Status Change to be set. The HCD can set this bit by writing Set Port Enable and clear it by writing Clear Port Enable. This bit cannot be set when CCS (Current Connect Status) is cleared. This bit is also set on completing a port reset when Reset Status Change is set or on completing a port suspend when Suspend Status Change is set. **0 —** Port is disabled. **1 —** Port is enabled. On write **Set Port Enable**: The HCD can set PES (Port Enable Status) by writing logic 1. Writing logic 0 has no effect. If CCS is cleared, this write does not set PES, but instead sets CSC (Connect Status Change). This informs the driver that it attempted to enable a disconnected port.
0	CCS	On read **Current Connect Status**: This bit reflects the current state of the downstream port. **0 —** No device is connected. **1 —** Device is connected. On write **Clear Port Enable**: The HCD can write logic 1 to this bit to clear the PES (Port Enable Status) bit. Writing logic 0 has no effect. The CCS bit is not affected by any write. **Remark:** This bit always reads logic 1 when the attached device is nonremovable (DeviceRemovable[NDP]).

11.2 EHCI controller capability registers

Other than the OHCI host controller, there are some registers in EHCI that define the capability of EHCI. The address range of these registers is located before operational registers.

11.2.1 CAPLENGTH/HCIVERSION register

The bit allocation of this 4-byte register is given in Table 93.

Table 93. CAPLENGTH/HCIVERSION - Capability Length/Host Controller Interface Version Number register bit allocation

Address: Content of the base address register + 00h

Bit	31	30	29	28	27	26	25	24
Symbol	HCIVERSION[15:8]							
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R

Bit	23	22	21	20	19	18	17	16
Symbol	HCIVERSION[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPLENGTH[7:0]							
Reset	0	0	1	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 94. CAPLENGTH/HCIVERSION - Capability Length/Host Controller Interface Version Number register bit description

Address: Content of the base address register + 00h

Bit	Symbol	Description
31 to 16	HCIVERSION [15:0]	**Host Controller Interface Version Number**: This field contains a BCD encoded version number of the interface to which the host controller interface conforms.
15 to 8	reserved	-
7 to 0	CAPLENGTH [7:0]	**Capability Register Length**: This is used as an offset. It is added to the register base to find the beginning of the operational register space.

11.2.2 HCSPARAMS register

The Host Controller Structural Parameters (HCSPARAMS) register is a set of fields that are structural parameters. The bit allocation is given in Table 95.

Table 95. HCSPARAMS - Host Controller Structural Parameters register bit allocation

Address: Content of the base address register + 04h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	N_CC[3:0]				N_PCC[3:0]			
Reset	0	0	0	1	0	0	1	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PRR	reserved		PPC	N_PORTS[3:0]			
Reset	1	0	0	1	0	0	1	0
Access	R	R	R	R	R	R	R	R

Table 96. HCSPARAMS - Host Controller Structural Parameters register bit description
Address: Content of the base address register + 04h

Bit	Symbol	Description
31 to 16	reserved	-
15 to 12	N_CC [3:0]	**Number of Companion Controller**: This field indicates the number of companion controllers associated with this Hi-Speed USB host controller. A value of zero in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than zero in this field indicates there are companion Original USB host controller(s). Port-ownership hand-offs are supported.
11 to 8	N_PCC [3:0]	**Number of Ports per Companion Controller**: This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to the system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC can have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, and so on. In the previous example, N_PCC could have been 4, in which case the first four are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC.
7	PRR	**Port Routing Rules**: This field indicates the method used to map ports to companion controllers. **0 —** The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC ports are routed to the next lowest function companion controller, and so on. **1 —** The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.
6 to 5	reserved	-
4	PPC	**Port Power Control**: This field indicates whether the host controller implementation includes port power control. Logic 1 indicates the port has port power switches. Logic 0 indicates the port does not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register.
3 to 0	N_PORTS [3:0]	**Number of Ports**: This field specifies the number of physical downstream ports implemented on this host controller. The value in this field determines how many port registers are addressable in the operational register space. Logic 0 in this field is undefined.

11.2.3 HCCPARAMS register

The Host Controller Capability Parameters (HCCPARAMS) register is a 4-byte register, and the bit allocation is given in Table 97.

Table 97. HCCPARAMS - Host Controller Capability Parameters register bit allocation
Address: Content of the base address register + 08h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Symbol	IST[3:0]				reserved		PFLF	64AC
Reset	0	0	0	1	0	0	1	0
Access	R	R	R	R	R	R	R	R

Table 98. HCCPARAMS - Host Controller Capability Parameters register bit description
Address: Content of the base address register + 08h

Bit	Symbol	Description
31 to 8	reserved	-
7 to 4	IST[3:0]	**Isochronous Scheduling Threshold**: Default = implementation dependent. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When IST[3] is logic 0, the value of the least significant three bits indicates the number of microframes a host controller can hold a set of isochronous data structures, one or more, before flushing the state. When IST[3] is logic 1, the host software assumes the host controller may cache an isochronous data structure for an entire frame.
3 to 2	reserved	-
1	PFLF	**Programmable Frame List Flag**: Default = implementation dependent. If this bit is cleared, the system software must use a frame list length of 1024 elements with the host controller. The USBCMD register FLS[1:0] (bits 3 and 2) is read-only and must be cleared. If PFLF is set, the system software can specify and use a smaller frame list, and configure the host through the FLS bit. The frame list must always be aligned on a 4 kB page boundary to ensure that the frame list is always physically contiguous.
0	64AC	**64-bit Addressing Capability**: This field contains the addressing range capability. **0 —** Data structures using 32-bit address memory pointers. **1 —** Data structures using 64-bit address memory pointers.

11.2.4 HCSP-PORTROUTE register

The HCSP-PORTROUTE (Companion Port Route Description) register is an optional read-only field that is valid only if PRR (bit 7 in the HCSPARAMS register) is logic 1. Its address is content of the base address register + 0Ch.

This field is a 15-element nibble array, each 4 bits is one array element. Each array location corresponds one-to-one with a physical port provided by the host controller. For example, PORTROUTE[0] corresponds to the first PORTSC port, PORTROUTE[1] to the second PORTSC port, and so on. The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

11.3 Operational registers of enhanced USB host controller

11.3.1 USBCMD register

The USB Command (USBCMD) register indicates the command to be executed by the serial host controller. Writing to this register causes a command to be executed. Table 99 shows the bit allocation.

Table 99. USBCMD - USB Command register bit allocation

Address: Content of the base address register + 20h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	ITC[7:0]							
Reset	0	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	LHCR	IAAD	ASE	PSE	FLS[1:0]		HC RESET	RS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 100. USBCMD - USB Command register bit description

Address: Content of the base address register + 20h

Bit	Symbol	Description
31 to 24	reserved	-
23 to 16	ITC[7:0]	**Interrupt Threshold Control**: Default = 08h. This field is used by the system software to select the maximum rate at which the host controller will issue interrupts. If software writes an invalid value to this register, the results are undefined. Valid values are: **00h —** reserved **01h —** 1 microframe **02h —** 2 microframes **04h —** 4 microframes **08h —** 8 microframes (equals 1 ms) **10h —** 16 microframes (equals 2 ms) **20h —** 32 microframes (equals 4 ms) **40h —** 64 microframes (equals 8 ms) Software modifications to this field while HCH (bit 12) in the USBSTS register is zero results in undefined behavior.
15 to 8	reserved	-
7	LHCR	**Light Host Controller Reset**: This control bit is not required. It allows the driver software to reset the EHCI controller, without affecting the state of the ports or the relationship to the companion host controllers. If not implemented, a read of this field will always return zero. If implemented, on read: **0 —** Indicates that the Light Host Controller Reset has completed and it is ready for the host software to re-initialize the host controller. **1 —** Indicates that the Light Host Controller Reset has not yet completed.

Table 100. USBCMD - USB Command register bit description *...continued*
Address: Content of the base address register + 20h

Bit	Symbol	Description
6	IAAD	**Interrupt on Asynchronous Advance Doorbell**: This bit is used as a doorbell by software to notify the host controller to issue an interrupt the next time it advances the asynchronous schedule. Software must write logic 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule states, it sets IAA (bit 5 in the USBSTS register). If IAAE (bit 5 in the USBINTR register) is logic 1, then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to logic 0 after it sets IAA. Software must not set this bit when the asynchronous schedule is inactive because this results in an undefined value.
5	ASE	**Asynchronous Schedule Enable**: Default = 0. This bit controls whether the host controller skips processing the asynchronous schedule. **0 —** Do not process the asynchronous schedule. **1 —** Use the ASYNCLISTADDR register to access the asynchronous schedule.
4	PSE	**Periodic Schedule Enable**: Default = 0. This bit controls whether the host controller skips processing the periodic schedule. **0 —** Do not process the periodic schedule. **1 —** Use the PERIODICLISTBASE register to access the periodic schedule.
3 to 2	FLS[1:0]	**Frame List Size**: Default = 00b. This field is read and write only if PFLF (bit 1) in the HCCPARAMS register is set to logic 1. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index register must be used for the frame list current index. **00b —** 1024 elements (4096 bytes) **01b —** 512 elements (2048 bytes) **10b —** 256 elements (1024 bytes) for small environments **11b —** reserved
1	HCRESET	**Host Controller Reset**: This control bit is used by the software to reset the host controller. The effects of this on Root Hub registers are similar to a chip hardware reset. Setting this bit causes the host controller to reset its internal pipelines, timers, counters, state machines, and so on, to their initial values. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. This reset does not affect the PCI Configuration registers. All operational registers, including port registers and port state machines, are set to their initial values. Port ownership reverts to the companion host controller(s). The software must re-initialize the host controller to return it to an operational state. This bit is cleared by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing logic 0 to this register. Software must check that bit HCH is logic 0 before setting this bit. Attempting to reset an actively running host controller results in undefined behavior.
0	RS	**Run/Stop**: 1 = Run. 0 = Stop. When set, the host controller executes the schedule. The host controller continues execution as long as this bit is set. When this bit is cleared, the host controller completes the current and active transactions in the USB pipeline, and then halts. Bit HCH indicates when the host controller has finished the transaction and has entered the stopped state. Software must check that the HCH bit is logic 1, before setting this bit.

11.3.2 USBSTS register

The USB Status (USBSTS) register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software clears the register bits by writing ones to them. The bit allocation is given in Table 101.

Table 101. USBSTS - USB Status register bit allocation
Address: Content of the base address register + 24h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	ASS	PSSTAT	RECL	HCH	reserved[1]			
Reset	0	0	0	1	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]		IAA	HSE	FLR	PCD	USB ERRINT	USBINT
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 102. USBSTS - USB Status register bit description
Address: Content of the base address register + 24h

Bit	Symbol	Description
31 to 16	reserved	-
15	ASS	**Asynchronous Schedule Status**: Default = 0. The bit reports the current real status of the asynchronous schedule. If this bit is logic 0, the status of the asynchronous schedule is disabled. If this bit is logic 1, the status of the asynchronous schedule is enabled. The host controller is not required to immediately disable or enable the asynchronous schedule when software changes ASE (bit 5 in the USBCMD register). When this bit and the ASE bit have the same value, the asynchronous schedule is either enabled (1) or disabled (0).
14	PSSTAT	**Periodic Schedule Status**: Default = 0. This bit reports the current status of the periodic schedule. If this bit is logic 0, the status of the periodic schedule is disabled. If this bit is logic 1, the status of the periodic schedule is enabled. The host controller is not required to immediately disable or enable the periodic schedule when software changes PSE (bit 4) in the USBCMD register. When this bit and the PSE bit have the same value, the periodic schedule is either enabled (1) or disabled (0).
13	RECL	**Reclamation**: Default = 0. This is a read-only status bit that is used to detect an empty asynchronous schedule.
12	HCH	**HC Halted**: Default = 1. This bit is logic 0 when RS (bit 0) in the USBCMD register is logic 1. The host controller sets this bit to logic 1 after it has stopped executing because the RS bit is set to logic 0, either by software or by the host controller hardware. For example, on an internal error.
11 to 6	reserved	-
5	IAA	**Interrupt on Asynchronous Advance**: Default = 0. The system software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing logic 1 to IAAD (bit 6) in the USBCMD register. This status bit indicates the assertion of that interrupt source.

Table 102. USBSTS - USB Status register bit description *...continued*
Address: Content of the base address register + 24h

Bit	Symbol	Description
4	HSE	**Host System Error**: The host controller sets this bit when a serious error occurs during a host system access, involving the host controller module. In a PCI system, conditions that set this bit include PCI parity error, PCI master abort, and PCI target abort. When this error occurs, the host controller clears RS (bit 0 in the USBCMD register) to prevent further execution of the scheduled TDs.
3	FLR	**Frame List Rollover**: The host controller sets this bit to logic 1 when the frame list index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size, as programmed in FLS (bits 3 to 2) of the USBCMD register, is 1024, the Frame Index register rolls over every time bit 13 of the FRINDEX register toggles. Similarly, if the size is 512, the host controller sets this bit to logic 1 every time bit 12 of the FRINDEX register toggles.
2	PCD	**Port Change Detect**: The host controller sets this bit to logic 1 when any port, where PO (bit 13 of PORTSC) is cleared, changes to logic 1, or FPR (bit 6 of PORTSC) changes to logic 1 as a result of a J-K transition detected on a suspended port. This bit is allowed to be maintained in the auxiliary power well. Alternatively, it is also acceptable that, on a D3-to-D0 transition of the EHCI host controller device, this bit is loaded with the logical OR of all the PORTSC change bits, including force port resume, overcurrent change, enable or disable change, and connect status change.
1	USBERR INT	**USB Error Interrupt**: The host controller sets this bit when an error condition occurs because of completing a USB transaction. For example, error counter underflow. If the Transfer Descriptor (TD) on which the error interrupt occurred also had its IOC bit set, both this bit and the USBINT bit are set. For details, refer to *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.
0	USBINT	**USB Interrupt**: The host controller sets this bit on completing a USB transaction, which results in the retirement of a TD that had its IOC bit set. The host controller also sets this bit when a short packet is detected, that is, the actual number of bytes received was less than the expected number of bytes. For details, refer to *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*.

11.3.3 USBINTR register

The USB Interrupt Enable (USBINTR) register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in USBSTS to allow the software to poll for events. The USBSTS register bit allocation is given in Table 103.

Table 103. USBINTR - USB Interrupt Enable register bit allocation
Address: Content of the base address register + 28h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]		IAAE	HSEE	FLRE	PCIE	USBERR INTE	USBINTE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 104. USBINTR - USB Interrupt Enable register bit description
Address: Content of the base address register + 28h

Bit	Symbol	Description
31 to 6	reserved	-
5	IAAE	**Interrupt on Asynchronous Advance Enable**: When this bit and IAA (bit 5 in the USBSTS register) are set, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit IAA.
4	HSEE	**Host System Error Enable**: When this bit and HSE (bit 4 in the USBSTS register) are set, the host controller issues an interrupt. The interrupt is acknowledged by software clearing bit HSE.
3	FLRE	**Frame List Rollover Enable**: When this bit and FLR (bit 3 in the USBSTS register) are set, the host controller issues an interrupt. The interrupt is acknowledged by software clearing bit FLR.
2	PCIE	**Port Change Interrupt Enable**: When this bit and PCD (bit 2 in the USBSTS register) are set, the host controller issues an interrupt. The interrupt is acknowledged by software clearing bit PCD.
1	USB ERRINTE	**USB Error Interrupt Enable**: When this bit and USBERRINT (bit 1 in the USBSTS register) are set, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit USBERRINT.
0	USBINTE	**USB Interrupt Enable**: When this bit and USBINT (bit 0 in the USBSTS register) are set, the host controller issues an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing bit USBINT.

11.3.4 FRINDEX register

The Frame Index (FRINDEX) register is used by the host controller to index into the periodic frame list. The register updates every 125 μs, once each microframe. Bits N to 3 are used to select a particular entry in the periodic frame list during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by the system software in FLS[1:0] (bits 3 to 2) of the USBCMD register. This register must be written as a DWORD. Byte writes produce undefined results. This register cannot be written unless the host controller is in the halted state, as indicated by HCH (bit 12 in the USBSTS register). A write to this register while RS (bit 0 in the USBCMD register) is set produces undefined results. Writes to this register also affect the SOF value.

The bit allocation is given in Table 105.

Table 105. FRINDEX - Frame Index register bit allocation
Address: Content of the base address register + 2Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]		FRINDEX[13:8]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	FRINDEX[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 106. FRINDEX - Frame Index register bit description
Address: Content of the base address register + 2Ch

Bit	Symbol	Description
31 to 14	reserved	-
13 to 0	FRINDEX [13:0]	**Frame Index**: Bits in this register are used for the frame number in the SOF packet and as the index into the frame list. The value in this register increments at the end of each time frame. For example, microframe. The bits used for the frame number in the SOF token are taken from bits 13 to 3 of this register. Bits N to 3 are used for the frame list current index. This means that each location of the frame list is accessed eight times, frames or microframes, before moving to the next index. Table 107 illustrates N based on the value of FLS[1:0] (bits 3 to 2 in the USBCMD register).

Table 107. N based value of FLS[1:0]

FLS[1:0]	Number elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	reserved	-

11.3.5 PERIODICLISTBASE register

The Periodic Frame List Base Address (PERIODICLISTBASE) register contains the beginning address of the periodic frame list in the system memory. If the host controller is in 64-bit mode, as indicated by logic 1 in 64AC (bit 0 of the HCCPARAMS register), the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. For details on the CTRLDSSEGMENT register, refer to *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*. The

system software loads this register before starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed as 4 kB aligned. The contents of this register are combined with the FRINDEX register to enable the host controller to step through the periodic frame list in sequence.

The bit allocation is given in Table 108.

Table 108. PERIODICLISTBASE - Periodic Frame List Base Address register bit allocation
Address: Content of the base address register + 34h

Bit	31	30	29	28	27	26	25	24
Symbol	BA[19:12]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	BA[11:4]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	BA[3:0]				reserved[1]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 109. PERIODICLISTBASE - Periodic Frame List Base Address register bit description
Address: Content of the base address register + 34h

Bit	Symbol	Description
31 to 12	BA[19:0]	**Base Address**: These bits correspond to memory address signals 31 to 12, respectively.
11 to 0	reserved	-

11.3.6 ASYNCLISTADDR register

This 32-bit register contains the address of the next asynchronous queue head to be executed. If the host controller is in 64-bit mode, as indicated by logic 1 in 64AC (bit 0 of the HCCPARAMS register), the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. For details on the CTRLDSSEGMENT register, refer to *Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0*. Bits 4 to 0 of this register always return zeros when read. The memory structure referenced by the physical memory pointer is assumed as 32 bytes (cache aligned). For bit allocation, see Table 110.

Table 110. ASYNCLISTADDR - Current Asynchronous List Address register bit allocation
Address: Content of the base address register + 38h

Bit	31	30	29	28	27	26	25	24
Symbol	LPL[26:19]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	LPL[18:11]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	LPL[10:3]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	LPL[2:0]			reserved[1]				
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 111. ASYNCLISTADDR - Current Asynchronous List Address register bit description
Address: Content of the base address register + 38h

Bit	Symbol	Description
31 to 5	LPL[26:0]	**Link Pointer List**: These bits correspond to memory address signals 31 to 12, respectively. This field may only reference a Queue Head (QH).
4 to 0	reserved	-

11.3.7 CONFIGFLAG register

The bit allocation of the Configure Flag (CONFIGFLAG) register is given in Table 112.

Table 112. CONFIGFLAG - Configure Flag register bit allocation
Address: Content of the base address register + 60h

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Symbol	reserved[1]							CF
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 113. CONFIGFLAG - Configure Flag register bit description
Address: Content of the base address register + 60h

Bit	Symbol	Description
31 to 1	reserved	-
0	CF	**Configure Flag**: The host software sets this bit as the last action in its process of configuring the host controller. This bit controls the default port-routing control logic. **0 —** Port routing control logic default-routes each port to an implementation dependent classic host controller. **1 —** Port routing control logic default-routes all ports to this host controller.

11.3.8 PORTSC registers 1, 2

The Port Status and Control (PORTSC) register is in the auxiliary power well. It is only reset by hardware when the auxiliary power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

If the port has power control, software cannot change the state of the port until it sets port power bits. Software must not attempt to change the state of the port until power is stable on the port; maximum delay is 20 ms from the transition. For bit allocation, see Table 114.

Table 114. PORTSC 1, 2 - Port Status and Control 1, 2 register bit allocation
Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved	WKOC_E	WKDSCNNT_E	WKCNNT_E	PTC[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]		PO	PP	LS[1:0]		reserved[1]	PR
Reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	7	6	5	4	3	2	1	0
Symbol	SUSP	FPR	OCC	OCA	PEDC	PED	ECSC	ECCS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R	R	R/W	R/W	R/W	R

[1] The reserved bits must always be written with the reset value.

Table 115. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description

Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
31 to 23	reserved	-
22	WKOC_E	**Wake on Overcurrent Enable**: Default = 0. Setting this bit enables the port to be sensitive to overcurrent conditions as wake-up events.[1]
21	WKDS CNNT_E	**Wake on Disconnect Enable**: Default = 0. Setting this bit enables the port to be sensitive to device disconnects as wake-up events.[1]
20	WKCNNT_E	**Wake on Connect Enable**: Default = 0. Setting this bit enables the port to be sensitive to device connects as wake-up events.[1]
19 to 16	PTC[3:0]	**Port Test Control**: Default = 0000b. When this field is logic 0, the port is not operating in test mode. A nonzero value indicates that it is operating in test mode and test mode is indicated by the value. The encoding of test mode bits are: **0000b —** Test mode disabled **0001b —** Test J_STATE **0010b —** Test K_STATE **0011b —** Test SE0_NAK **0100b —** Test packet **0101b —** Test FORCE_ENABLE **0110b to 1111b —** reserved
15 to 14	reserved	-
13	PO	**Port Owner**: Default = 1. This bit unconditionally goes to logic 0 when CF (bit 0) in the CONFIGFLAG register makes logic 0 to logic 1 transition. This bit unconditionally goes to logic 1 when the CF bit is logic 0. The system software uses this field to release ownership of the port to a selected host controller, if the attached device is not a high-speed device. Software writes logic 1 to this bit, if the attached device is not a high-speed device. Logic 1 in this bit means that a companion host controller owns and controls the port.
12	PP	**Port Power**: The function of this bit depends on the value of PPC (bit 4) in the HCSPARAMS register. **If PPC = 0 and PP = 1 —** The host controller does not have port power control switches. Always powered. **If PPC = 1 and PP = 1 or 0 —** The host controller has port power control switches. This bit represents the current setting of the switch: logic 0 = off, logic 1 = on. When PP is logic 0, the port is nonfunctional and will not report any status. When an overcurrent condition is detected on a powered port and PPC is logic 1, the PP bit in each affected port may be changed by the host controller from logic 1 to logic 0, removing power from the port.

Table 115. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description *...continued*
Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
11 to 10	LS[1:0]	**Line Status**: This field reflects the current logical levels of the DP (bit 11) and DM (bit 10) signal lines. These bits are used to detect low-speed USB devices before the port reset and enable sequence. This field is valid only when the Port Enable bit is logic 0, and the Current Connect Status bit is set to logic 1. **00b —** SE0: Not a low-speed device, perform EHCI reset **01b —** K-state: Low-speed device, release ownership of the port **10b —** J-state: Not a low-speed device, perform EHCI reset **11b —** Undefined: Not a low-speed device, perform EHCI reset If the PP bit is logic 0, this field is undefined.
9	reserved	-
8	PR	**Port Reset**: Logic 1 means the port is in reset. Logic 0 means the port is not in reset. Default = 0. When software sets this bit from logic 0, the bus reset sequence as defined in *Universal Serial Bus Specification Rev. 2.0* is started. Software clears this bit to terminate the bus reset sequence. Software must hold this bit at logic 1 until the reset sequence, as specified in *Universal Serial Bus Specification Rev. 2.0*, is completed. **Remark:** When software sets this bit, it must also clear the Port Enable bit. **Remark:** When software clears this bit, there may be a delay before the bit status changes to logic 0 because it will not read logic 0 until the reset is completed. If the port is in high-speed mode after reset is completed, the host controller will automatically enable this port; it can set the Port Enable bit. A host controller must terminate the reset and stabilize the state of the port within 2 ms of software changing this bit from logic 1 to logic 0. For example, if the port detects that the attached device is high-speed during a reset, then the host controller must enable the port within 2 ms of software clearing this bit. HCH (bit 12) in the USBSTS register must be logic 0 before software attempts to use this bit. The host controller may hold Port Reset asserted when the HCH bit is set.[1]
7	SUSP	**Suspend**: Default = 0. Logic 1 means the port is in the suspend state. Logic 0 means the port is not suspended. The PED (Port Enabled) bit and this bit define the port states as follows: **PED = 0 and SUSP = X —** Port is disabled. **PED = 1 and SUSP = 0 —** Port is enabled. **PED = 1 and SUSP = 1 —** Port is suspended. When in the suspend state, downstream propagation of data is blocked on this port, except for the port reset. If a transaction was in progress when this bit was set, blocking occurs at the end of the current transaction. In the suspend state, the port is sensitive to resume detection. The bit status does not change until the port is suspended and there may be a delay in suspending a port, if there is a transaction currently in progress on USB. Attempts to clear this bit are ignored by the host controller. The host controller will unconditionally set this bit to logic 0 when: • Software changes the FPR (Force Port Resume) bit to logic 0. • Software changes the PR (Port Reset) bit to logic 1. If the host software sets this bit when the Port Enabled bit is logic 0, the results are undefined.[1]

Table 115. PORTSC 1, 2 - Port Status and Control 1, 2 register bit description *...continued*
Address: Content of the base address register + 64h + (4 × Port Number − 1) where Port Number is 1, 2

Bit	Symbol	Description
6	FPR	**Force Port Resume**: Logic 1 means resume detected or driven on the port. Logic 0 means no resume (K-state) detected or driven on the port. Default = 0. Software sets this bit to drive the resume signaling. The host controller sets this bit if a J-to-K transition is detected, while the port is in the suspend state. When this bit changes to logic 1 because a J-to-K transition is detected, PCD (bit 2) in the USBSTS register is also set to logic 1. If software sets this bit to logic 1, the host controller must not set the PCD bit. When the EHCI controller owns the port, resume follows the sequence specified in *Universal Serial Bus Specification Rev. 2.0*. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains set. Software must time the resume and clear this bit after the correct amount of time has elapsed. Clearing this bit causes the port to return to high-speed mode, forcing the bus below the port into a high-speed idle. This bit will remain at logic 1, until the port has switched to the high-speed idle. The host controller must complete this transition within 2 ms of software clearing this bit.[1]
5	OCC	**Overcurrent Change**: Default = 0. This bit is set to logic 1 when there is a change in overcurrent active. Software clears this bit by setting it to logic 1.
4	OCA	**Overcurrent Active**: Default = 0. If set to logic 1, this port has an overcurrent condition. If set to logic 0, this port does not have an overcurrent condition. This bit will automatically change from logic 1 to logic 0 when the overcurrent condition is removed.
3	PEDC	**Port Enable/Disable Change**: Logic 1 means the port enabled or disabled status has changed. Logic 0 means no change. Default = 0. For the root hub, this bit is set only when a port is disabled because of the appropriate conditions existing at the EOF2 point. For definition of port error, refer to Chapter 11 of *Universal Serial Bus Specification Rev. 2.0*. Software clears this bit by setting it.[1]
2	PED	**Port Enabled/Disabled**: Logic 1 means enable. Logic 0 means disable. Default = 0. Ports can only be enabled by the host controller as a part of the reset and enable sequence. Software cannot enable a port by writing logic 1 to this field. The host controller will only set this bit when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition or by host software. The bit status does not change until the port state has changed. There may be a delay in disabling or enabling a port because of other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port, except for reset.[1]
1	ECSC	**Connect Status Change**: Logic 1 means change in ECCS. Logic 0 means no change. Default = 0. This bit indicates a change has occurred in the ECCS of the port. The host controller sets this bit for all changes to the port device connect status, even if the system software has not cleared an existing connect status change. For example, the insertion status changes two times before the system software has cleared the changed condition, hub hardware will be setting an already-set bit, that is, the bit will remain set. Software clears this bit by writing logic 1 to it.[1]
0	ECCS	**Current Connect Status**: Logic 1 indicates a device is present on the port. Logic 0 indicates no device is present. Default = 0. This value reflects the current state of the port and may not directly correspond to the event that caused the ECSC bit to be set.[1]

[1] These fields read logic 0, if the PP bit is logic 0.

11.4 Miscellaneous registers

The ISP1568A employs mechanisms to improve throughput in USB transfers. In certain system in which PCI throughput is low, however, these mechanisms may fail. The system tuning register provides a mean to disable these mechanisms using software. For bit allocation of the register, see Table 116.

Table 116. System Tuning register bit allocation
Address: Content of the base address register + 6Ch

Bit	31	30	29	28	27	26	25	24
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	reserved[1]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved[1]						RBD	WMD
Reset	0	0	0	0	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] The reserved bits must always be written with the reset value.

Table 117. System Tuning register bit description
Address: Content of the base address register + 6Ch

Bit	Symbol	Description
31 to 2	-	reserved
1	RBD	**Ring Buffering Disable**: Default = 1. To enable the ring buffering, clear the RBD bit to logic 0. To disable the ring buffering, set the RBD bit to logic 1. The ISP1568A employs the ring buffering mechanism to improve throughput in USB IN transfers. This mechanism allows the start of an IN packet transfer immediately after a previous IN packet is received. In some systems, with congested PCI bus, data overrun conditions may occur when the ring buffering is enabled. Software can set this bit to disable the ring buffering. **Remark:** If the SYS_TUNE pin is connected to V_{CC}, the RBD bit will always be logic 1.
0	WMD	**Watermark Disable**: Default = 1. To enable the watermark feature, clear the WMD bit to logic 0; to disable the watermark feature, set WMD to logic 1. The ISP1568A employs a watermark mechanism to improve throughput in USB bulk and interrupt OUT transfers. This mechanism starts USB transfer over the USB bus when data fetched from the host system reaches the watermark level (191 bytes, 255 bytes, 383 bytes, 511 bytes, 639 bytes, and 767 bytes) just before the full packet size. For example, the ISP1568A will start transferring an OUT packet of size 1024 bytes over the USB bus when 767 bytes has been fetched from the host system. In some systems, with congested PCI bus, data underrun conditions may occur when the watermark is enabled. Software can set this bit to disable the watermark feature. **Remark:** If the SYS_TUNE pin is connected to V_{CC}, the WMD bit will always be logic 1.

12. Limiting values

Table 118. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(IO)}$	IO supply voltage			−0.5	+4.6	V
$V_{CC(REG)}$	regulator supply voltage			−0.5	+4.6	V
$V_{CC(IO)AUX}$	auxiliary input/output supply voltage			−0.5	+4.6	V
$V_{CC(AUX)}$	auxiliary supply voltage		[1]	−0.5	+4.6	V
$V_{CCA(AUX)}$	auxiliary analog supply voltage			−0.5	+4.6	V
I_{lu}	latch-up current	$V_I < 0$ V or $V_I > V_{CC(IO)}$		-	100	mA
V_{esd}	electrostatic discharge voltage	all pins ($I_{LI} < 1$ μA)	[2]	−2	+2	kV
T_{stg}	storage temperature			−40	+125	°C

[1] $V_{CC(AUX)}$ should come up not later than $V_{CC(IO)}$ and $V_{CC(REG)}$.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model JESD22-A114C).

13. Recommended operating conditions

Table 119. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(IO)}$	IO supply voltage		3.0	3.3	3.6	V
$V_{CC(REG)}$	regulator supply voltage		3.0	3.3	3.6	V
$V_{CC(IO)AUX}$	auxiliary input/output supply voltage		3.0	3.3	3.6	V
$V_{CC(AUX)}$	auxiliary supply voltage		3.0	3.3	3.6	V
$V_{CCA(AUX)}$	auxiliary analog supply voltage		3.0	3.3	3.6	V
V_I	input voltage		0	-	$V_{CC(IO)}$	V
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.95	V
T_{amb}	ambient temperature		−40	-	+85	°C

14. Static characteristics

Table 120. Static characteristics: I²C-bus interface (SDA and SCL)
$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.7 × $V_{CC(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 × $V_{CC(IO)}$	V
V_{hys}	hysteresis voltage		0.15	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
$I_{CC(susp)}$	suspend supply current		-	1	-	μA

Table 121. Static characteristics: digital pins (PWE1_N, OC1_N, PWE2_N, and OC2_N)
$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage		2.4	-	-	V

Table 122. Static characteristics: PCI interface block
$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.5 × $V_{CC(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 × $V_{CC(IO)}$	V
V_{IPU}	input pull-up voltage		2.1	-	-	V
I_{LI}	input leakage current	0 V < V_I < $V_{CC(IO)}$	−10	-	+10	μA
V_{OH}	HIGH-level output voltage	I_O = 500 μA	2.7	-	-	V
V_{OL}	LOW-level output voltage	I_O = 1500 μA	-	-	0.3	V
C_{in}	input capacitance		-	-	10	pF
C_{clk}	clock capacitance		5	-	12	pF
C_{IDSEL}	IDSEL pin capacitance		-	-	8	pF

Table 123. Static characteristics: USB interface block (pins DM1 to DM2 and DP1 to DP2)
$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels for high-speed						
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)		100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)		525	-	625	mV

Table 123. Static characteristics: USB interface block (pins DM1 to DM2 and DP1 to DP2) *…continued*
$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSDI}	high-speed differential input sensitivity	$\|V_{DP} - V_{DM}\|$	300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)		−50	-	+500	mV
Output levels for high-speed						
V_{HSOI}	high-speed idle level voltage		−10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage		360	-	440	mV
V_{HSOL}	high-speed data signaling LOW-level voltage		−10	-	+10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700[1]	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		−900[1]	-	−500	mV
Input levels for full-speed and low-speed						
V_{IH}	HIGH-level input voltage	drive	2.0	-	-	V
V_{IHZ}	HIGH-level input voltage (floating)		2.7	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage range		0.8	-	2.5	V
Output levels for full-speed and low-speed						
V_{OH}	HIGH-level output voltage		2.8	-	3.6	V
V_{OL}	LOW-level output voltage		0	-	0.3	V
V_{OSE1}	SE1 output voltage		0.8	-	-	V
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
Leakage current						
I_{LZ}	off-state leakage current		−1	-	+1	μA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	5	pF

[1] High-speed termination resistor disabled, pull-up resistor connected. Only during reset, when both the hub and the device are capable of high-speed operation.

Table 124. Static characteristics: $V_{POR(trip)}$
$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{trip(high)}$	high trip-level		1.0	1.2	1.4	V
$V_{trip(low)}$	low trip-level		0.95	1.1	1.3	V
$HL_{trip(diff)}$	difference between high and low trip-level		50	120	180	mV

Table 125. Current consumption

$V_{CC(IO)AUX}$ = 3.0 V to 3.6 V; $V_{CC(AUX)}$ = 3.0 V to 3.6 V; $V_{CCA(AUX)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 3.0 V to 3.6 V; $V_{CC(REG)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)AUX}$ = 3.3 V; $V_{CC(AUX)}$ = 3.3 V; $V_{CCA(AUX)}$ = 3.3 V; $V_{CC(IO)}$ = 3.3 V; $V_{CC(REG)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Cumulative current	Conditions	Typ	Unit
Total current on pins $V_{CC(IO)AUX}$ plus $V_{CC(AUX)}$ plus $V_{CCA(AUX)}$ plus $V_{CC(IO)}$ plus $V_{CC(REG)}$	no device connected to the ISP1568A[1]	27	mA
	one high-speed device connected to the ISP1568A	54	mA
	two high-speed devices connected to the ISP1568A	75	mA
Auxiliary current on pins $V_{CC(IO)AUX}$ plus $V_{CC(AUX)}$ plus $V_{CCA(AUX)}$	no device connected to the ISP1568A[1]	19	mA
	one high-speed device connected to the ISP1568A	43	mA
	two high-speed devices connected to the ISP1568A	63	mA
On pins $V_{CC(IO)}$ plus $V_{CC(REG)}$	no device connected to the ISP1568A[1]	8	mA
	one high-speed device connected to the ISP1568A	11	mA
	two high-speed devices connected to the ISP1568A	12	mA

[1] When one or two full-speed or low-speed power devices are connected, the current consumption is comparable to the current consumption when no high-speed devices are connected. There is a difference of approximately 1 mA.

Table 126. Current consumption: S1 and S3

$V_{CC(IO)AUX}$ = 3.0 V to 3.6 V; $V_{CC(AUX)}$ = 3.0 V to 3.6 V; $V_{CCA(AUX)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 3.0 V to 3.6 V; $V_{CC(REG)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)AUX}$ = 3.3 V; $V_{CC(AUX)}$ = 3.3 V; $V_{CCA(AUX)}$ = 3.3 V; $V_{CC(IO)}$ = 3.3 V; $V_{CC(REG)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Current consumption	Typ	Unit
S1[1]	2.10	mA
S3[2]	160	µA

[1] S1 represents the system state that will determine the B1 and D1 states. For details, refer to *PCI Bus Power Management Interface Specification Rev. 1.1*.

[2] S3 represents the system state that will determine the B3 and D3 states. For details, refer to *PCI Bus Power Management Interface Specification Rev. 1.1*.

15. Dynamic characteristics

Table 127. Dynamic characteristics: system clock timing

$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PCI clock							
$f_{clk(PCI)}$	PCI clock frequency			31	-	33	MHz
Crystal specification							
f_{clk}	clock frequency		[1]	-	12	-	MHz
R_S	series resistance			-	-	100	Ω
C_L	load capacitance			-	18	-	pF
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1		[2]	-	-	200	ps
Δf/f	frequency stability	on pin XTAL1		-	-	50	ppm
External clock specification							
$f_{i(XTAL1)}$	input frequency on pin XTAL1			-	12	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1		[2]	-	-	200	ps
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1			-	-	50	ppm
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1			45	50	55	%

[1] Suggested values for external capacitors are 22 pF to 27 pF.

[2] RMS = Root Mean Square.

Table 128. Dynamic characteristics: I²C-bus interface (SDA and SCL)

$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}; 10 pF < C_b < 400 pF[1]	-	0	250	ns

[1] The capacitive load for each bus line (C_b) is specified in pF. To meet the specification for V_{OL} and the maximum rise time (300 ns), use an external pull-up resistor with $R_{UP(max)}$ = 850 / C_b kΩ and $R_{UP(min)}$ = ($V_{CC(IO)}$ − 0.4) / 3 kΩ.

Table 129. Dynamic characteristics: PCI interface block

$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SR	slew rate	standard load[1]	1	-	4	V/ns

[1] Standard load is 10 pF together with a pull-up and pull-down resistor of 10 kΩ.

Table 130. Dynamic characteristics: high-speed source electrical characteristics

$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{HSR}	rise time (10% to 90%)		500	-	-	ps
t_{HSF}	fall time (10% to 90%)		500	-	-	ps

Table 130. Dynamic characteristics: high-speed source electrical characteristics *...continued*

$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{HSDRV}	driver output impedance (which also serves as high-speed termination)	includes the R_S resistor	40.5	45	49.5	Ω
Clock timing						
t_{HSDRAT}	high-speed data rate		479.76	-	480.24	Mbit/s
t_{HSFRAM}	microframe interval		124.9375	-	125.0625	µs
t_{HSRFI}	consecutive microframe interval difference		1	-	four high-speed bit times	ns

Table 131. Dynamic characteristics: full-speed source electrical characteristics

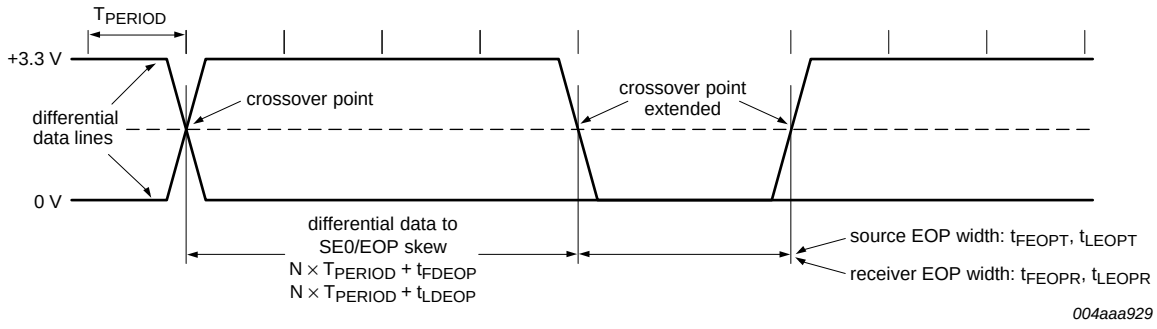
$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10% to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90% to 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching		90	-	111.1	%
Data timing: see Figure 9						
t_{FDEOP}	source jitter for differential transition to SE0 transition	full-speed timing	−2	-	+5	ns
t_{FEOPT}	source SE0 interval of EOP		160	-	175	ns
t_{FEOPR}	receiver SE0 interval of EOP		82	-	-	ns
t_{LDEOP}	upstream facing port source jitter for differential transition to SE0 transition	low-speed timing	−40	-	+100	ns
t_{LEOPT}	source SE0 interval of EOP		1.25	-	1.5	µs
t_{LEOPR}	receiver SE0 interval of EOP		670	-	-	ns
t_{FST}	width of SE0 interval during differential transition		-	-	14	ns

Table 132. Dynamic characteristics: low-speed source electrical characteristics

$V_{CCA(AUX)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CCA(AUX)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{LR}	transition time: rise time		75	-	300	ns
t_{LF}	transition time: fall time		75	-	300	ns
t_{LRFM}	rise and fall time matching		90	-	125	%



T_{PERIOD} is the bit duration corresponding to the USB data rate.

Fig 9. USB source differential data-to-EOP transition skew and EOP width

15.1 Timing

Table 133. PCI clock and IO timing

$V_{CC(IO)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at $V_{CC(IO)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PCI clock timing; see Figure 10						
T_{cyc}	CLK cycle time		30	-	32	ns
t_{high}	CLK HIGH time		11	-	-	ns
t_{low}	CLK LOW time		11	-	-	ns
SR_{CLK}	CLK slew rate		1	-	4	V/ns
$SR_{RST\#}$	RST# slew rate		50	-	-	mV/ns
PCI input timing; see Figure 11						
t_{su}	input set-up time to CLK - bused signals		7	-	-	ns
$t_{su(ptp)}$	input set-up time to CLK - point-to-point	[1]	10	-	-	ns
t_h	input hold time from CLK		0	-	-	ns
PCI output timing; see Figure 12						
t_{val}	CLK to signal valid delay time - bused signals		2	-	11	ns
$t_{val(ptp)}$	CLK to signal valid delay time - point-to-point	[1]	2	-	12	ns
t_{dZH}	float to active HIGH delay time		2	-	-	ns
t_{dHZ}	active HIGH to float delay time		-	-	28	ns
PCI reset timing						
t_{rst}	reset active time after power stable		1	-	-	ms
$t_{rst-clk}$	reset active time after CLK stable		100	-	-	µs

[1] REQ# and GNT# are point-to-point signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All others are bus signals.

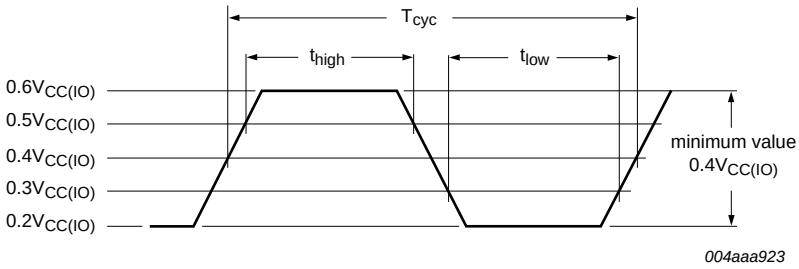


Fig 10. PCI clock

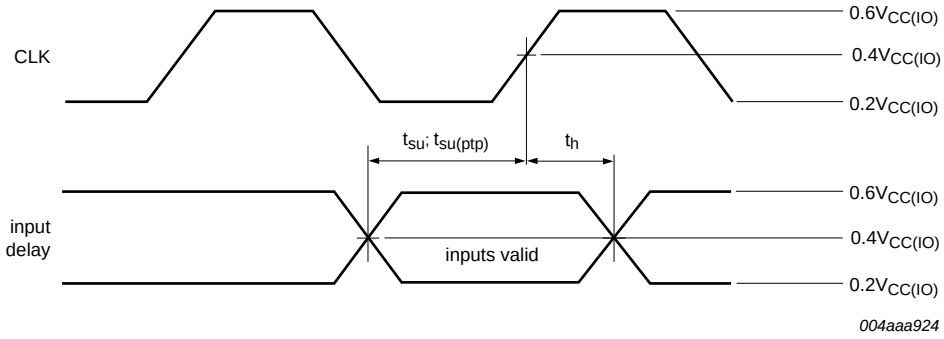


Fig 11. PCI input timing

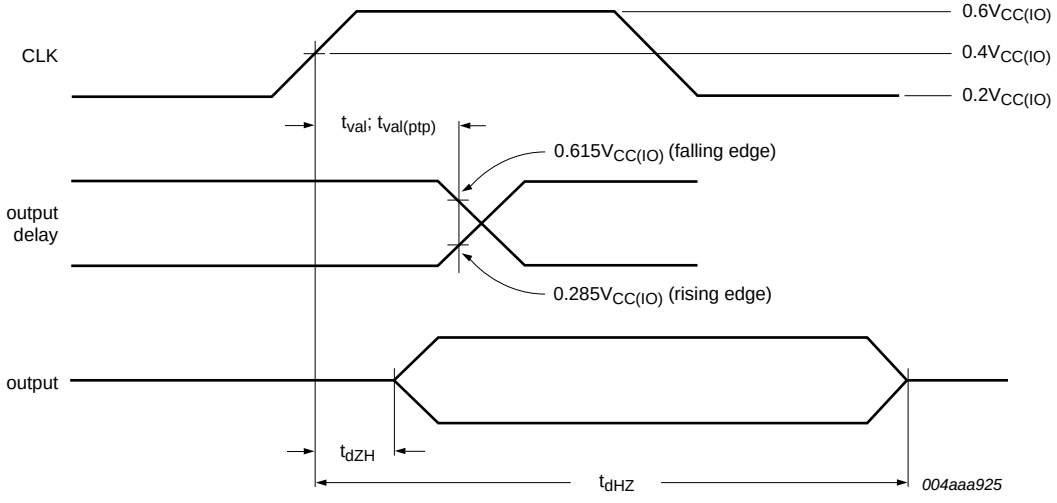
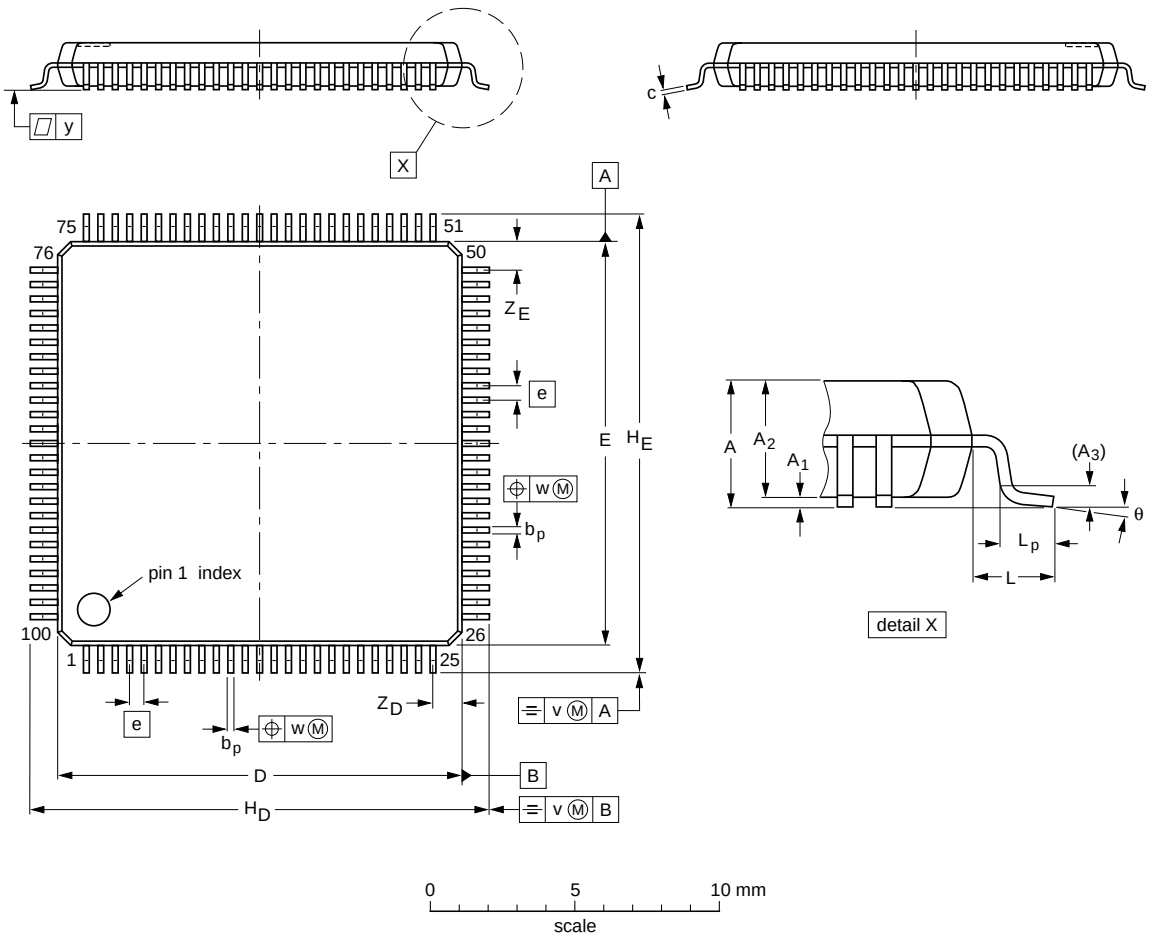


Fig 12. PCI output timing

16. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

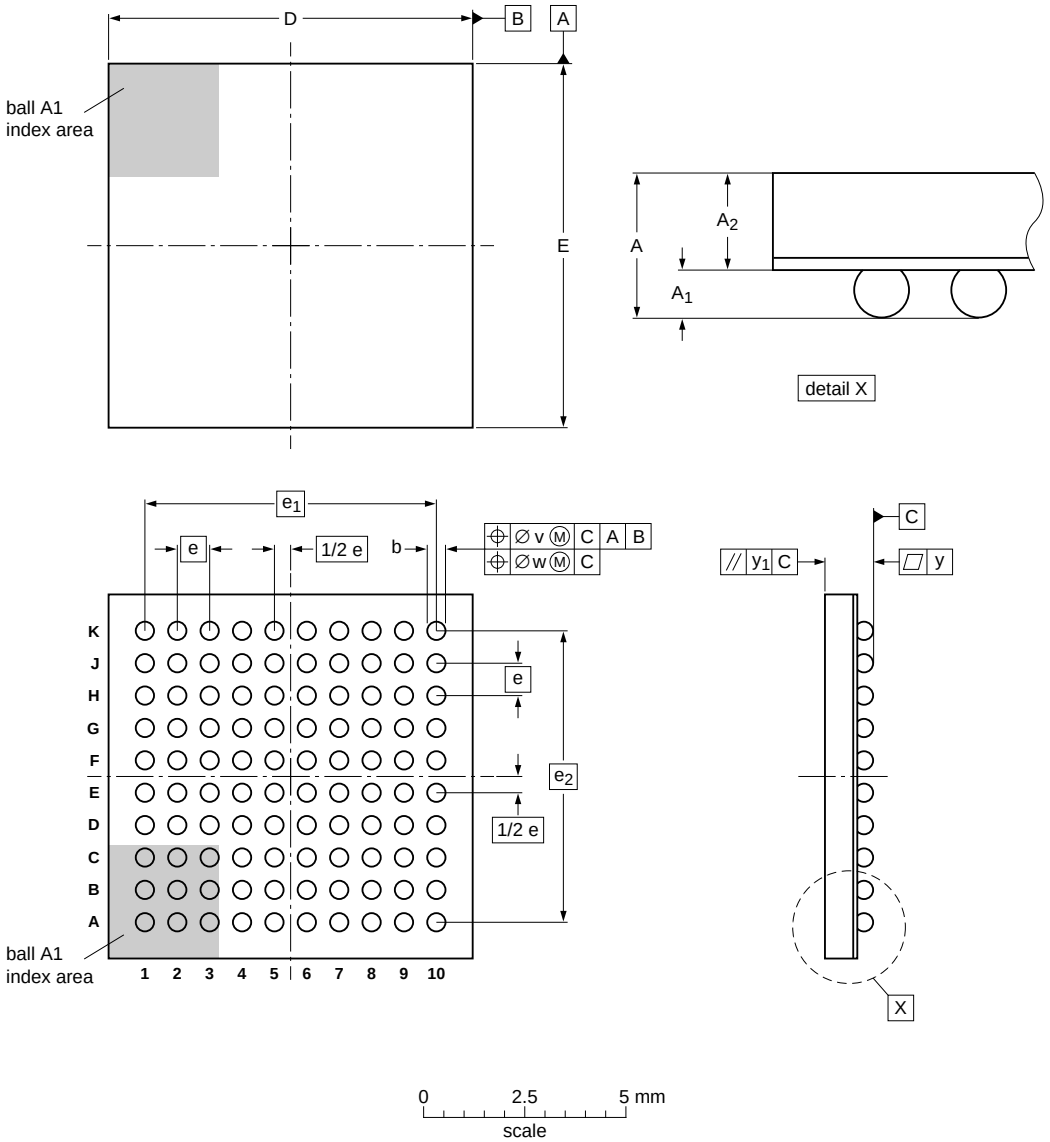
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 13. Package outline SOT407-1 (LQFP100)

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 14. Package outline SOT926-1 (TFBGA100)

17. Abbreviations

Table 134. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DID	Device ID
DWORD	Double Word
ED	Endpoint Descriptor
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMI	ElectroMagnetic Interference
EOF	End-Of-Frame
EOP	End-Of-Packet
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
HC	Host Controller
HCCA	Host Controller Communication Area
HCD	Host Controller Driver
HCI	Host Controller Interface
HS	High-Speed
LS	Low-Speed
OHCI	Open Host Controller Interface
PCI	Peripheral Component Interconnect
PCI-SIG	PCI-Special Interest Group
PLL	Phase-Locked Loop
PMC	Power Management Capabilities
PME	Power Management Event
POR	Power-On Reset
POST	Power-On System Test
RoHS	Restriction of Hazardous Substances
SOF	Start-Of-Frame
STB	Set-Top Box
TD	Transfer Descriptor
USB	Universal Serial Bus
VID	Vendor ID

18. References

[1] **Universal Serial Bus Specification —** Rev. 2.0

[2] **Enhanced Host Controller Interface Specification for Universal Serial Bus —** Rev. 1.0

[3] **Open Host Controller Interface Specification for USB —** Rev. 1.0a

[4] **PCI Local Bus Specification —** Rev. 2.2

[5] **PCI Bus Power Management Interface Specification —** Rev. 1.1

[6] **The I^2C-bus Specification —** Version 2.1

19. Revision history

Table 135. Revision history

Revision	Release date	Data sheet status	Change notice
3	20100105	Product data sheet	-
Modifications:	• Updated the filename according to the new standards. • Section 4 “Ordering information”: updated. • Table 2 “Pin description”: added Table note 3. • Section 7.9 “PCI reset at power up”: added. • Table 117 “System Tuning register bit description”: updated description for bits 1 and 0. • Table 118 “Limiting values”: added Table note 1.		
2	20090716	Product data sheet	-
1	20090615	Product data sheet	-

20. Tables

continued >>

continued >>

21. Figures

22. Contents

continued >>

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