



TS5A9411 10-Ω 1:2 SPDT Analog Switch Single-Channel 2:1 Multiplexer and Demultiplexer

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance
(10-Ω Maximum at $V_{CC} = 5\text{ V}$)
- Low Power Consumption
- TTL- and CMOS-Compatible Control Input
- Low Input and Output Capacitance
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion
- 2.25-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA
Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model
(A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Control Inputs Are 5.5-V Tolerant

2 Applications

- Cell Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample-and-Hold Circuits

3 Description

The TS5A9411 device is a bidirectional, single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers low ON-state resistance, low leakage, and low power with a break-before-make feature. These features make this device suitable for portable and battery-powered applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A9411	SOT (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

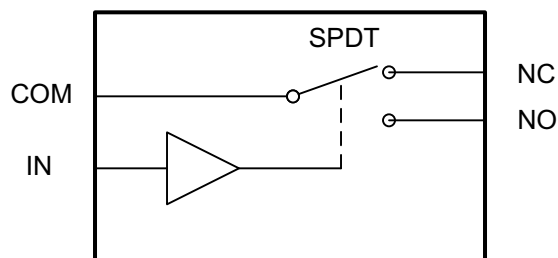


Table of Contents

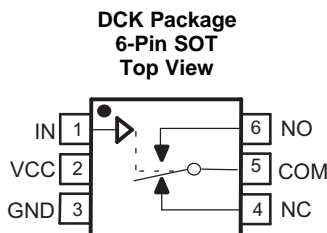
1 Features	1	8.3 Feature Description	12
2 Applications	1	8.4 Device Functional Modes	12
3 Description	1	9 Application and Implementation	13
4 Revision History	2	9.1 Application Information	13
5 Pin Configuration and Functions	3	9.2 Typical Application	13
6 Specifications	3	10 Power Supply Recommendations	14
6.1 Absolute Maximum Ratings	3	11 Layout	14
6.2 ESD Ratings	3	11.1 Layout Guidelines	14
6.3 Recommended Operating Conditions	4	11.2 Layout Example	14
6.4 Thermal Information	4	12 Device and Documentation Support	15
6.5 Electrical Characteristics: 5-V Supply	4	12.1 Device Support	15
6.6 Electrical Characteristics: 3-V Supply	5	12.2 Documentation Support	16
6.7 Electrical Characteristics: 2.5-V Supply	6	12.3 Receiving Notification of Documentation Updates	16
6.8 Typical Characteristics	7	12.4 Community Resources	16
7 Parameter Measurement Information	8	12.5 Trademarks	16
8 Detailed Description	12	12.6 Electrostatic Discharge Caution	16
8.1 Overview	12	12.7 Glossary	16
8.2 Functional Block Diagram	12	13 Mechanical, Packaging, and Orderable Information	17

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2008) to Revision B	Page
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>Specifications</i> section, <i>ESD Ratings</i> table, <i>Recommended Operating Conditions</i> table, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table; see <i>Package Option Addendum</i> at the end of the data sheet	1
• Deleted <i>Summary of Characteristics</i> table	1
• Moved ON-state switch current and ON-state peak switch current From: <i>Absolute Maximum Ratings</i> table To: <i>Recommended Operating Conditions</i> table	4
• Added <i>Thermal Information</i> table	4
• Changed Package thermal impedance, $R_{\theta JA}$, value in <i>Thermal Information</i> table From: 259°C/W To: 346.7°C/W	4
• Deleted <i>Charge Injection vs V_{COM}</i> graph from <i>Typical Characteristics</i>	7
• Changed graph title From: OFF Isolation vs Crosstalk ($V_{CC} = 3$ V) To: Crosstalk and Insertion Loss vs Frequency ($V_{CC} = 3$ V) in <i>Typical Characteristics</i>	7
• Changed $V+$ to V_{CC} and IN to V_{IN} on all images in <i>Parameter Measurement Information</i>	8

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	5	I/O	Common signal path
GND	3	—	Digital ground
IN	1	I	Digital control input. High = COM connected to NO; Low = COM connected to NC.
NC	4	I/O	Normally closed signal path
NO	6	I/O	Normally open signal path
VCC	2	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply voltage	−0.3	6	V
Analog voltage ⁽³⁾	−0.3	$V_{CC} + 0.3$	V
Digital input voltage	−0.5	$V_{CC} + 0.3$	V
Analog port diode current ($V_{NC}, V_{NO}, V_{COM} < 0$)	−50		mA
Digital input clamp current ($V_I < 0$)	−50		mA
Continuous current through VCC		100	mA
Continuous current through GND	−100		mA
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) This value is limited to 5.5 V (maximum).

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.25	5.5	V
V _{NO}	Analog voltage	0	V _{CC}	V
V _{NC}		0	V _{CC}	
V _{COM}		0	V _{CC}	
V _I	Digital input voltage	0	5.5	V
	ON-state switch current (V _{NO} , V _{NC} , V _{COM} = 0 to V _{CC})	–50	50	mA
	ON-state peak switch current (V _{NO} , V _{NC} , V _{COM} = 0 to V _{CC}) ⁽¹⁾	–200	200	mA

(1) Pulse at 1-ms duration < 10% duty cycle

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5A9411	UNIT
		DCK (SOT)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	346.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	163.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	154.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	17.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	153.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: 5-V Supply

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
r _{ON}	ON-state resistance	V _{NO} or V _{NC} = 3 V, V _{CC} = 4.5 V, I _{COM} = −10 mA, Switch ON, see Figure 5	T _A = 25°C	5.3	9	Ω	
			−40°C ≤ T _A ≤ 85°C		10		
Δr _{ON}	ON-state resistance match between channels	V _{NO} or V _{NC} = 3 V, V _{CC} = 4.5 V, I _{COM} = −10 mA, Switch ON, see Figure 5	T _A = 25°C	0.03	0.3	Ω	
			−40°C ≤ T _A ≤ 85°C		0.3		
r _{ON(FLAT)}	ON-state resistance flatness	0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , V _{CC} = 4.5 V, I _{COM} = −10 mA, Switch ON, see Figure 5		2		Ω	
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V _{NC} or V _{NO} = 1 V and V _{COM} = 1 V to 4.5 V, or V _{NC} or V _{NO} = 4.5 V and V _{COM} = 1 V; V _{CC} = 5.5 V, Switch OFF, see Figure 6	T _A = 25°C	−500	500	pA	
			−40°C ≤ T _A ≤ 85°C	−3	3	nA	
I _{NC(ON)} , I _{NO(ON)}	NC, NO ON leakage current	V _{NC} or V _{NO} = 1 V and V _{COM} = 1 V, or V _{NC} or V _{NO} = 4.5 V and V _{COM} = 4.5 V; V _{CC} = 5.5 V, Switch ON, see Figure 7	T _A = 25°C	−500	500	pA	
			−40°C ≤ T _A ≤ 85°C	−3	3	nA	
I _{COM(ON)}	COM ON leakage current	V _{NC} or V _{NO} = Open, V _{COM} = 1 V or 4.5 V, V _{CC} = 5.5 V, Switch ON, see Figure 7	T _A = 25°C	−500	500	pA	
			−40°C ≤ T _A ≤ 85°C	−3	3	nA	
DIGITAL INPUT (IN) ⁽¹⁾							
V _{IH}	Input logic high	−40°C ≤ T _A ≤ 85°C	4.5 V ≤ V _{CC} ≤ 5.5 V	2.4	5.5	V	
			V _{CC} = 4.5 V	2	5.5		
V _{IL}	Input logic low	4.5 V ≤ V _{CC} ≤ 5.5 V, −40°C ≤ T _A ≤ 85°C		0	0.8	V	
I _{IH} , I _{IL}	Input leakage current	V _I = 5.5 V or 0, V _{CC} = 5.5 V	T _A = 25°C	−0.05	0.05	μA	
			−40°C ≤ T _A ≤ 85°C	−0.05	0.05		
DYNAMIC							
t _{ON}	Turnon time	V _{COM} = 3 V, R _L = 300 Ω, C _L = 35 pF, see Figure 9	V _{CC} = 5 V, T _A = 25°C		9	ns	
			4.5 V ≤ V _{CC} ≤ 5.5 V, −40°C ≤ T _A ≤ 85°C		10		

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

Electrical Characteristics: 5-V Supply (continued)

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF} Turnoff time	$V_{COM} = 3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 9 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$			7 7.5	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = 3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 10 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		1 0.9		ns
Q_C Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, see Figure 14		12.5		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$ NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$ NC, NO ON capacitance	V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, see Figure 8		8.5		pF
$C_{COM(ON)}$ COM ON capacitance	$V_{COM} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch ON, see Figure 8		8.5		pF
C_I Digital input capacitance	$V_I = V_{CC}$ or GND, $f = 1\text{ MHz}$, see Figure 8		25		pF
BW Bandwidth	$R_L = 50\ \Omega$, Switch ON, see Figure 11		100		MHz
O_{ISO} OFF isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Switch OFF, see Figure 12		-84		dB
X_{TALK} Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Switch ON, see Figure 13		-85		dB
THD Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz , see Figure 15		0.03%		
SUPPLY					
I_{CC} Positive supply current	$V_I = V_{CC}$ or GND, $V_{CC} = 5.5\text{ V}$, Switch ON or OFF $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.01 0.5		μA

6.6 Electrical Characteristics: 3-V Supply

 $V_{CC} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH					
r_{ON} ON-state resistance	V_{NO} or $V_{NC} = 1.5\text{ V}$, $V_{CC} = 2.7\text{ V}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		11.5 20	15	Ω
Δr_{ON} ON-state resistance match between channels	V_{NO} or $V_{NC} = 1.5\text{ V}$, $V_{CC} = 2.7\text{ V}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.05 0.3	0.3	Ω
$r_{ON(FLAT)}$ ON-state resistance flatness	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5		2		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$ NC, NO OFF leakage current	V_{NC} or $V_{NO} = 1\text{ V}$ and $V_{COM} = 1\text{ V}$ to 3 V , or V_{NC} or $V_{NO} = 3\text{ V}$ and $V_{COM} = 1\text{ V}$; $V_{CC} = 3.3\text{ V}$, Switch OFF, see Figure 6 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-400 -2		400 2	pA nA
$I_{NC(ON)}$, $I_{NO(ON)}$ NC, NO ON leakage current	V_{NC} or $V_{NO} = 1\text{ V}$ and $V_{COM} = 1\text{ V}$, or V_{NC} or $V_{NO} = 3\text{ V}$ and $V_{COM} = 3\text{ V}$; $V_{CC} = 3.3\text{ V}$, Switch ON, see Figure 7 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-400 -2		400 2	pA nA
$I_{COM(ON)}$ COM ON leakage current	V_{NC} or $V_{NO} = \text{Open}$, $V_{COM} = 1\text{ V}$ or 3 V , $V_{CC} = 3.3\text{ V}$, Switch ON, see Figure 7 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-400 -2		400 2	pA nA
DIGITAL INPUT (IN)⁽¹⁾					
V_{IH} Input logic high	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	2		5.5	V
V_{IL} Input logic low	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0		0.8	V
I_{IH} , I_{IL} Input leakage current	$V_I = 5.5\text{ V}$ or 0 , $V_{CC} = 3.6\text{ V}$ $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-0.05 -0.05		0.05 0.05	μA
DYNAMIC					
t_{ON} Turnon time	$V_{COM} = 3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 9 $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ $2.7\text{ V} \leq V_{CC} \leq 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$			13 15	ns
t_{OFF} Turnoff time	$V_{COM} = 3\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 9 $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ $2.7\text{ V} \leq V_{CC} \leq 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$			7.5 8.5	ns
t_{BBM} Break-before-make time	$V_{NC} = V_{NO} = 3\text{ V}$, $R_L = 300\ \Omega$, $V_{CC} = 3.3\text{ V}$, $C_L = 35\text{ pF}$, see Figure 10 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		1 0.9		ns
Q_C Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, see Figure 14		6		pC

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

Electrical Characteristics: 3-V Supply (continued)

 $V_{CC} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		8.5		pF
$C_{COM(ON)}$	COM ON capacitance $V_{COM} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		8.5		pF
C_I	Digital input capacitance $V_I = V_{CC}$ or GND, $f = 1\text{ MHz}$, see Figure 8		2.5		pF
BW	Bandwidth $R_L = 50\ \Omega$, Switch ON, see Figure 11		100		MHz
O_{ISO}	OFF isolation $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, Switch OFF, see Figure 12		–84		dB
X_{TALK}	Crosstalk $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, Switch ON, see Figure 13		–85		dB
THD	Total harmonic distortion $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz , see Figure 15		0.09%		
SUPPLY					
I_{CC}	Positive supply current $V_I = V_{CC}$ or GND, $V_{CC} = 3.6\text{ V}$, Switch ON or OFF	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.01	0.5	μA

6.7 Electrical Characteristics: 2.5-V Supply

 $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH					
r_{ON}	ON-state resistance V_{NO} or $V_{NC} = 1\text{ V}$, $V_{CC} = 2.25\text{ V}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	15	25	Ω
Δr_{ON}	ON-state resistance match between channels V_{NO} or $V_{NC} = 1\text{ V}$, $V_{CC} = 2.25\text{ V}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.06	0.3	Ω
$r_{ON(FLAT)}$	ON-state resistance flatness $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $V_{CC} = 2.25\text{ V}$, $I_{COM} = -10\text{ mA}$, Switch ON, see Figure 5		4		Ω
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current V_{NC} or $V_{NO} = 1.5\text{ V}$ and $V_{COM} = 0.5\text{ V}$ to 1.5 V , or V_{NC} or $V_{NO} = 1.5\text{ V}$ and $V_{COM} = 1.5\text{ V}$; $V_{CC} = 2.75\text{ V}$, Switch OFF, see Figure 6	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	–300	300	pA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current V_{NC} or $V_{NO} = 1.5\text{ V}$ and $V_{COM} = 0.5\text{ V}$ to 1.5 V , or V_{NC} or $V_{NO} = 1.5\text{ V}$ and $V_{COM} = 1.5\text{ V}$; $V_{CC} = 2.75\text{ V}$, Switch ON, see Figure 7	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	–300	300	pA
$I_{COM(ON)}$	COM ON leakage current V_{NC} or $V_{NO} = \text{Open}$, $V_{COM} = 0.5\text{ V}$ or 1.5 V , $V_{CC} = 2.75\text{ V}$, Switch ON, see Figure 7	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	–300	300	pA
DIGITAL INPUT (IN)⁽¹⁾					
V_{IH}	Input logic high	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	2	5.5	V
V_{IL}	Input logic low	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0	0.4	V
I_{IH} , I_{IL}	Input leakage current $V_I = 5.5\text{ V}$ or 0 V , $V_{CC} = 2.75\text{ V}$	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	–0.05	0.05	μA
DYNAMIC					
t_{ON}	Turnon time $V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 9	$V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ $2.25\text{ V} \leq V_{CC} \leq 2.75\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	18	20	ns
t_{OFF}	Turnoff time $V_{COM} = 2\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 9	$V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ $2.25\text{ V} \leq V_{CC} \leq 2.75\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	8	9.5	ns
t_{BBM}	Break-before-make time $V_{NC} = V_{NO} = 2\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 10	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	1	0.9	ns
Q_C	Charge injection $V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, see Figure 14		4.5		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		3.5		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance V_{NC} or $V_{NO} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		8.5		pF

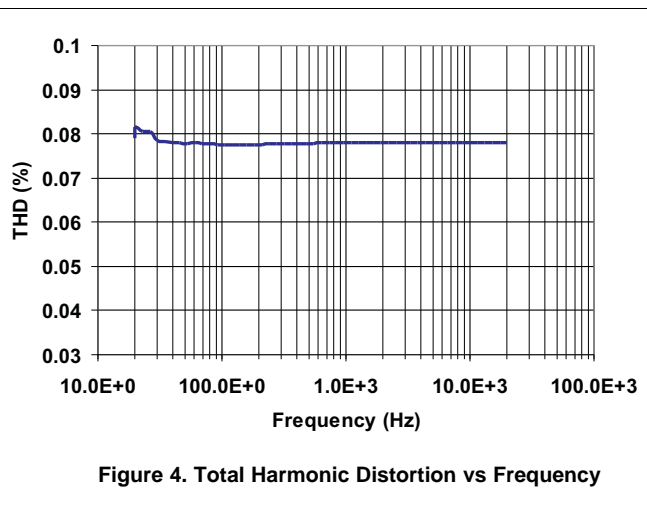
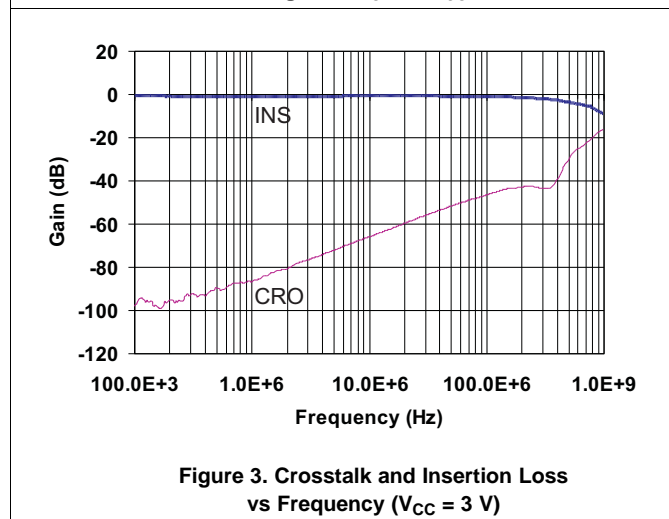
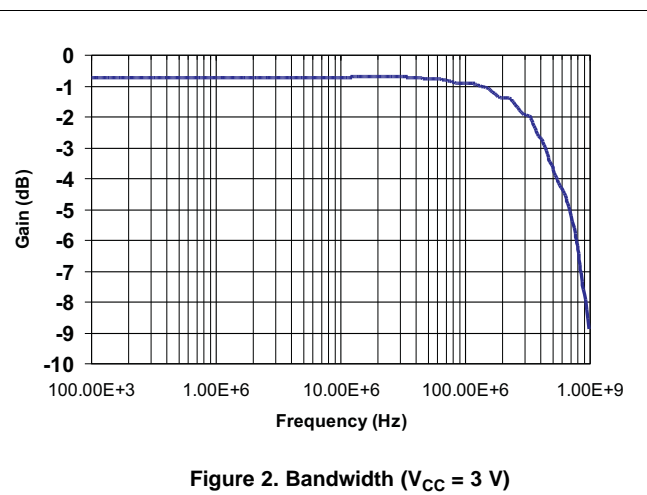
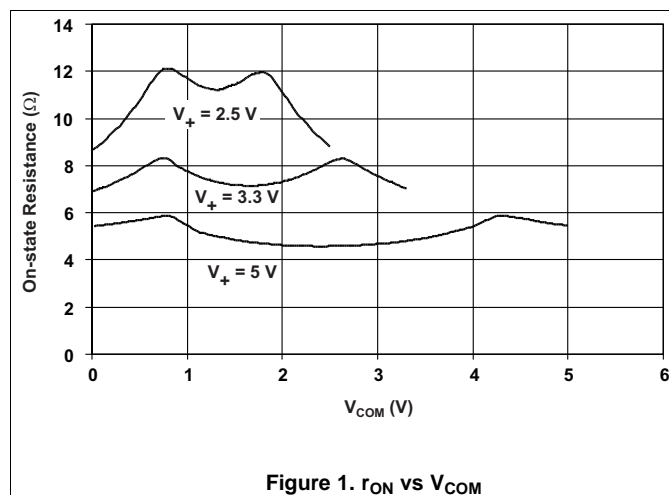
(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

Electrical Characteristics: 2.5-V Supply (continued)

$V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{COM(ON)}$	COM ON capacitance $V_{COM} = V_{CC}$ or GND, $f = 1\text{ MHz}$, Switch OFF, see Figure 8		8.5		pF
C_i	Digital input capacitance $V_i = V_{CC}$ or GND, $f = 1\text{ MHz}$, see Figure 8		2.5		pF
BW	Bandwidth $R_L = 50\ \Omega$, Switch ON, see Figure 11		100		MHz
O_{ISO}	OFF isolation $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, Switch OFF, see Figure 12		-84		dB
X_{TALK}	Crosstalk $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, Switch ON, see Figure 13		-84		dB
THD	Total harmonic distortion $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz , see Figure 15		0.15%		
SUPPLY					
I_{CC}	Positive supply current $V_i = V_{CC}$ or GND, $V_{CC} = 2.75\text{ V}$, Switch ON or OFF	$T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.01 0.5	μA

6.8 Typical Characteristics



7 Parameter Measurement Information

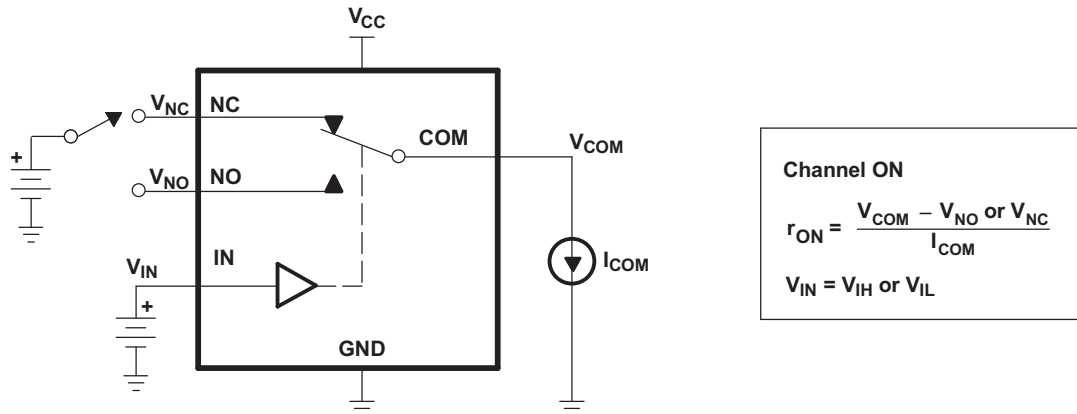


Figure 5. ON-State Resistance

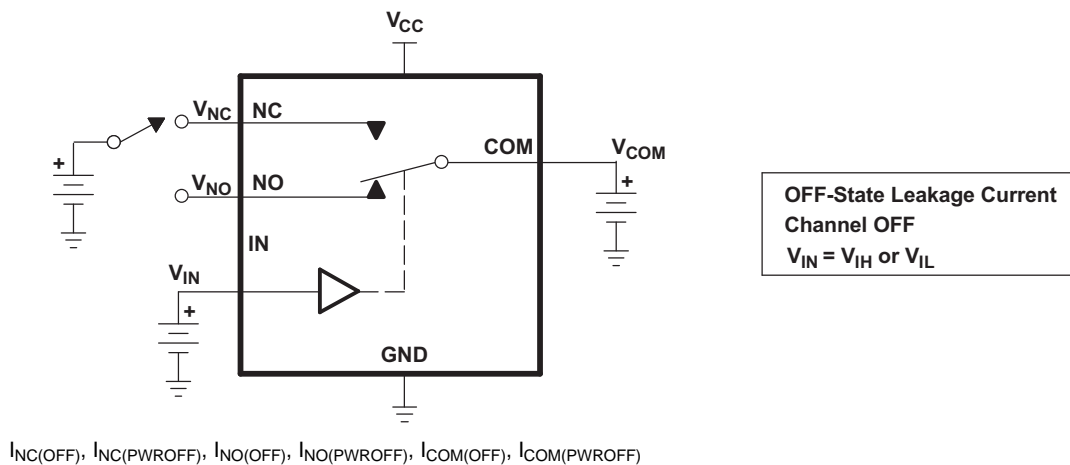


Figure 6. OFF-State Leakage Current

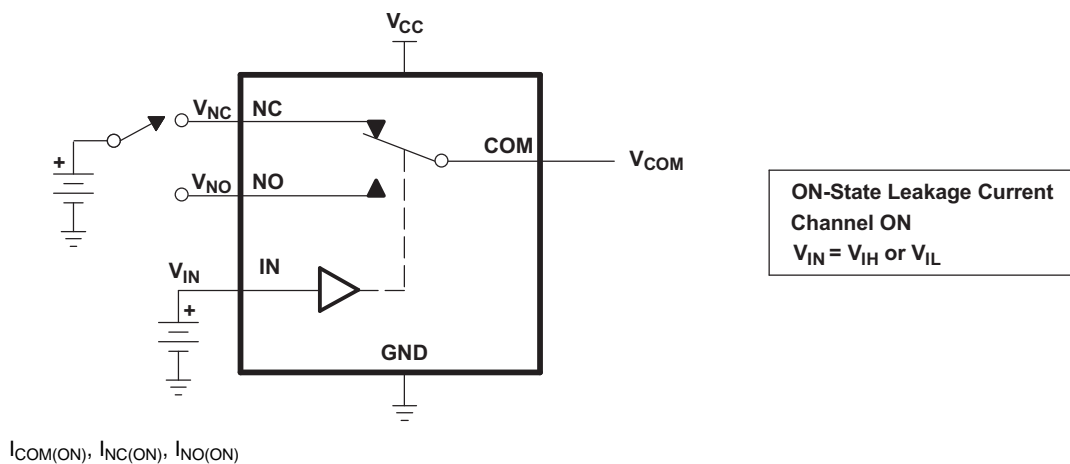


Figure 7. ON-State Leakage Current

Parameter Measurement Information (continued)

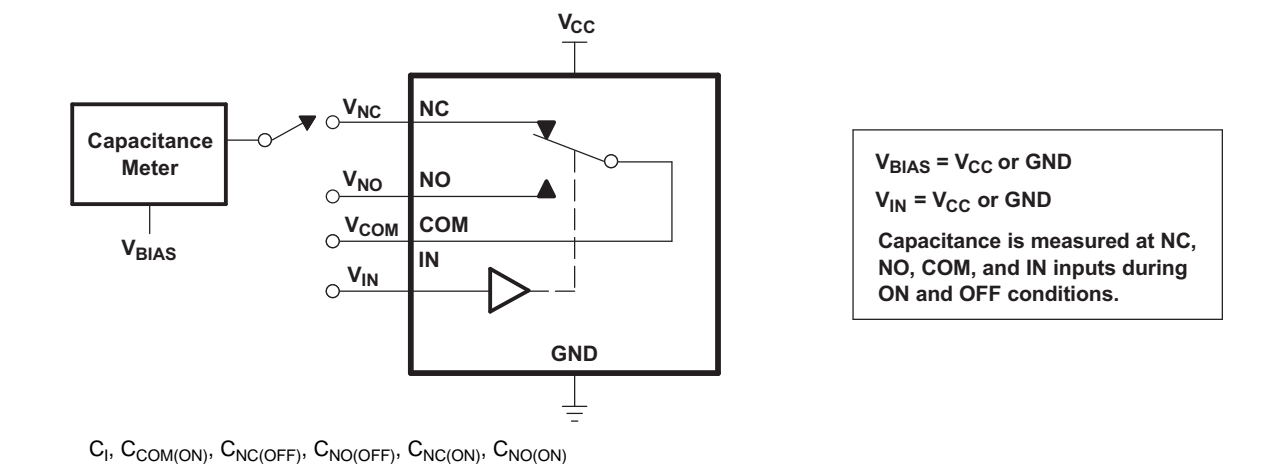
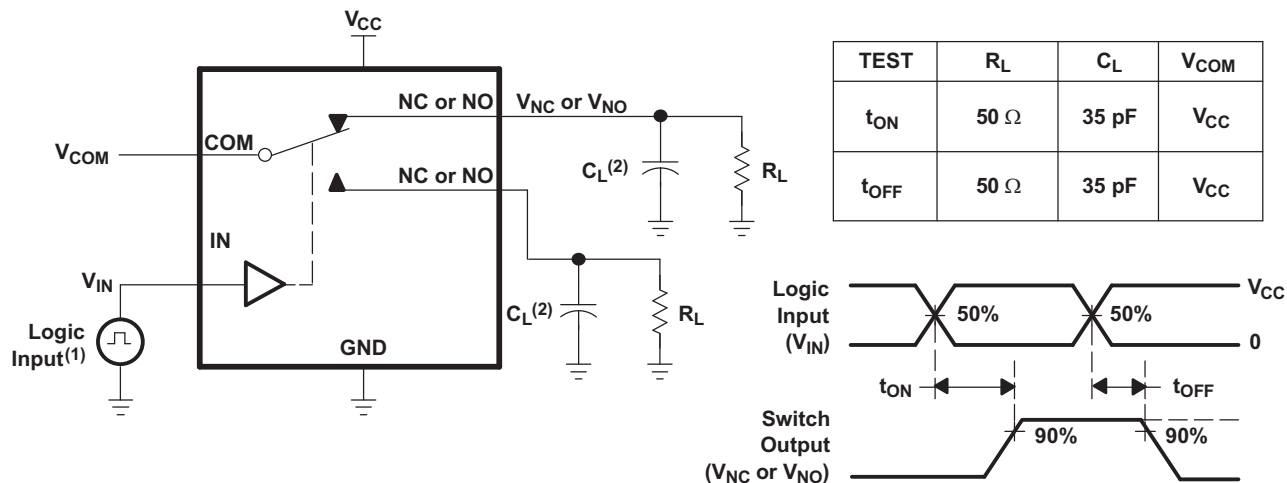


Figure 8. Capacitance



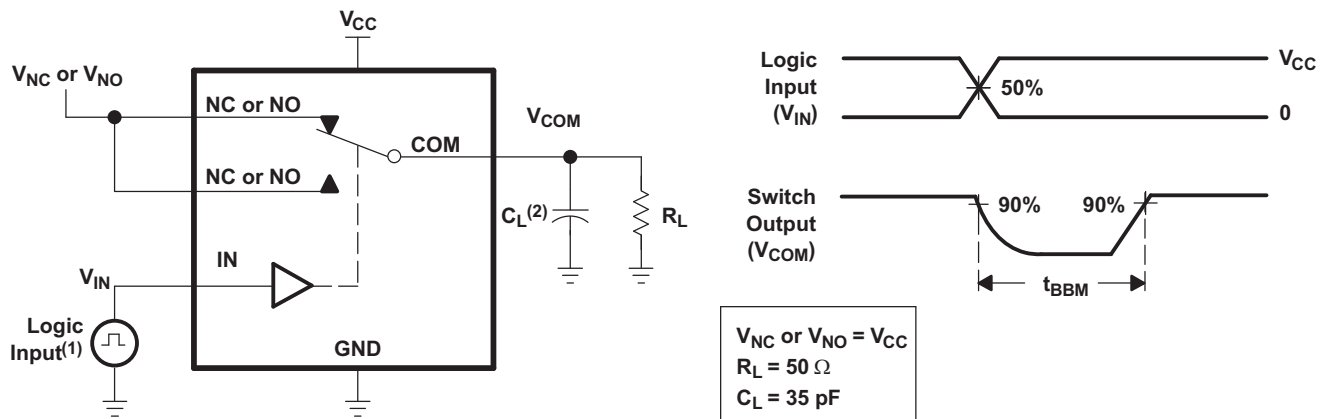
(1) All input pulses are supplied by generators having the following characteristics:

- $PRR \leq 10\ \text{MHz}$
- $Z_O = 50\ \Omega$
- $t_r < 5\ \text{ns}$
- $t_f < 5\ \text{ns}$

(2) C_L includes probe and jig capacitance.

Figure 9. Turnon and Turnoff Time

Parameter Measurement Information (continued)



- (1) All input pulses are supplied by generators having the following characteristics:
 - $\text{PRR} \leq 10\ \text{MHz}$
 - $Z_O = 50\ \Omega$
 - $t_r < 5\ \text{ns}$
 - $t_f < 5\ \text{ns}$
- (2) C_L includes probe and jig capacitance.

Figure 10. Break-Before-Make Time

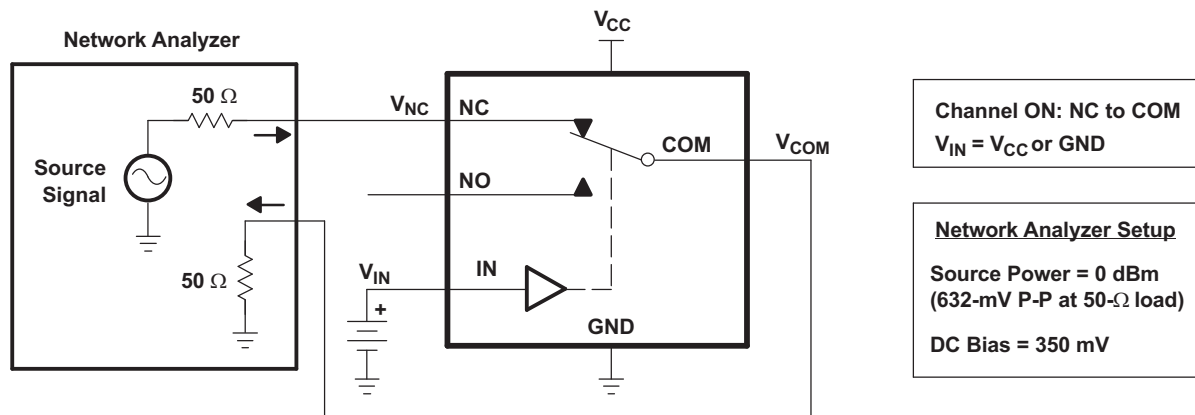


Figure 11. Bandwidth

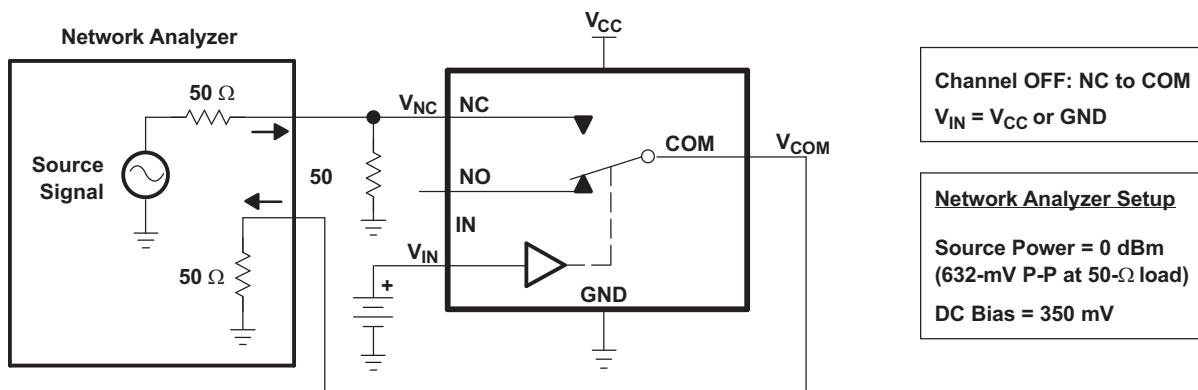


Figure 12. OFF Isolation

Parameter Measurement Information (continued)

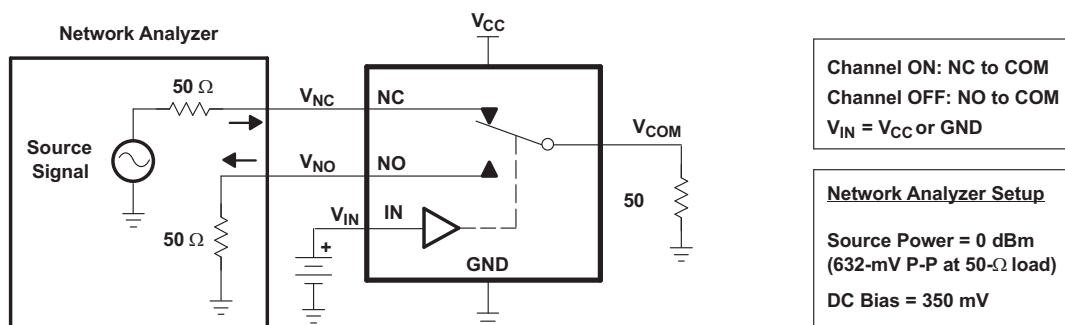
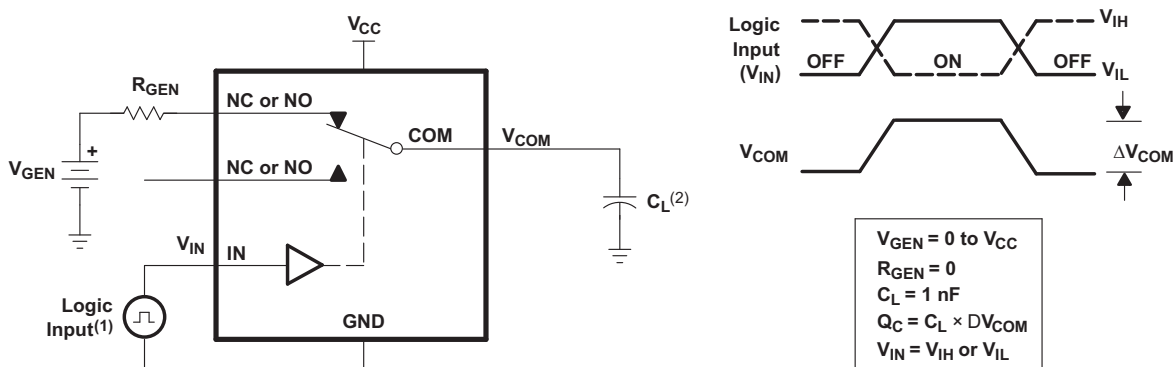
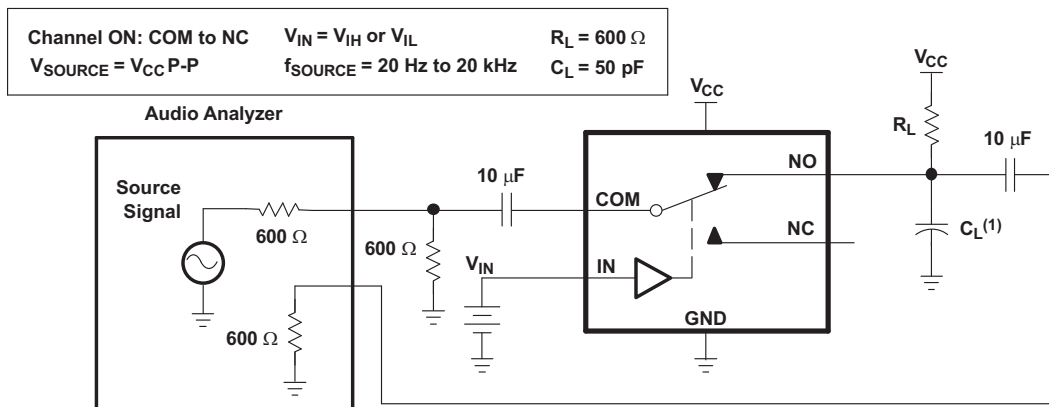


Figure 13. Crosstalk



- (1) All input pulses are supplied by generators having the following characteristics:
- $PRR \leq 10$ MHz
 - $Z_O = 50 \Omega$
 - $t_r < 5$ ns
 - $t_f < 5$ ns
- (2) C_L includes probe and jig capacitance.

Figure 14. Charge Injection



- (1) C_L includes probe and jig capacitance.

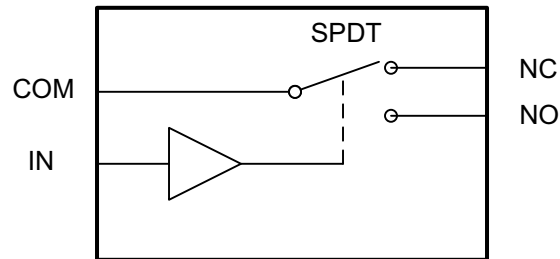
Figure 15. Total Harmonic Distortion

8 Detailed Description

8.1 Overview

The TS5A9411 device is a 1:2 or single-pole-double-throw (SPDT) solid-state analog switch. The TS5A9411, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin or NO pin depending on the status of the IN pin. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO. The TS5A9411 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A9411 make this switch an excellent choice for analog signals that require minimal distortion. The 2.25-V to 5.5-V operation allows compatibility with more voltage nodes, and the bidirectional I/Os can pass analog signals from 0 V to V_{CC} with low distortion.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the TS5A9411. If IN pin is low, COM is connected to NC. If IN is high, COM is connected to NO.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs. The device is used in systems where multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

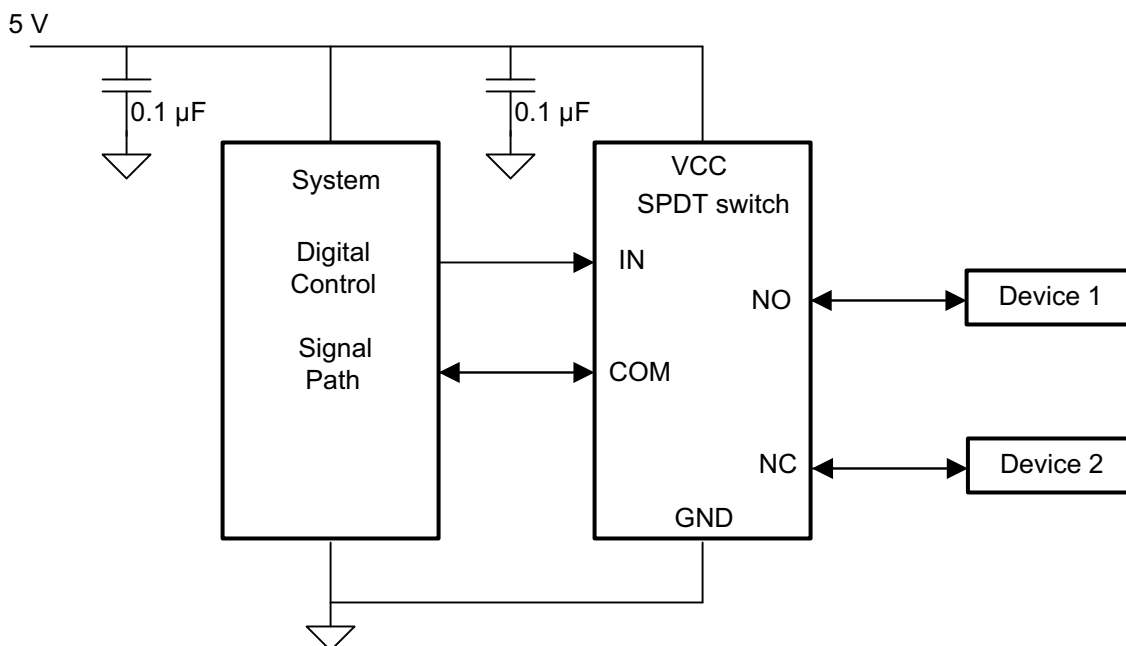


Figure 16. Typical Application Diagram

9.2.1 Design Requirements

Pull the digitally controlled input select pin (IN) to V_{CC} or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the input or output signal swing of the device is dependant of the supply voltage (V_{CC}).

Typical Application (continued)

9.2.3 Application Curve

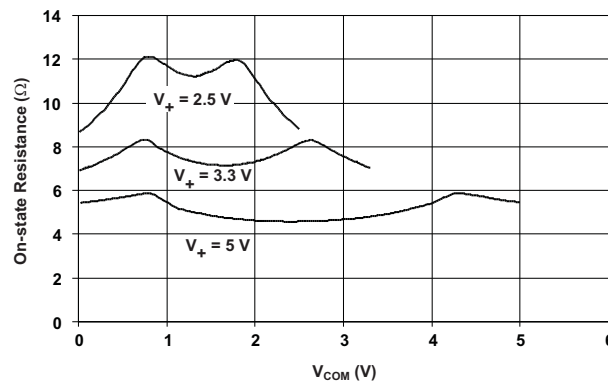


Figure 17. r_{ON} vs V_{COM}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM pins.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pins (VCC and –VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

11.2 Layout Example

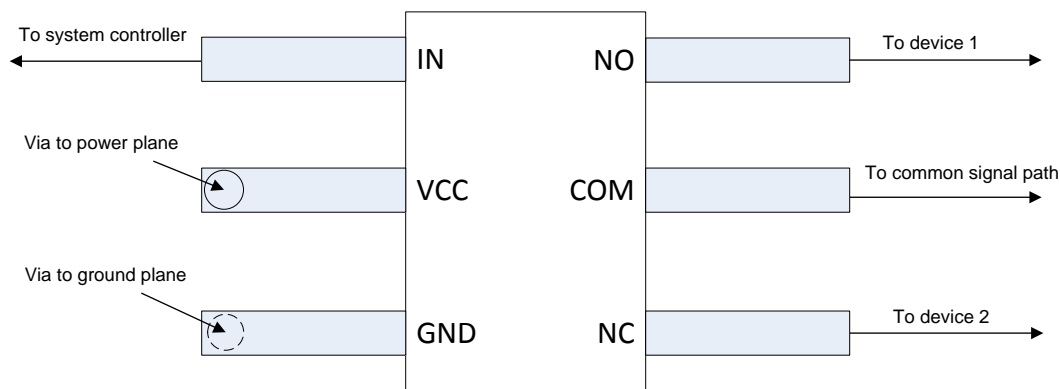


Figure 18. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
C_{COM(ON)}	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON.
C_{NC(OFF)}	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.
C_{NC(ON)}	Capacitance at the NC port when the corresponding channel (NC to COM) is ON.
C_{NO(OFF)}	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF.
C_{NO(ON)}	Capacitance at the NO port when the corresponding channel (NO to COM) is ON.
C_I	Capacitance of control input (IN).
I_{CC}	Static power-supply current with the control (IN) pin at V _{CC} or GND.
I_{COM(ON)}	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open.
I_{COM(PWROFF)}	Leakage current measured at the COM port during the power-down condition (V _{CC} = 0).
I_{IH}, I_{IL}	Leakage current measured at the control input (IN).
I_{NC(OFF)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.
I_{NC(ON)}	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.
I_{NO(OFF)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions.
I_{NO(ON)}	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open.
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
Δr_{ON}	Difference of r_{ON} between channels in a specific device.
r_{ON}	Resistance between COM and NC or COM and NO ports when the channel is ON.
r_{ON(FLAT)}	Difference of r_{ON} in a channel over the specified range of conditions.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is

Device Support (continued)

defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.

V_{COM}	Voltage at COM.
V_I	Voltage at the control input (IN).
V_{IH}	Minimum input voltage for logic high for the control input (IN).
V_{IL}	Maximum input voltage for logic low for the control input (IN).
V_{NC}	Voltage at NC.
V_{NO}	Voltage at NO.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A9411DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F, 32R) (32H, 32P)	Samples
TS5A9411DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F, 32R) 32H	Samples
TS5A9411DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F, 32R) 32H	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



www.ti.com

PACKAGE OPTION ADDENDUM

24-Aug-2018

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A9411DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A9411DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A9411DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A9411DCKT	SC70	DCK	6	250	202.0	201.0	28.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.