PTN3393

2-lane DisplayPort to VGA adapter IC

Rev. 4 — 10 June 2014 Product data sheet

1. General description

The PTN3393 is a DisplayPort to VGA adapter IC designed to connect a DisplayPort source to a VGA sink. The PTN3393 integrates a DisplayPort receiver and a high-speed triple video digital-to-analog converter that supports display resolutions from VGA to WUXGA (see Table 5). The PTN3393 supports either one or two DisplayPort v1.1a lanes operating at either 2.7 Gbit/s or 1.62 Gbit/s per lane. The PTN3393 has 'Flash-over-AUX' capability enabling simple firmware upgradability in the field.

The PTN3393 supports I^2C-bus over AUX per *DisplayPort v1.1a specification* (Ref. 1), and bridges the VESA DDC channel to the DisplayPort Interface.

The PTN3393 is designed for single supply and minimizes application costs. It can be powered directly from the DisplayPort source side 3.3 V supply without a need for additional core voltage regulator. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. The PTN3393 also aids in monitor detection by performing load sensing and reporting sink connection status to the source.

2. Features and benefits

2.1 VESA-compliant DisplayPort v1.1a converter

- Main Link: 1-lane and 2-lane modes supported
  - HBR (High Bit Rate) at 2.7 Gbit/s per lane
  - RBR (Reduced Bit Rate) at 1.62 Gbit/s per lane
  - BER (Bit Error Rate) better than 10^{-9}
  - Down-spreading SSC (Spread Spectrum Clocking) supported
- 1 MHz AUX channel
  - Supports native AUX CH syntax
  - Supports I^2C-bus over AUX CH syntax
- Hot Plug Detect (HPD) signal to the source
- Cost-effective design optimized for VGA application

2.2 DDC channel output

- Supports 100 kbit/s I^2C-bus speed, declared in DPCD register
  - Support of I^2C-bus speed control by DisplayPort source via DPCD registers, facilitating use of longer VGA cables
- I^2C Over Aux feature facilitates full support of MCCS, DDC-CI, and DDC protocols (see Ref. 2)

2.3 Analog video output

- VSIS 1.2 compliance (Ref. 3) for all supported video output modes
- Analog RGB current-source outputs
- VSYNC and HSYNC outputs
- Pixel clock up to 240 MHz
- Triple 8-bit Digital-to-Analog Converter (DAC)
- Direct drive of double terminated 75 Ω load with standard 700 mV (peak-to-peak) signals

2.4 General features

- Supports 'Flash-over-AUX' field upgradability
- Monitor presence detection. Connection/disconnection reported via HPD IRQ and DPCD update.
- All display resolutions from VGA to WUXGA are supported[1], including e.g.:
  - WUXGA: 6 bits, 1920 × 1200, 60 Hz, 193 MHz pixel clock rate
  - WUXGA: 1920 × 1200, 60 Hz, reduced blanking, 154 MHz pixel clock rate
  - UXGA: 1600 × 1200, 60 Hz, 162 MHz pixel clock rate
  - SXGA: 1280 × 1024, 60 Hz, 108 MHz pixel clock rate
  - XGA: 1024 × 768, 60 Hz, 65 MHz pixel clock rate
  - SVGA: 800 × 600, 60 Hz, 40 MHz pixel clock rate
  - VGA: 640 × 480, 60 Hz, 25 MHz pixel clock rate
  - Any resolution and refresh rates are supported up to 8 bit color
- Bits per color (bpc) supported[1]
  - 6, 8 bits supported
  - 10, 12, 16 bits supported by truncation to 8 MSBs
- All VGA colorimetry formats (RGB) supported
- Power modes
  - Active-mode power consumption:
    ~600 mW at UXGA / 162 MHz pixel clock
    ~500 mW at SXGA / 108 MHz pixel clock
  - ~40 mW at Low-power mode or before link training started
- On-board crystal oscillator for use with external 27 MHz crystal
- ESD protection: 7 kV ESD HBM JEDEC
- 3.3 V ± 10 % power supply
- Commercial temperature range: 0 °C to 85 °C
- 40-pin HVQFN, 6 mm × 6 mm × 0.85 mm (nominal); 0.5 mm pitch; lead-free package

1. Except for color depth beyond 8 bits, display resolutions and refresh rates are only limited to those which a standard 2-lane DisplayPort configuration is able to support.

3. Applications

- Dongle PC accessory
  - Dongle connected to PC DisplayPort output and connected to RGB monitor via VGA cable
  - PTN3393 is powered by the DP_PWR pin on the DisplayPort connector
- Desktop and notebook computers
- Notebook docking stations

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN3393BS[1]	PTN3393	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; 6 × 6 × 0.85 mm	SOT618-6
PTN3393BS/FX[2]	PTN3393	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; 6 × 6 × 0.85 mm	SOT618-6

[1] PTN3393BS uses latest firmware version.

[2] PTN3393BS/FX uses specific firmware version ('X' = 1, 2, 3, etc., and changes according to firmware version).

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3393BS[1]	PTN3393BSY	HVQFN40	Reel 13" Q1/T1 *Standard mark SMD dry pack	4000	T_{amb} = 0 °C to +85 °C
PTN3393BS/FX[2]	PTN3393BS/FXY	HVQFN40	Reel 13" Q1/T1 *Standard mark SMD dry pack	4000	T_{amb} = 0 °C to +85 °C

[1] PTN3393BS uses latest firmware version.

[2] PTN3393BS/FX uses specific firmware version ('X' = 1, 2, 3, etc., and changes according to firmware version).

5. Functional diagram

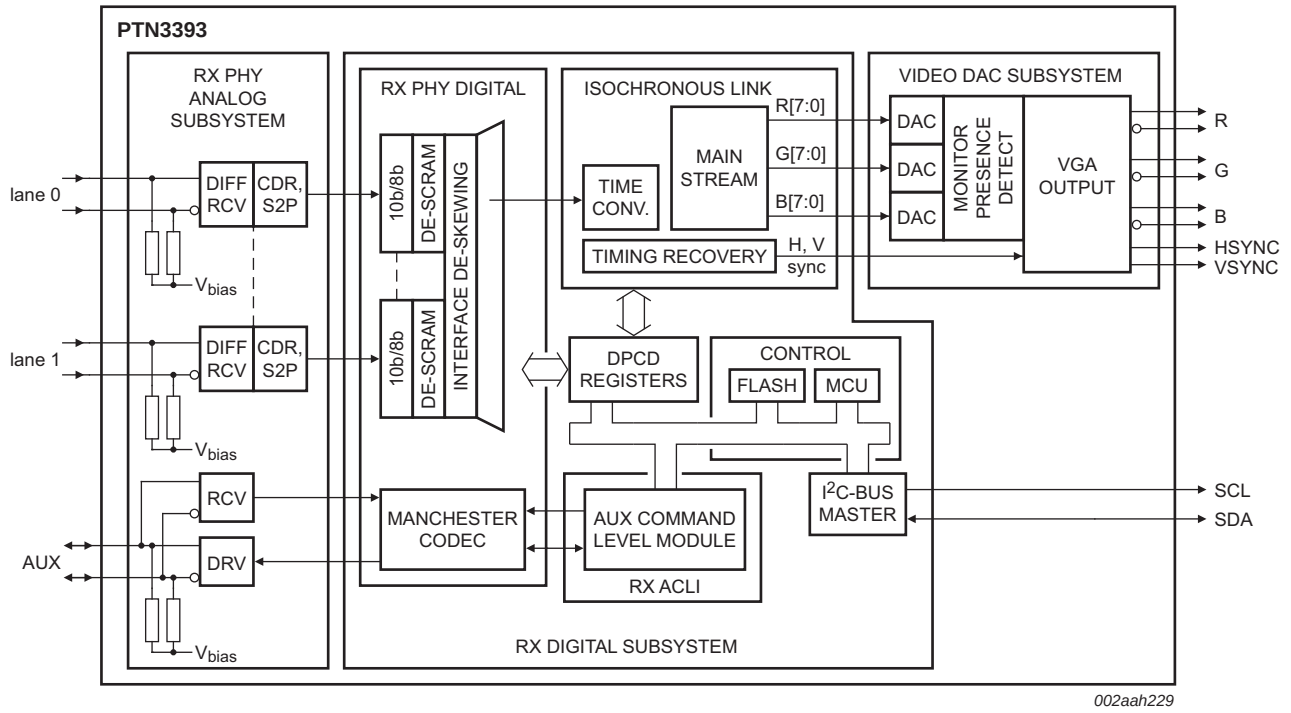


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

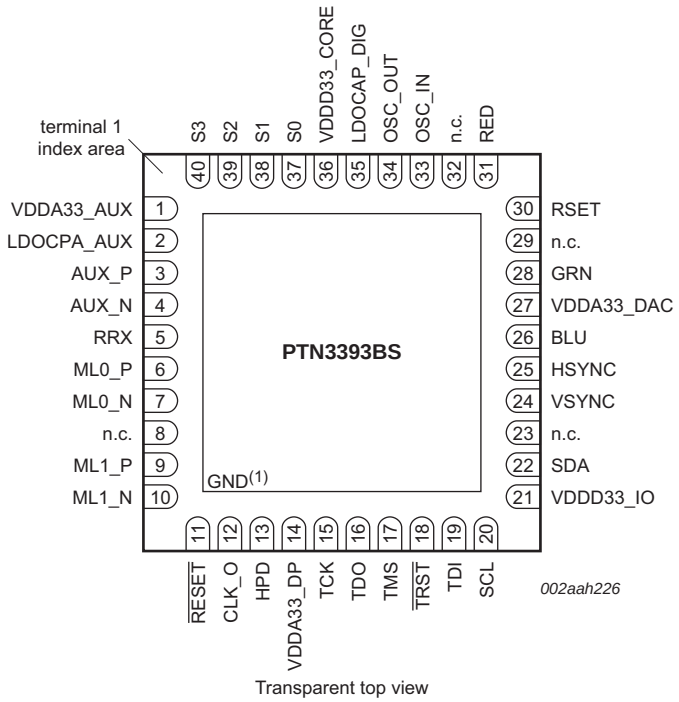


Fig 2. Pin configuration for HVQFN40

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Power			
VDDD33_CORE	36	power	Digital core 3.3 V supply voltage
VDDA33_AUX	1	power	Analog AUX, bias and PLL 3.3 V supply voltage
VDDA33_DP	14	power	Analog 3.3 V supply for DisplayPort receiver module
VDDD33_IO	21	power	I/O 3.3 V supply voltage
VDDA33_DAC	27	power	Analog 3.3 V supply for DAC
LDOCAP_AUX	2	power	1.8 V AUX supply decoupling
LDOCAP_DIG	35	power	1.8 V digital core supply decoupling
DisplayPort			
ML0_P	6	self-biasing differential input	DisplayPort main lane signal lane 0, positive
ML0_N	7	self-biasing differential input	DisplayPort main lane signal lane 0, negative
ML1_P	9	self-biasing differential input	DisplayPort main lane signal lane 1, positive
ML1_N	10	self-biasing differential input	DisplayPort main lane signal lane 1, negative
AUX_P	3	self-biasing differential input/output	DisplayPort auxiliary channel signal, positive
AUX_N	4	self-biasing differential input/output	DisplayPort auxiliary channel signal, negative
HPD	13	3.3 V TTL single-ended output	Hot Plug Detect
RGB DAC outputs			
BLU	26	analog output	‘blue’ current analog output
GRN	28	analog output	‘green’ current analog output
RED	31	analog output	‘red’ current analog output
RSET	30	analog input/output	DAC full-scale current control resistor. Pull down to ground by an external 1.2 kΩ ± 1 % resistor.
DDC			
SCL	20	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC clock I/O. Pulled up by external resistor to 5 V.
SDA	22	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC data I/O. Pulled up by external resistor to 5 V.
Monitor-side sync			
HSYNC	25	single-ended 3.3 V TTL output	horizontal sync signal to monitor
VSYNC	24	single-ended 3.3 V TTL output	vertical sync signal to monitor

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
JTAG			
TCK	15	input	JTAG clock input
TDO	16	output	JTAG data output
TMS	17	input	JTAG mode select input
$\overline{\text{TRST}}$	18	input	JTAG reset (active LOW) input
TDI	19	input	JTAG data input
Miscellaneous			
S0	37	input	Open (internal pull-down) = logic 0 Implement VGA-side monitor detect according to *VESA DisplayPort Standard v1.1a*, sections 7 and 8. HIGH (external pull-up) = logic 1 Set HPD HIGH upon VGA monitor detection; set HPD LOW upon VGA monitor detachment.
S1	38	input	reserved; leave open-circuit (default internal pull-down)
S2	39	input	Open (internal pull-down) = logic 0 to set default I^2C-bus speed to 50 kbit/s. HIGH (external pull-up) = logic 1, to set default I^2C-bus speed to 10 kbit/s. This pin may be left open-circuit (internal pull-down) or tied to V_{DD} according to the desired default I^2C-bus speed. See more explanation about S2 pin setting and DPCD register 00109h.
S3	40	input	reserved; leave open-circuit (default internal pull-down)
$\overline{\text{RESET}}$	11	input	Hardware reset input (active LOW); internal pull-up. A capacitor must be connected between this pin and ground. A 1 μF capacitor is recommended.
CLK_O	12	output	DisplayPort receiver test clock output
OSC_IN	33	input	crystal oscillator input
OSC_OUT	34	output	crystal oscillator output
RRX	5	input	Receiver termination resistance control. A 12 kΩ resistor must be connected between this pin and LDOCAP_AUX (pin 2).
n.c.	8, 23, 29, 32	-	not connected
GND[1]	-	power	central supply ground connection (exposed die pad)

[1] HVQFN40 package die supply ground is connected to exposed center pad. Exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

7. Functional description

Referring to Figure 1 “Functional diagram”, the PTN3393 converts the DisplayPort AC-coupled high-speed differential signaling protocol into a VESA VSIS 1.2 compliant analog VGA signaling. The PTN3393 integrates a DisplayPort receiver (according to *VESA DisplayPort v1.1a specification*, Ref. 1) and a high-speed triple 8-bit video digital-to-analog converter that supports display resolution from VGA to WUXGA (see Table 5 “Display resolution and pixel clock rate[1]”), up to a pixel clock rate of 240 MHz. The PTN3393 supports one or two DisplayPort v1.1a Main Link lanes operating at either in 2.7 Gbit/s or 1.62 Gbit/s per lane. The PTN3393 can drive up to 100 feet of analog video cable.

The DisplayPort receiver comprises the following functional blocks:

- Main Link
- AUX CH (Auxiliary Channel)
- DPCD (DisplayPort Configuration Data)
- Monitor detection
- EDID handling
- Video DAC

The RGB video data with corresponding synchronization references is extracted from the main stream video data. Main stream video attribute information is also extracted. This information is inserted once per video frame during the vertical blanking period by the DisplayPort source. The attributes describe the main video stream format in terms of geometry, timing, and color format. The original clock and video stream are derived from these main link data.

The PTN3393 internal DPCD registers can be accessed by the source via the auxiliary channel. The monitor’s DDC control bus may also be controlled via the auxiliary channel. A bridging conversion block translates the input DisplayPort auxiliary channel signals from the source side to the DDC signals on the sink side. The PTN3393 passes through sink-side status change (for example, hot-plug events) to the source side, through HPD interrupts and DPCD registers.

7.1 DisplayPort Main Link

The DisplayPort main link consists of doubly terminated, AC-coupled differential pair. The 50 Ω internally calibrated termination resistors are integrated inside PTN3393.

The PTN3393 supports HBR at 2.7 Gbit/s and RBR at 1.62 Gbit/s per lane.

7.2 DisplayPort auxiliary channel

The AUX CH is a half-duplex, bidirectional channel between DisplayPort transmitter and receiver. It consists of one differential pair transporting self-clocked data at 1 Mbit/s. The PTN3393 integrates the AUX CH replier (or slave), and responds to transactions initiated by the DisplayPort source AUX CH requester (or master).

The AUX CH uses the Manchester-II code for the self-clocked transmission of signals; every ‘zero’ is represented by LOW-to-HIGH transition, and ‘one’ represented by HIGH-to-LOW transition, in the middle of the bit time.

7.3 DPCD registers

DPCD registers that are part of the VESA DisplayPort v1.1a are described in detail in Ref. 1. The following paragraphs only describe the specific implementation by PTN3393.

The PTN3393 DisplayPort receiver capability and status information about the link are reported by DisplayPort Configuration Data (DPCD) registers, when a DisplayPort source issues a read command on the AUX CH. The DisplayPort source device can also write to the link configuration field of DPCD to configure and initialize the link. The DPCD is DisplayPort v1.1a compliant.

It is the responsibility of the host to only issue commands within the capability of the PTN3393 as defined in the ‘Receiver Capability Field’ in order to prevent undefined behavior. PTN3393 specific DPCD registers are listed in Table 4.

7.3.1 PTN3393 specific DPCD register settings

Table 4. PTN3393 specific DPCD registers

DPCD register [1]	Description	Power-on Reset value	Read/write over AUX CH
Receiver Capability Field			
0000Bh	RECEIVE_PORT1_CAP_1. ReceiverPort1 Capability_1.	00h	read only
0000Ch	I^2C-bus speed control capabilities bit map. The bit values in this register are assigned to I^2C-bus speeds as follows: Bits 7:0 0000 0001b = 1 kbit/s; supported by PTN3393 0000 0010b = 3 kbit/s; supported by PTN3393 0000 0100b = 10 kbit/s; supported by PTN3393 0000 1000b = 100 kbit/s; supported by PTN3393 0001 0000b = 400 kbit/s; not supported by PTN3393 0010 0000b = 1 Mbit/s; not supported by PTN3393 0100 0000b = reserved 1000 0000b = 50 kbit/s; supported by PTN3393BS/F3 1000 0000b = reserved in PTN3393BS/F1, PTN3393BS/F2	8Fh	read only
Automated testing subfield (optional)			
00218h to 0027Fh	Not supported.		
Branch device-specific field			
00500h	BRANCH_IEEE_OUI 7:0 Branch vendor 24-bit IEEE OUI. NXP OUI = 00	00h	read only
00501h	BRANCH_IEEE_OUI 15:8 NXP OUI = 60	60h	read only
00502h	BRANCH_IEEE_OUI 23:16 NXP OUI = 37	37h	read only
00503h	ID string = 3392N2	33h	read only
00504h		33h	read only
00505h		39h	read only
00506h		32h	read only
00507h		4Eh	read only
00508h		32h	read only
00509h	Hardware revision level v1.2	12h	read only
0050Ah, 0050Bh	Major revision level (example: **v1**.38), Minor revision level (example: v1.**38**)	01h, 26h	read only
0050Ch to 005FFh	RESERVED		read only

[1] Byte fields that are not explicitly listed are by definition reserved ('RES') and their default value is 0h.

7.3.2 I²C over AUX CH registers

7.3.2.1 I²C-bus speed control register (read only, 0000Ch)

Bit or bits are set to indicate I²C-bus speed control capabilities.

DisplayPort source reads register 0000Ch and sets the I²C-bus speed according to the DPCD register 00109h setting. The PTN3393 then adapts its I²C-bus bit rate to the speed set by the DisplayPort source.

7.3.2.2 I²C-bus speed control/status register (read/write, 00109h)

Bit values in this register are assigned to I²C-bus speeds.

Prior to software writing to this register, PTN3393 defaults to the I²C-bus speed (either 50 kbit/s or 10 kbit/s) selected by the S2 pin (Table 3).

On read, the PTN3393 returns a value set to indicate the speed currently in use.

On write, software provides a mask to limit the speeds to be enabled:

- The PTN3393 uses the slowest speed enabled by the mask and the PTN3393 speed capabilities.
- If the result of the mask with the speed capabilities is 0000 0000b, then the PTN3393 keeps the S2 setting I²C-bus speed that it is using before the software write (that is, no change).

Some specific examples are listed below for clarification purposes:

- If the source writes 1111 1111b, the PTN3393 uses the lowest speed of 1 kbit/s.
- If the source writes 0000 1100b, the PTN3393 uses the lower of 10 kbit/s and 100 kbit/s, that is, 10 kbit/s.
- If the source writes 0011 0000b, the PTN3393 would stay using the same I²C-bus speed that it is using before the software write (that is, no change).

For DDC communication, the PTN3393 generates defer responses to the source while the I²C-bus transfer is taking place as specified in the *DisplayPort standard v1.1a*. Note that when the I²C-bus bit rate is set to 1 kbit/s, each bit takes 1 ms. One byte including I2C_ACK takes 9 ms. Given this, the DisplayPort source should expect over 20 I2C_DEFER's when requesting to read a byte over I²C-bus at the slowest rate.

7.4 Monitor detection

The PTN3393 assumes 75 Ω double termination, as shown in Figure 6. The load sensing circuit of the PTN3393 senses a 37.5 Ω or 75 Ω termination respectively, when the monitor is connected or disconnected. The load-sensing circuit is active during the vertical blanking period (never during the horizontal retrace period), so that there is no disturbance to the screen image caused by the load-sensing circuit.

Upon detection of an RGB monitor being connected, the PTN3393 dynamically updates DPCD register 00200h and 00204h, to indicate the presence of a sink device being connected (see Section 7.3). After updating the DPCD register 00200h, the PTN3393 generates an IRQ request on HPD.

The PTN3393 implements two different ways to handle the HPD signal. The HPD behavior is governed by the S0 pin's value after the reset and initialization sequence is completed (see Figure 3).

- If S0 is tied LOW, HPD is driven HIGH irrespective of whether a VGA monitor is detected.
- If S0 pin is tied HIGH, HPD is only driven HIGH when a monitor is detected.

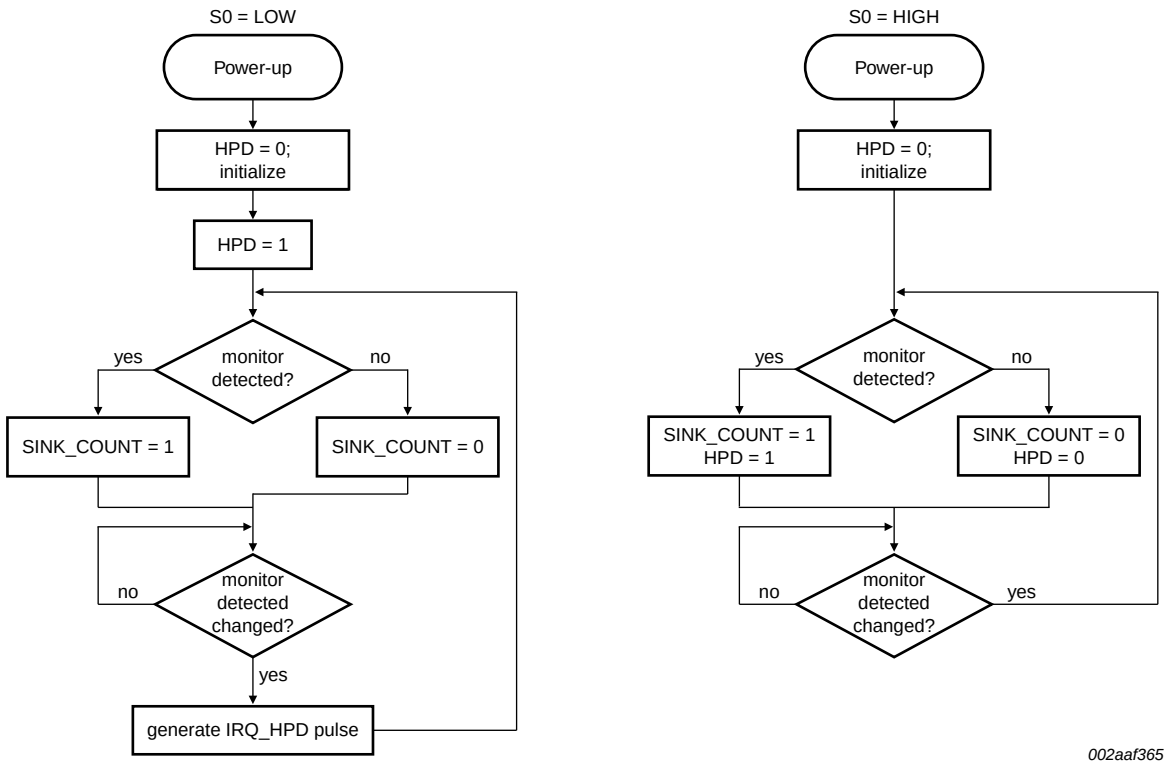


Fig 3. Pin S0 behavior

7.4.1 S0 = logic 0

If S0 is left open-circuit (internal pull-down) (DisplayPort v1.1a compliant behavior), PTN3393 behaves as stated in *VESA DisplayPort v1.1a*, sections 7 and 8. PTN3393 will keep HPD LOW during its internal initialization sequence after power-up. It then updates DPCD register SINK_COUNT to the expected value, depending if a VGA monitor is detected or not, and then asserts HPD HIGH whatever is the value of SINK_COUNT register. Each time PTN3393 detects a change in the VGA monitor connection status, it updates the SINK_COUNT register accordingly, sets DOWNSTREAM_PORT_STATUS_CHANGED register bit to 1 and generates IRQ_HPD pulse to signal the source about the status change. Refer to Figure 3, S0 = LOW flowchart.

7.4.2 S0 = logic 1

If S1 is tied to HIGH with external pull-up (best interoperability behavior), the PTN3393 will keep HPD LOW during its internal initialization sequence after power-up. It then waits for a VGA monitor to be connected downstream before asserting HPD HIGH to force source waiting for a VGA monitor before starting protocol negotiations. If a VGA monitor is disconnected during normal operations, PTN3393 asserts HPD LOW so that the source considers that no sink device is connected anymore. Refer to Figure 3, S0 = HIGH flowchart.

7.5 EDID handling

Figure 4 shows a DisplayPort-to-analog video converter (or dongle) situated between the DisplayPort source and a VGA monitor. The PTN3393 converts a DP I^2C Over AUX request to I^2C on the monitor's DDC bus. The monitor's EDID read data is then returned to the DP source via an I^2C Over AUX response issued by the PTN3393.

It is the responsibility of the source to choose only video modes which are declared in the EDID and to adjust the DisplayPort link capabilities (link rate and lane count) to provide the necessary video bandwidth. The PTN3393 does not cache or modify the EDID to match the capabilities of the DisplayPort link data.

If the DisplayPort source drives display modes that are not specified in the EDID mode list, the PTN3393 does not detect such conditions, and displays at its output what it is presented by the DisplayPort source.

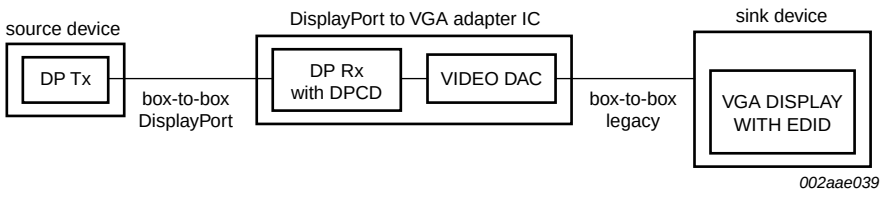


Fig 4. DisplayPort to VGA adapter IC (dongle) sits between the DisplayPort source and a VGA monitor with EDID

7.6 Triple 8-bit video DACs and VGA outputs

The triple 8-bit video DACs output a 700 mV (peak-to-peak) analog video output signal into 37.5 Ω load, as is the case of a doubly terminated 75 Ω cable. The DAC is capable of supporting the maximum pixel rate supported by a two-lane DP link (240 MHz).

The PTN3393 generates the RGB video timing and synchronization signals, RGB signals are then sent to the DACs for conversion to analog signals.

7.6.1 DAC reference resistor

An external reference resistor must be connected between pin RSET and analog ground. This resistor sets the reference current which determines the analog output level, and is specified as 1.2 kΩ with a 1 % tolerance. This value allows a 0.7 V (peak-to-peak) output into a 37.5 Ω load, such as a double-terminated 75 Ω coaxial cable.

8. Power-up and reset

PTN3393 has built-in power-on reset circuitry which automatically sequences the part through reset and initialization.

For proper behavior, a capacitor should be connected from the RESET_N pin to ground to slow down the internal reset pulse; 1 μF capacitance is recommended.

Before link is established, the PTN3393 holds VSYNC and HSYNC signals LOW and blanks the RGB signals.

While the PTN3393 performs initialization,

- The HPD signal is driven LOW, to indicate to the DisplayPort source that the PTN3393 is not ready for link communication
- The RED, GRN, BLU and complementary outputs (RED_N, GRN_N, BLU_N) are disabled
- The VSYNC and HSYNC outputs are driven LOW

9. Application design-in information

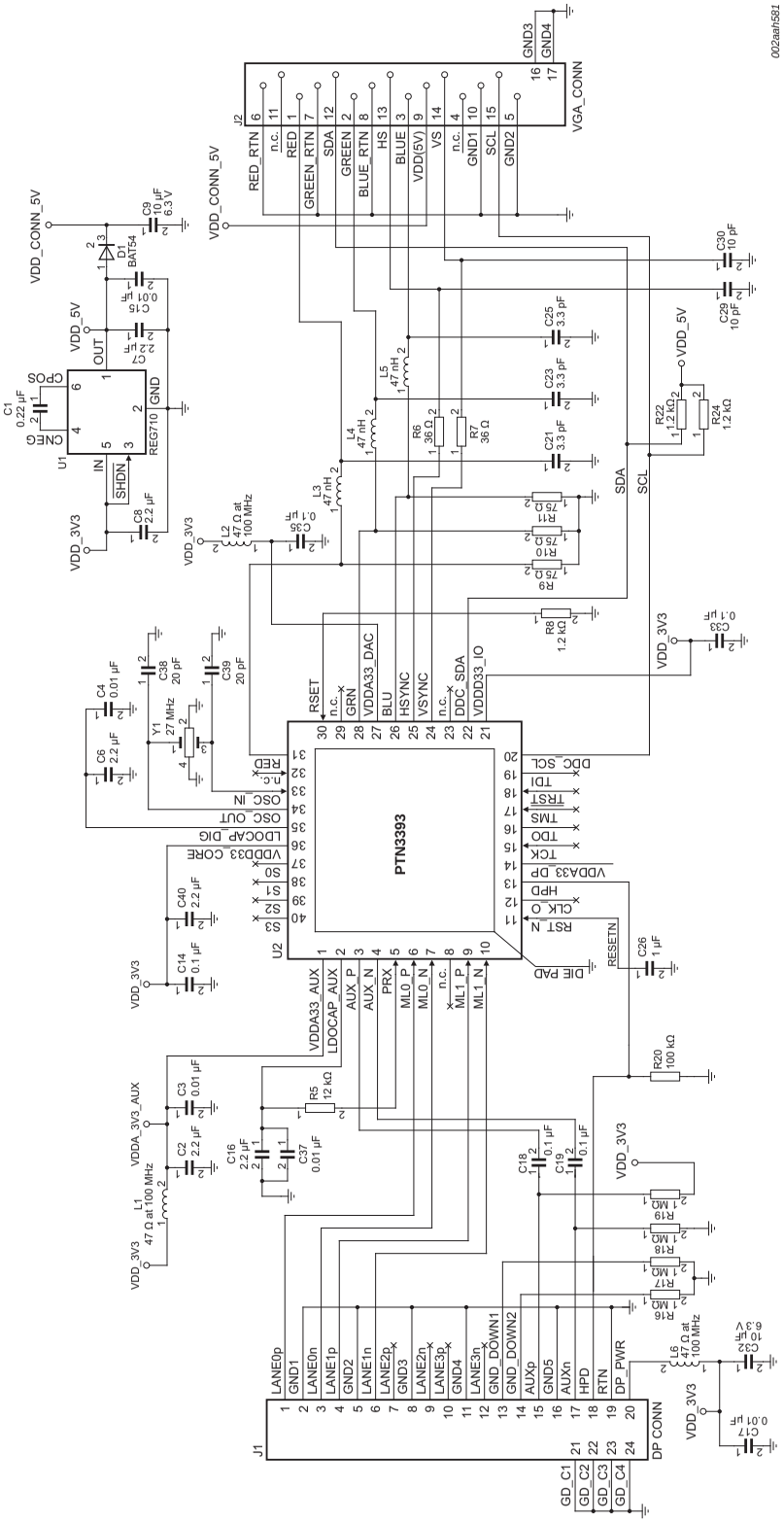


Fig 5. Application diagram

9.1 Display resolution

Table 5 lists some example display resolutions and clock rates that PTN3393 supports. (Refer to Footnote 1 on page 2.)

Table 5. Display resolution and pixel clock rate[1]

Display type	Active video		Total frame		Bits per pixel	Vertical frequency (Hz)	Pixel clock (MHz)	Data rate (Gbit/s)	Standard type
	Horizontal	Vertical	Horizontal total (pixel)	Vertical total (line)					
VGA	640	480	800	525	24	59.94	25.175	0.76	Industry standard
SVGA	800	600	1056	628	24	60.317	40.000	1.20	VESA guidelines
XGA	1024	768	1344	806	24	60.004	65.000	1.95	VESA guidelines
XGA+	1152	864	1600	900	24	75	108.000	3.24	VESA standard
HD	1360	768	1792	795	24	60.015	85.500	2.56	VESA standard
HD/WXGA	1366	768	1792	798	24	59.79	85.501	2.57	VESA standard
HD/WXGA	1280	720	1650	750	24	60	74.250	2.23	CEA standard
WXGA	1280	800	1680	831	24	59.81	83.500	2.50	CVT
WXGA	1280	800	1696	838	24	74.934	106.500	3.19	CVT
WXGA	1280	800	1712	843	24	84.88	122.500	3.68	CVT
SXGA–	1280	960	1800	1000	24	60	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	60.02	108.000	3.24	VESA standard
SXGA	1280	1024	1688	1066	24	75.025	135.001	4.05	VESA standard
SXGA	1280	1024	1728	1072	24	85.024	157.500	4.72	VESA standard
SXGA+	1400	1050	1864	1089	24	59.978	121.749	3.65	CVT
WXGA+	1440	900	1904	934	24	59.887	106.499	3.19	CVT
HD+	1600	900	1800	1000	24	60	108.000	3.24	VESA standard
UXGA	1600	1200	2160	1250	24	60	162.000	4.86	VESA standard
UXGA	1600	1200	2160	1250	24	65	175.500	5.27	VESA standard
WSXGA+	1680	1050	2240	1089	24	59.954	146.249	4.39	CVT
FHD	1920	1080	2200	1125	24	60	148.500	4.46	CEA standard
WUXGA	1920	1200	2592	1245	18	59.885	193.251	4.35	CVT
WUXGA	1920	1200	2080	1235	24	59.95	154.000	4.62	CVT RB
	1920	1440	2600	1500	18	60	234.000	5.27	CVT RB
QWXGA	2048	1152	2250	1200	24	60	162.000	4.86	VESA standard
QXGA	2048	1536	2144	1555	24	49.266	164.249	4.93	CVT

[1] Contact NXP team for other monitor timings not listed in this table.

The available bandwidth over a 2-lane HBR DisplayPort v1.1a link limits pixel clock rate support to:

- 240 MHz at 6 bpc
- 180 MHz at 8 bpc

9.2 Power supply filter

All supply pins can be tied to a single 3.3 V power source. Sufficient decoupling capacitance to ground should be connected from each V_{DD} pin directly to ground to filter supply noise. (Refer to Figure 5 “Application diagram”.)

9.3 DAC terminations

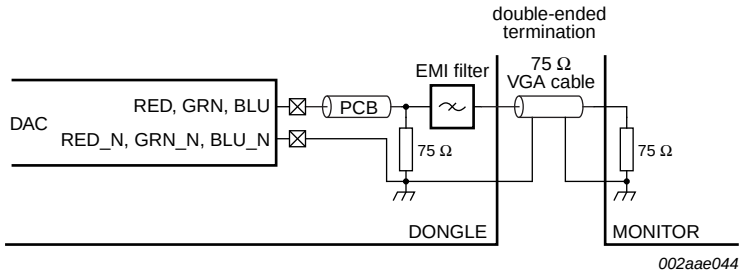


Fig 6. Recommended DAC terminations for PTN3393

We recommend the DAC outputs to use 75 Ω double termination. Figure 6 shows an example of VGA dongle application. A 75 Ω termination is used to terminate inside the dongle, and another 75 Ω termination is typically used inside the RGB monitor. The load sensing mechanism assumes this double termination.

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		−0.3	+3.8	V
V_{DDD}	digital supply voltage		−0.3	+4.6	V
V_I	input voltage	3.3 V CMOS inputs	−0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature		−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	7000	V
		CDM [2]	-	1000	V

[1] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[2] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

11. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_I	input voltage	3.3 V CMOS inputs	0	3.3	3.6	V
		SDA and SCL inputs with respect to ground	0	5	5.5	V
$V_{I(AV)}$	average input voltage	DC value at ML_LANE0+, ML_LANE0−, ML_LANE1+, ML_LANE1−, AUX_CH+, AUX_CH− inputs [1]	-	0	-	V
$R_{ext(RSET)}$	external resistance on pin RSET	between RSET (pin 22) and GND	-	1.2 ± 1 %	-	kΩ
T_{amb}	ambient temperature	commercial grade	0	-	85	°C

[1] Input signals to these pins must be AC-coupled.

12. Characteristics

12.1 Current consumption, power dissipation and thermal characteristics

Table 8. Current consumption, power dissipation and thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	normal operation, UXGA / 162 MHz pixel clock	-	180	-	mA
$I_{DD(stb)}$	standby supply current	Standby mode	-	12	-	mA
P	power dissipation	normal operation, UXGA / 162 MHz pixel clock	-	600	-	mW
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air for SOT619-1	-	35	-	K/W
R_{PU}	pull-up resistance	RESET_N pin; $0\ V \leq V_I \leq V_{DD}$	44	66	95	kΩ
R_{pd}	pull-down resistance	S0 to S3 pins; $0\ V \leq V_I \leq V_{DD}$	44	66	95	kΩ

12.2 DisplayPort receiver main link

Table 9. DisplayPort receiver main link characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval	for high bit rate (2.7 Gbit/s per lane)	[1]	-	370	-	ps
		for low bit rate (1.62 Gbit/s per lane)	[1]	-	617	-	ps
Δf_{DOWN_SPREAD}	link clock down spreading		[2]	0.0	-	0.5	%
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage	at RX package pins					
		for high bit rate	[3]	120	-	-	mV
		for reduced bit rate	[3]	40	-	-	mV
$t_{RX\_EYE\_CONN}$	receiver eye time at RX-side connector pins	for high bit rate	[4]	0.51	-	-	UI
		for reduced bit rate	[4][5]	0.25	-	-	UI
$t_{RX\_EYE\_CHIP}$	receiver eye time at RX package pins	for high bit rate	[4]	0.47	-	-	UI
		for reduced bit rate	[4][5]	0.22	-	-	UI
$t_{RX\_EYE\_m\text{-}mJT\_CHP}$	time between jitter median and maximum median deviation (package pins)	for high bit rate	[4]	-	-	0.265	UI
		for reduced bit rate	[4][5]	-	-	0.39	UI
$V_{RX\_DC\_CM}$	RX DC common mode voltage		[6]	0	-	2.0	V
I_{RX_SHORT}	RX short-circuit current limit		[7]	-	-	50	mA
$t_{sk(dif)}$	differential skew time	inter-pair; lane-to-lane skew at RX package pins	[8]	-	-	5200	ps
		lane intra-pair skew at RX package pins;					
		for high bit rate	[9]	-	-	100	ps
		for reduced bit rate	[9]	-	-	300	ps
$f_{RX\_TRACKING\_BW}$	jitter tracking bandwidth		[10]	20	-	-	MHz

[1] Range is nominal ±350 ppm. DisplayPort link RX does not require local crystal for link clock generation.

[2] Up to 0.5 % down spread is supported. Modulation frequency range of 30 kHz to 33 kHz must be supported.

[3] Informative; refer to Figure 7 for definition of differential voltage.

[4] $t_{RX\_EYE\_m\text{-}mJT\_CHP}$ specifies the total allowable Deterministic Jitter (DJ).

[5] $1 - t_{RX\_EYE\_CONN}$ specifies the allowable Total Jitter (TJ).

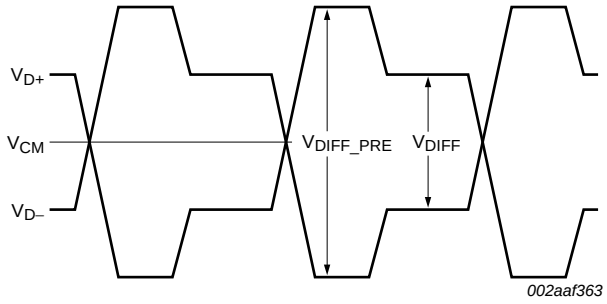
[6] Common mode voltage is equal to V_{bias_RX} voltage.

[7] Total drive current of the input bias circuit when it is shorted to its ground.

[8] Maximum skew limit between different RX lanes of a DisplayPort link.

[9] Maximum skew limit between D+ and D of the same lane.

[10] Minimum CDR tracking bandwidth at the receiver when the input is repetition of D10.2 symbols without scrambling.



pre-emphasis = 20Log(V_{DIFF_PRE} / V_{DIFF})

Fig 7. Definitions of pre-emphasis and differential voltage

12.3 DisplayPort receiver AUX CH

Table 10. DisplayPort receiver AUX CH characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UI	unit interval	AUX	[1]	0.4	0.5	0.6	μs
$N_{PRECHARGE\_PULSES}$	number of precharge pulses		[2]	10	-	16	
$t_{AUX\_BUS\_PARK}$	AUX CH bus park time		[3]	10	-	-	ns
$t_{jit(cc)}$	cycle-to-cycle jitter time	transmitting device	[4]	-	-	0.04	UI
		receiving device	[5]	-	-	0.05	UI
$V_{AUX\_DIFFp-p}$	AUX differential peak-to-peak voltage	transmitting device	[6]	0.39	-	1.38	V
		receiving device	[6]	0.32	-	1.36	V
$R_{AUX\_TERM(DC)}$	AUX CH termination DC resistance	informative		-	100	-	Ω
$V_{AUX\_DC\_CM}$	AUX DC common-mode voltage		[7]	0	-	2.0	V
$V_{AUX\_TURN\_CM}$	AUX turnaround common-mode voltage		[8]	-	-	0.4	V
I_{AUX_SHORT}	AUX short-circuit current limit		[9]	-	-	90	mA
C_{AUX}	AUX AC coupling capacitor		[10]	75	-	200	nF

[1] Results in the bit rate of 1 Mbit/s including the overhead of Manchester II coding.

[2] Each pulse is a ‘0’ in Manchester II code.

[3] Period after the AUX CH STOP condition for which the bus is parked.

[4] Maximum allowable UI variation within a single transaction at connector pins of a transmitting device. Equal to 24 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[5] Maximum allowable UI variation within a single transaction at connector pins of a receiving device. Equal to 30 ns maximum. The transmitting device is a source device for a request transaction and a sink device for a reply transaction.

[6] $V_{AUX\_DIFFp-p} = 2 \times |V_{AUX+} - V_{AUX-}|$.

[7] Common-mode voltage is equal to V_{bias_TX} (or V_{bias_RX}) voltage.

[8] Steady-state common-mode voltage shift between transmit and receive modes of operation.

[9] Total drive current of the transmitter when it is shorted to its ground.

[10] The AUX CH AC coupling capacitor placed both on the DisplayPort source and sink devices.

12.4 HPD characteristics

Table 11. HPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output characteristics						
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA	2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA	-	-	0.8	V
I_{OSH}	HIGH-level short-circuit output current	drive HIGH; cell connected to ground	-	-	129	mA
I_{OSL}	LOW-level short-circuit output current	drive LOW; cell connected to V_{DD}	-	-	126	mA

12.5 DDC characteristics

Table 12. DDC characteristics

V_{CC} = 4.5 V to 5.5 V.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
V_{IH}	HIGH-level input voltage		2	-	5.5	V
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
$V_{I(hys)}$	hysteresis of input voltage		0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = 5.5 V	-	-	±1	µA
Output characteristics						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3.0	-	-	mA
$I_{O(sc)}$	short-circuit output current	drive LOW; cell connected to V_{DD}	-	-	40.0	mA
C_{io}	input/output capacitance	V_I = 3 V or 0 V; V_{DD} = 3.3 V	-	6	7	pF
		V_I = 3 V or 0 V; V_{DD} = 0 V	-	6	7	pF

[1] V_{CC} is the pull-up voltage for DDC.

12.6 DAC

Table 13. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{res(DAC)}$	DAC resolution		-	-	8	bit
f_{clk}	clock frequency		-	-	240	MHz
$\Delta I_{o(DAC)}$	DAC output current variation	DAC-to-DAC	-	-	4	%
INL	integral non-linearity		−1	±0.5	+1	LSB
DNL	differential non-linearity		−1	-	+1	LSB
$V_{o(DAC)}$	DAC output voltage		0	-	1.25	V
$C_{o(DAC)}$	DAC output capacitance		-	3.5	-	pF
$\alpha_{ct(DAC)}$	DAC crosstalk	between DAC outputs	-	−54	-	dB

12.7 HSYNC, VSYNC characteristics

Table 14. HSYNC and VSYNC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output characteristics						
V_{OH}	HIGH-level output voltage	I_{OH} = 8 mA	2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −8 mA	-	-	0.8	V
I_{OSH}	HIGH-level short-circuit output current	drive HIGH; cell connected to ground [1]	-	-	129.0	mA
I_{OSL}	LOW-level short-circuit output current	drive LOW; cell connected to V_{DD} [1]	-	-	126.0	mA

[1] The parameter values specified are simulated and absolute values.

12.8 Strap pins S[3:0]

Table 15. Strap pins S[3:0] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
V_{IH}	HIGH-level input voltage		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage				0.3 × V_{DD}	V
Weak pull-down characteristics						
I_{pd}	pull-down current	V_I = V_{DD}	25.0	50.0	95.0	µA

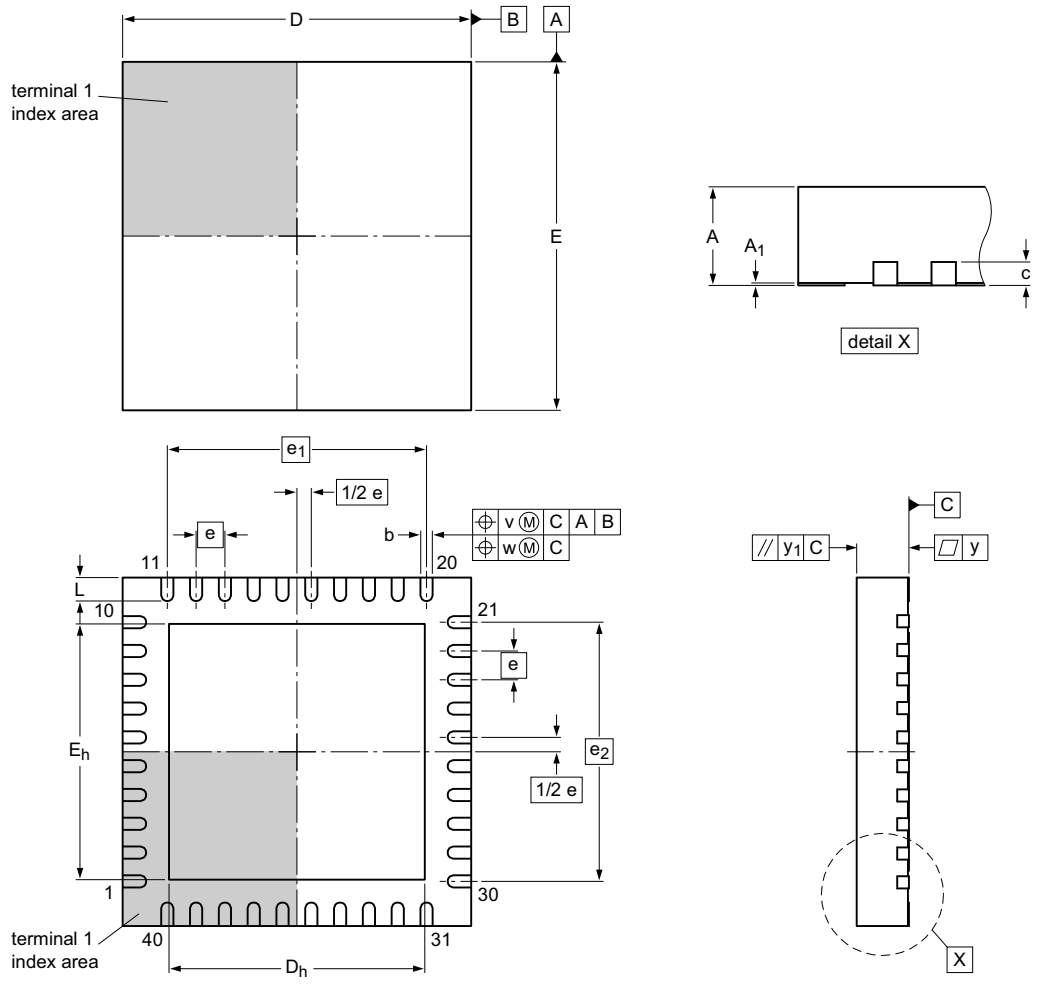
12.9 JTAG and RESET_N

Table 16. JTAG and RESET_N characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
V_{IH}	HIGH-level input voltage		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage				0.3 × V_{DD}	V
Output characteristics						
V_{OH}	HIGH-level output voltage	RESET_N; I_{OH} = 4 mA	2	-	-	V
		JTAG; I_{OH} = 2 mA	2	-	-	V
V_{OL}	LOW-level output voltage	RESET_N; I_{OL} = −4 mA	-	-	0.8	V
		JTAG; I_{OL} = −2 mA	-	-	0.8	V

13. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-6**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		6.1	4.55	6.1	4.55				0.5				
mm	nom	0.85	0.02	0.21	0.2	6.0	4.40	6.0	4.40	0.5	4.5	4.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	4.25	5.9	4.25				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-6_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT618-6		MO-220	- - -		~~09-02-23~~ 09-03-04

Fig 8. Package outline SOT618-6 (HVQFN40)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17 and 18

Table 17. SnPb eutectic process (from J-STD-020D)

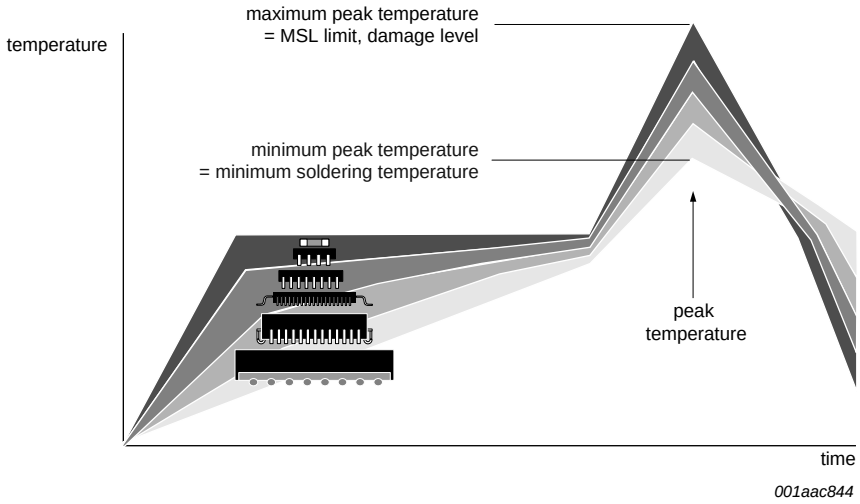
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 18. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 19. Abbreviations

Acronym	Description
AUX CH	Auxiliary Channel
BER	Bit Error Rate
bpc	bits per color
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CVT	Coordinated Video Timings
CVT RB	CVT Reduced Blanking
DAC	Digital-to-Analog Converter
DDC	Data Display Channel
DJ	Deterministic Jitter
DP	DisplayPort (VESA)
DPCD	DisplayPort Configuration Data
ECC	Error Correction Code
EDID	Extended Display Identification Data
ESD	ElectroStatic Discharge
HBM	Human Body Model
HBR	High Bit Rate
HDCP	High-bandwidth Digital Content Protection
HPD	Hot Plug Detect

Table 19. Abbreviations *...continued*

Acronym	Description
I^2C-bus	Inter-Integrated Circuit bus
IEC	International Electrotechnical Commission
I/O	Input/Output
LSB	Least Significant Bit
MCCS	Monitor Control Command Set (VESA)
MSB	Most Significant Bit
QXGA	Quad eXtended Graphics Array
RBR	Reduced Bit Rate
RGB	Red/Green/Blue
SSC	Spread Spectrum Clocking
SVGA	Super Video Graphics Array
SXGA	Super eXtended Graphics Array
TJ	Total Jitter
UI	Unit Interval
UXGA	Ultra eXtended Graphics Array
VESA	Video Electronics Standards Association
VGA	Video Graphics Array
VSIS	Video Signal Interface Standard
WUXGA	Wide Ultra eXtended Graphics Array
XGA	eXtended Graphics Array

16. References

[1] **VESA DisplayPort Standard —** Version 1, Revision 1a; January 11, 2008

[2] **Display Data Channel Command Interface Standard —** Version 1.1; October 29, 2004

[3] **Video Signal Standard (VSIS) —** Version 1, Rev. 2; December 12, 2002

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3393 v.4	20140610	Product data sheet	-	PTN3393 v.3
Modifications:	• Table 5 “Display resolution and pixel clock rate[1]” updated • Table 6 “Limiting values”: – Table note [1] updated to new ESD testing standards – Table note [2] updated to new ESD testing standards			
PTN3393 v.3	20130808	Product data sheet	-	PTN3393 v.2
PTN3393 v.2	20130422	Product data sheet	-	PTN3393 v.1
PTN3393 v.1	20130404	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 June 2014
Document identifier: PTN3393

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

PTN3393BSY PTN3393BS/F1Y